Fixed 1/ 2/ 4/ 8 Message Mode (C2.0)

Datasheet

Recording voice IC

■ FEATURES

- Operating Voltage Range: 3V ~ 6.5V
- Single Chip, High Quality Audio/Voice Recording & Playback Solution
  - ◆ No External ICs Required
  - ◆ Minimum External Components
- User Friendly, Easy to Use Operation
  - ◆ Programming & Development Systems Not Required
- 170/ 340/ 680 sec. Voice Recording Length in aPR33A1/aPR33A2/aPR33A3
- Powerful 16-Bits Digital Audio Processor.
- Nonvolatile Flash Memory Technology
  - ◆ No Battery Backup Required
- External Reset pin.
- Powerful Power Management Unit
  - ◆ Very Low Standby Current: 1uA
  - ◆ Low Power-Down Current: 15uA
  - ◆ Supports Power-Down Mode for Power Saving
- Built-in Audio-Recording Microphone Amplifier
  - ◆ No External OPAMP or BJT Required
  - ◆ Easy to PCB layout
- Configurable analog interface
  - ◆ Differential-ended MIC pre-amp for Low Noise
  - ◆ High Quality Line Receiver
- High Quality Analog to Digital and PWM module
  - ◆ Resolution up to 16-bits
- Simple And Direct User Interface
- Averagely 1,2,4 or 8 voice messages record & playback

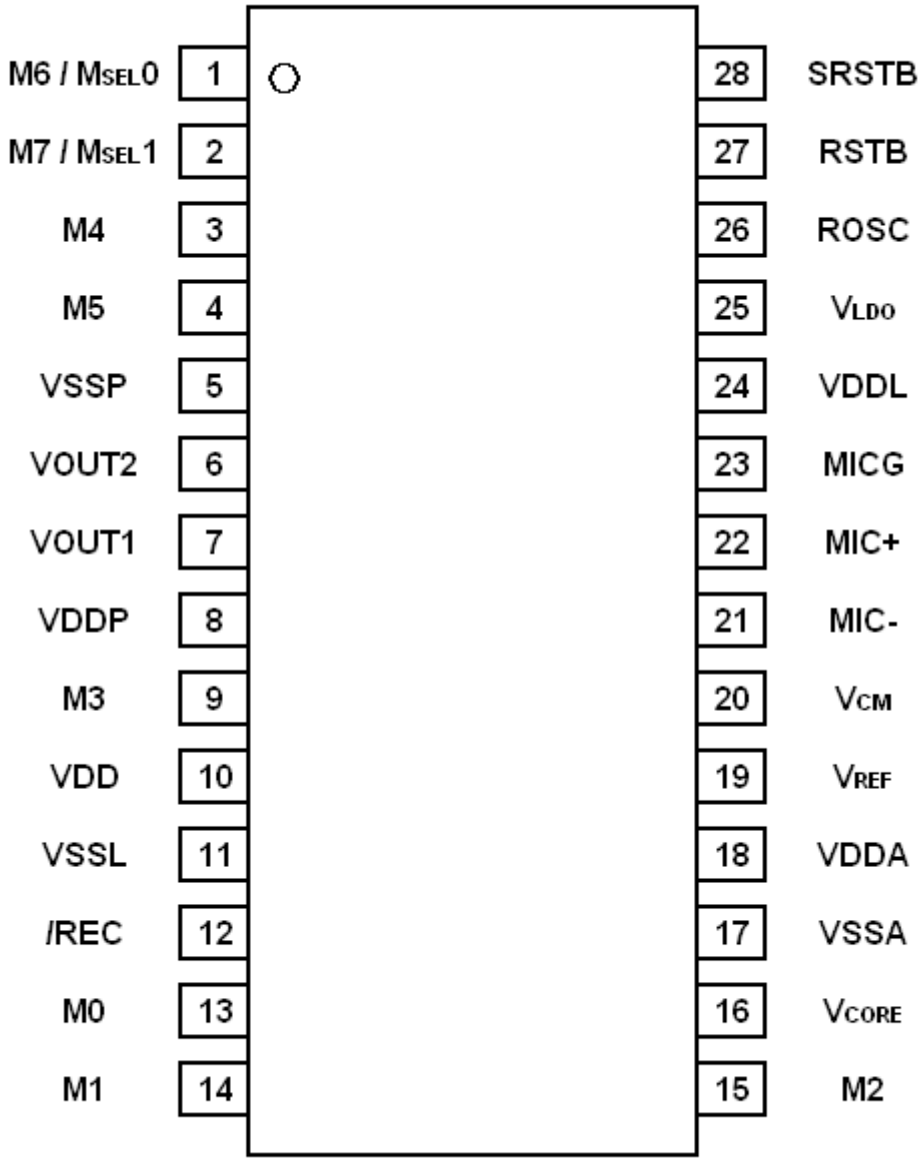
■ DESCRIPTION

Today's consumers demand the best in audio/voice. They want crystal-clear sound wherever they are in whatever format they want to use. APLUS delivers the technology to enhance a listener's audio/voice experience.

The aPR33A series are powerful audio processor along with high performance audio analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). The aPR33A series are a fully integrated solution offering high performance and unparalleled integration with analog input, digital processing and analog output functionality. The aPR33A series incorporates all the functionality required to perform demanding audio/voice applications. High quality audio/voice systems with lower bill-of-material costs can be implemented with the aPR33A series because of its integrated analog data converters and full suite of quality-enhancing features such as sample-rate convertor.

The aPR33A series C2.0 is specially designed for simple key trigger, user can record and playback the message averagely for 1, 2, 4 or 8 voice message(s) by switch, It is suitable in simple interface or need to limit the length of single message, e.g. toys, leave messages system, answering machine etc. Meanwhile, this mode provides the power-management system. Users can let the chip enter power-down mode when unused. It can effectively reduce electric current consuming to 15uA and increase the using time in any projects powered by batteries.

■ PIN CONFIGURATION

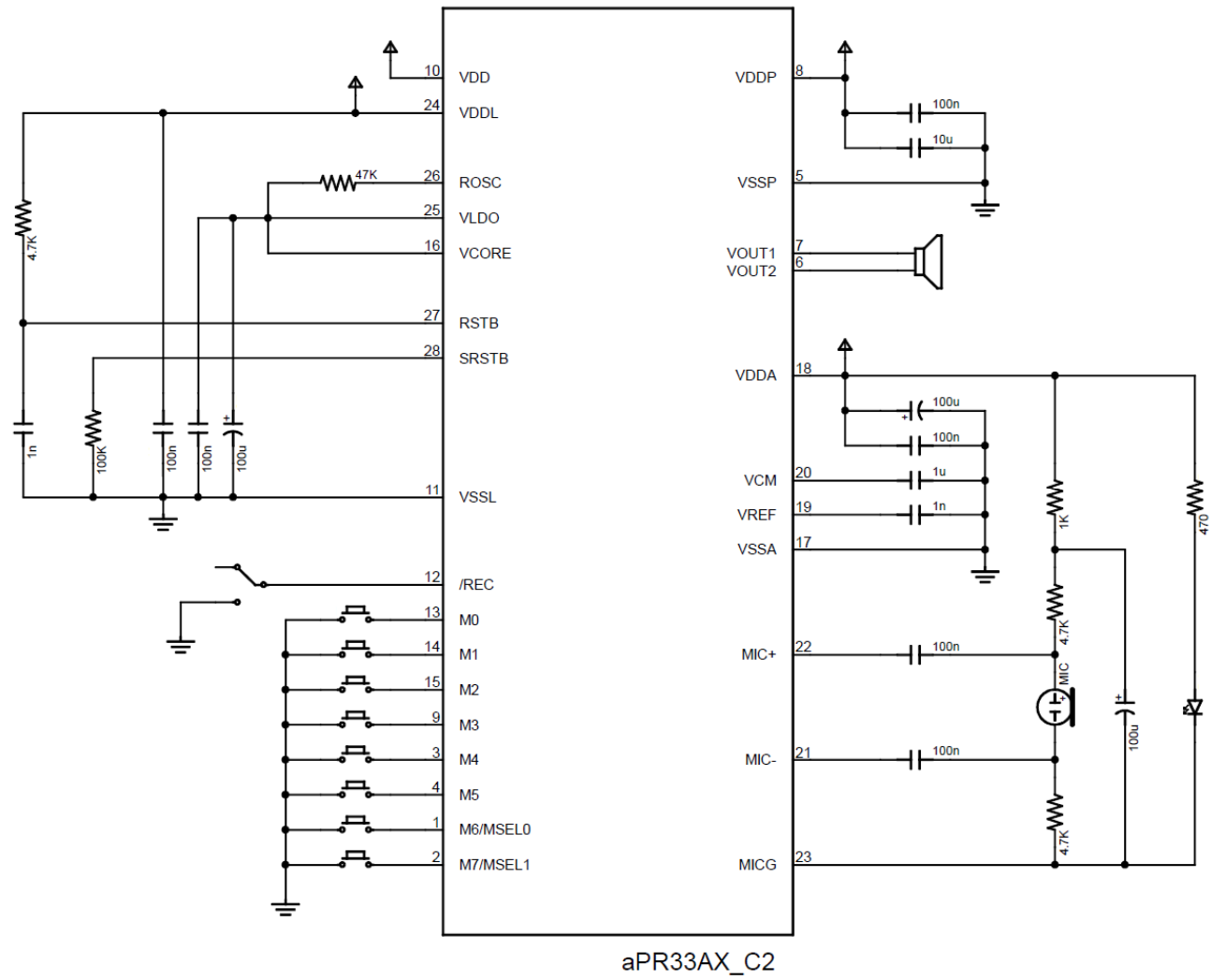


SOP Package

■ PIN DESCRIPTION

Pin Names	Pin No	TYPE	Description
VDDP VDD VDDA VDDL	8 10 18 24		Positive power supply.
VSSP VSSL VSSA	5 11 17		Power ground.
V_{LDO}	25		Internal LDO output.
V_{CORE}	16		Positive power supply for core.
V_{REF}	19		Reference voltage.
V_{CM}	20		Common mode voltage.
Rosc	26	INPUT	Oscillator resistor input.
RSTB	27	INPUT	Reset. (Low active)
SRSTB	28	INPUT	System reset, pull-down a resistor to the VSSL.
MIC+ MIC-	21 22	INPUT	Microphone differential input.
MICG	23	OUTPUT	Microphone ground.
VOUT2 VOUT1	6 7	OUTPUT	PWM output to drive speaker directly.
/REC	12	INPUT	Record Mode. (Low active)
M0	13	INPUT	Message-0.
M1	14	INPUT	Message-1.
M2	15	INPUT	Message-2.
M3	9	INPUT	Message-3.
M4	3	INPUT	Message-4.
M5	4	INPUT	Message-5.
M6 / $M_{SEL}0$	1	INPUT	Message-6, Message select 0.
M7 / $M_{SEL}1$	2	INPUT	Message-7, Message select 1.

■ TYPICAL APPLICATION



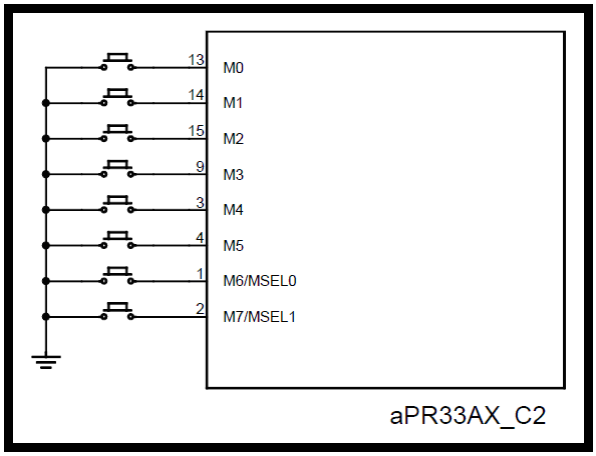
■ MESSAGE MODE

In fixed 1/ 2/ 4/ 8 message mode (C2.0), user can divide the memory averagely for 1, 2, 4 or 8 message(s). The message mode will be applied after chip reset by the MSEL0 and MSEL1 pin.

Please note the message should be recorded and played in same message mode, we CAN NOT guarantee the message is complete after message mode changed. For example, user recorded 8 messages in the 8-message mode, those messages can be played in 8-message mode only. If user changed to 1, 2 or 4 message mode, system will discard those messages.

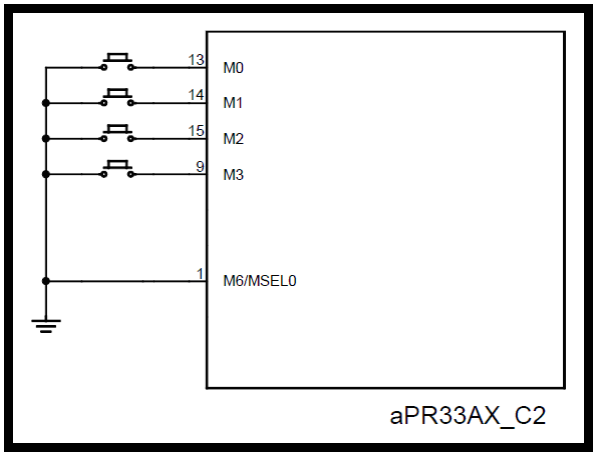
- 8-Message Mode

  The memory will be divided to 8 messages averagely when both MSEL0 and MSEL1 pin float after chip reset.



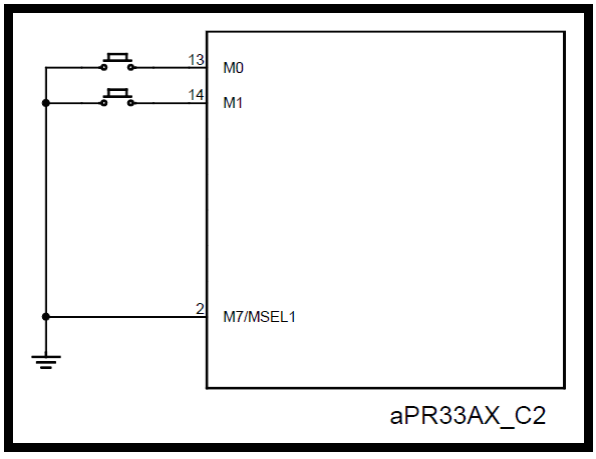
- 4-Message Mode

  The memory will be divided to 4 messages averagely when MSEL0 pin connected to VSS and MSEL1 pin float after chip reset.



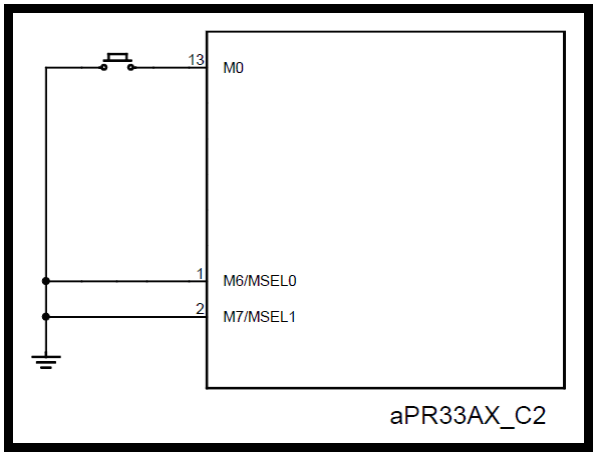
- 2-Message Mode

  The memory will be divided to 2 messages averagely when MSEL1 pin connected to VSS and MSEL0 pin float after chip reset.



- 1-Message Mode

  The memory will be for 1 message when both MSEL0 and MSEL1 pin connected to VSS after chip reset.



■ RECORD MESSAGE

During the /REC pin drove to V_{IL}, chip in the record mode.

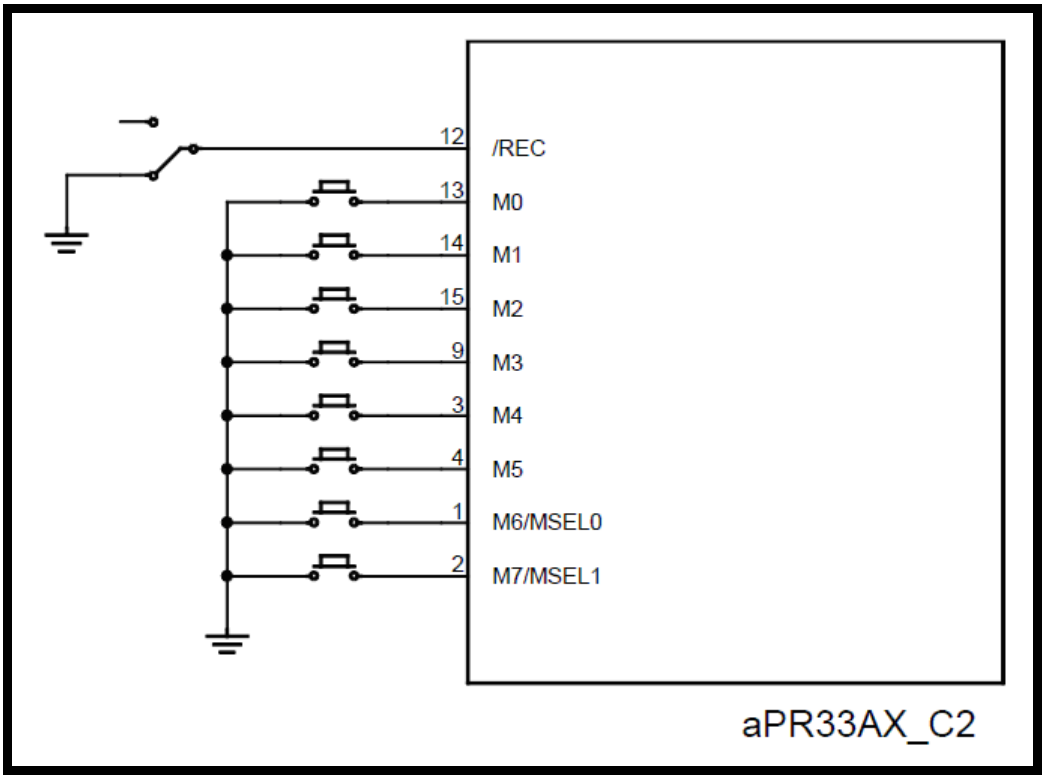
When the message pin (M0, M1, M2 … M7) drove to V_{IL} in record mode, the chip will playback “beep” tone and message record starting.

The message record will continue until message pin released or full of this message, and the chip will playback “beep” tone 2 times to indicate the message record finished.

If the message already exist and user record again, the old one’s message will be replaced.

The following fig. showed a typical record circuit for 8-message mode. We connected a slide-switch between /REC pin and VSS, and connected 8 tact-switches between M0 ~ M7 pin and VSS. When the slide-switch fixed in VSS side and any tact-switch will be pressed, chip will start message record and until the user releases the tact-switch.

Note: After reset, /REC and M0 to M7 pin will be pull-up to VDD by internal resistor.



■ PLAYBACK MESSAGE

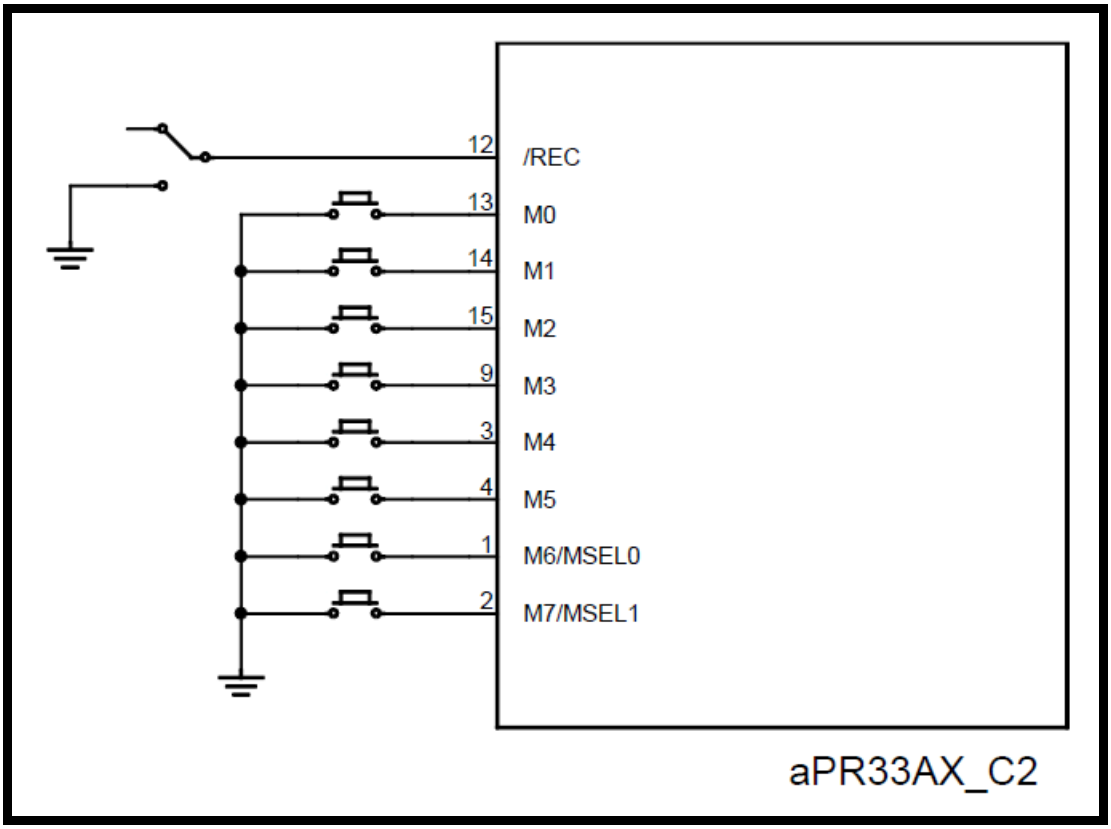
During the /REC pin drove to V_{IH}, chip in the playback mode.

When the message pin (M0, M1, M2 … M7) drove from V_{IH} to V_{IL} in playback mode, the message playback starting.

The message playback will continue until message pin drove from V_{IH} to V_{IL} again or end of this message.

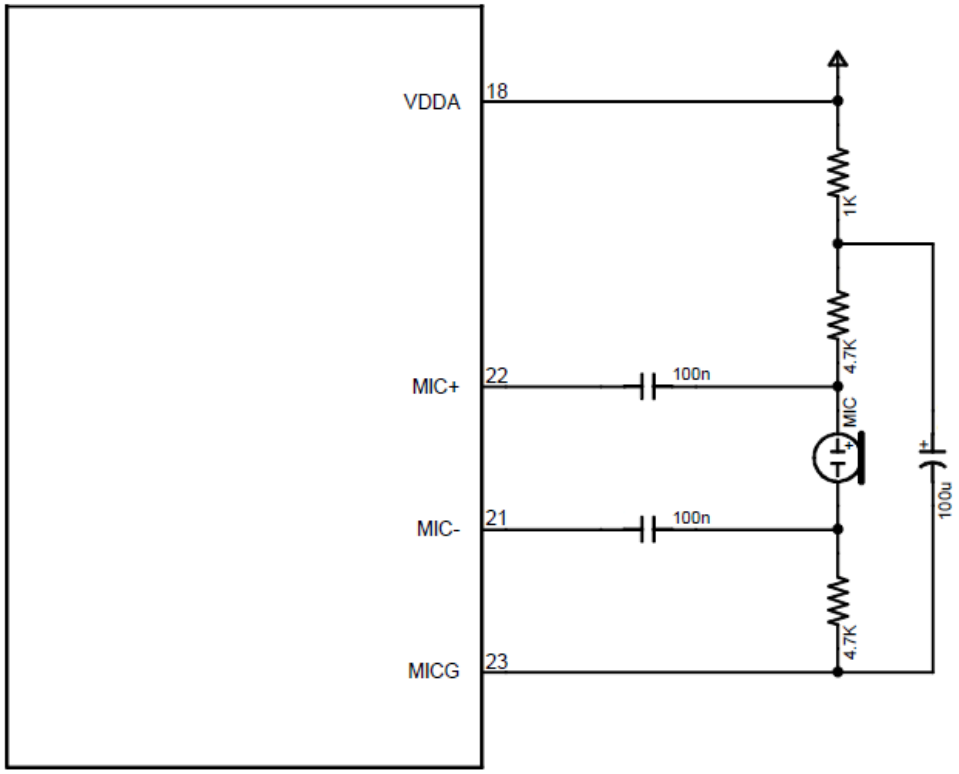
The following fig. showed a typical playback circuit for 8-message mode. We connected a slide-switch between /REC and VSS, and connected 8 tact-switches between M0 ~ M7 and VSS. When the slide-switch fixed in float side and any tact-switch will be pressed, chip will start message playback and until the user pressed the tact-switch again or end of message.

Note: After reset, /REC and M0 to M7 pin will be pull-up to VDD by internal resistor.

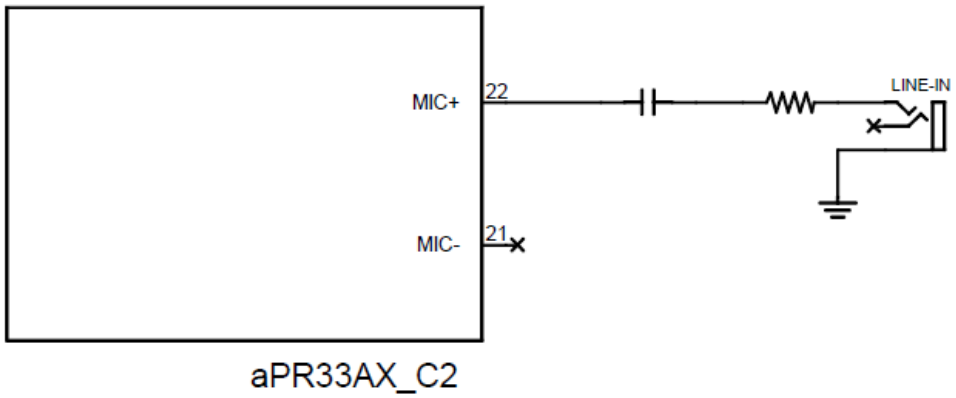


■ VOICE INPUT

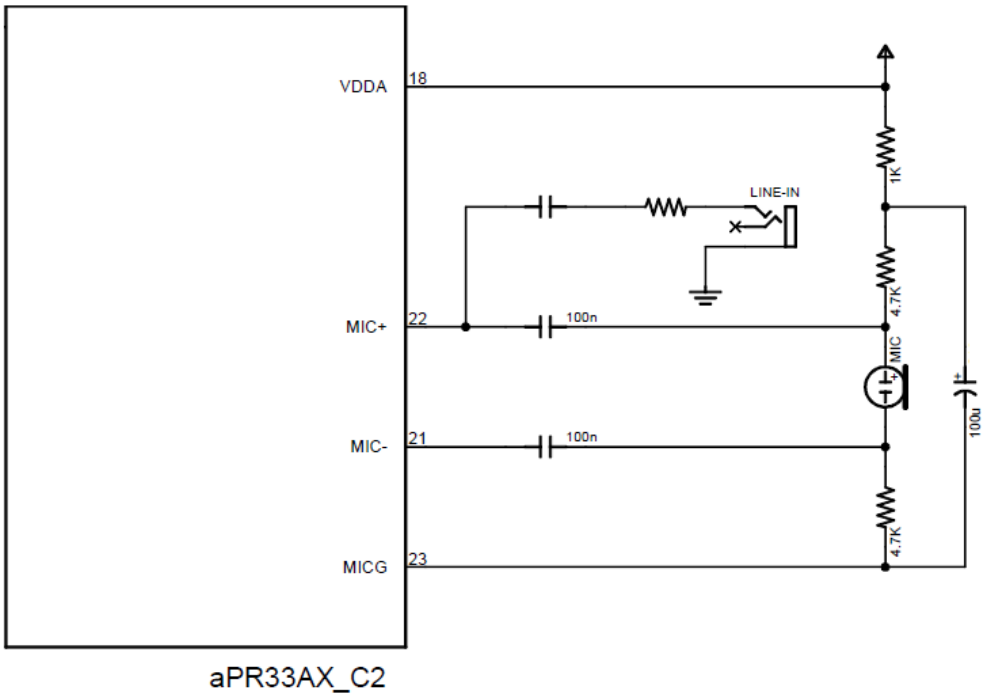
The aPR33A series supported single channel voice input by microphone or line-in. The following fig. showed circuit for different input methods: microphone, line-in and mixture of both.



(A) Microphone



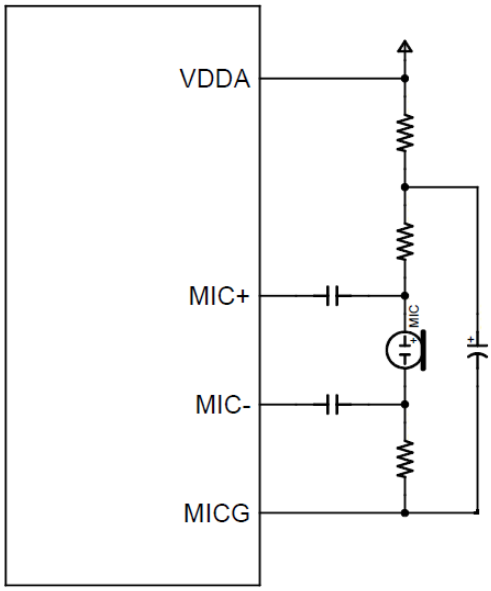
(B) Line-In



(C) Microphone + Line-In

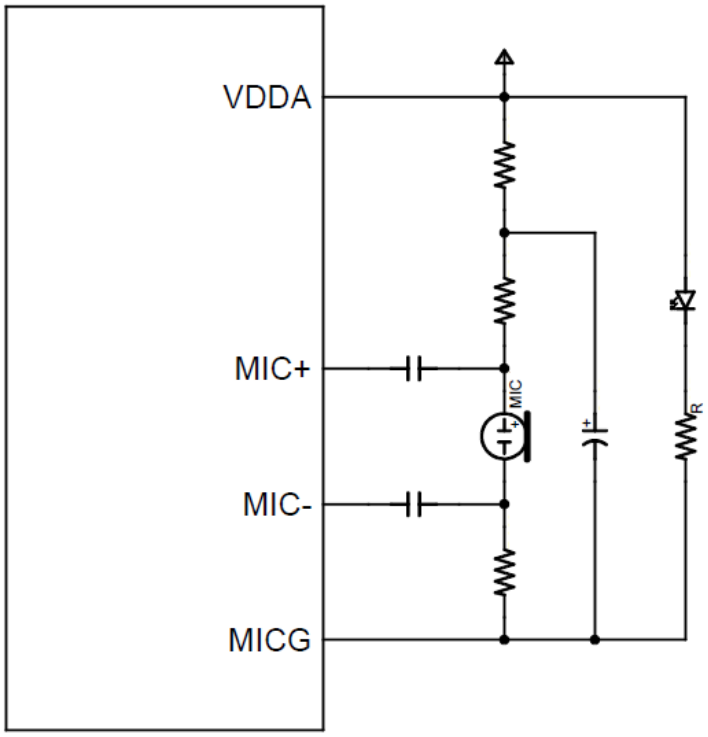
■ BUSY

The MICG pin will be drove to low during the message record or playback, and drove to high during idle or standby, user can detect MICG status to know chip is busy or not.

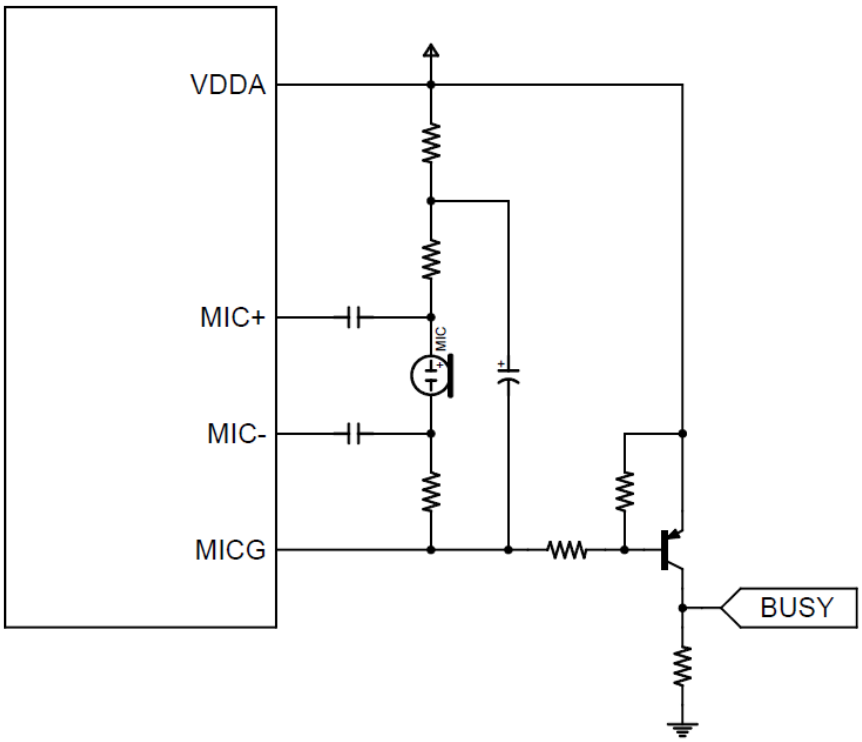


Please note it is limited for MICG pin driving current. Reference to I_{OH} and I_{OL} in section "**DC CHARACTERISTICS"**. If MICG pin is over loading from external circuit, it will cause noise in microphone circuit.

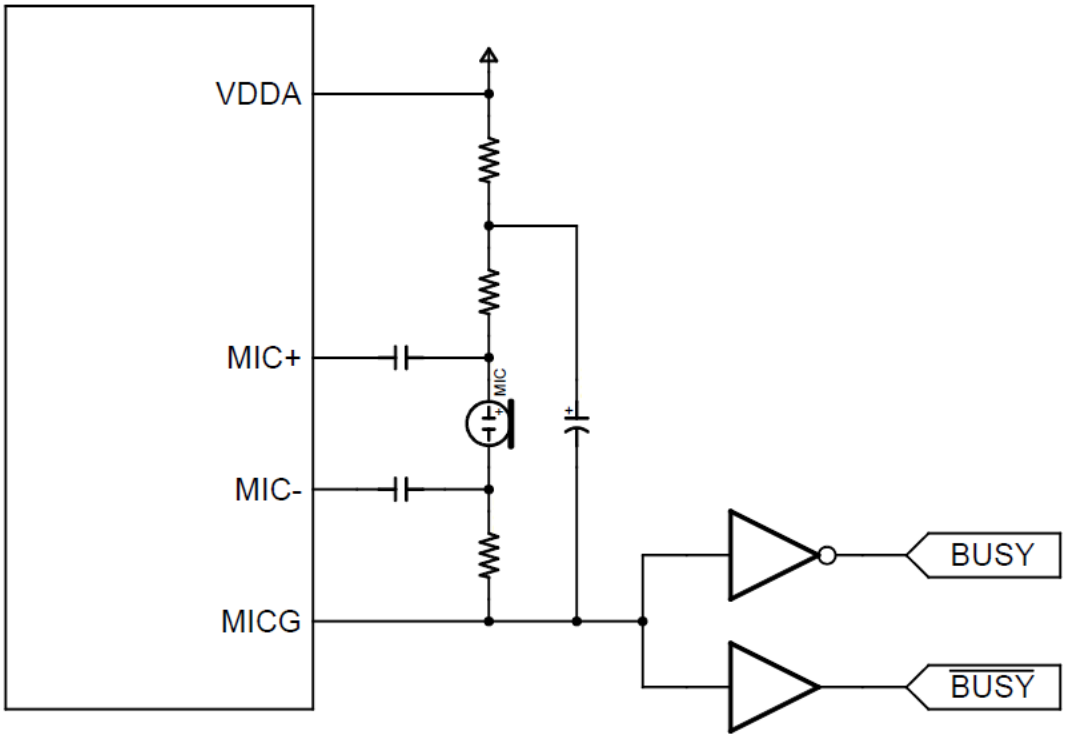
Below is a typical application. We add one LED to indicate IC record and playback status. We use one Resistor to limit current. And suggest R> 470Ω



Below Transistor circuit is to get higher current, larger than I_{OH} or I_{OL}.



To get best sound quality, we can use buffer or inverter to isolate MICG to avoid noise from external circuit. Driving current is provided by buffer(inverter) only.

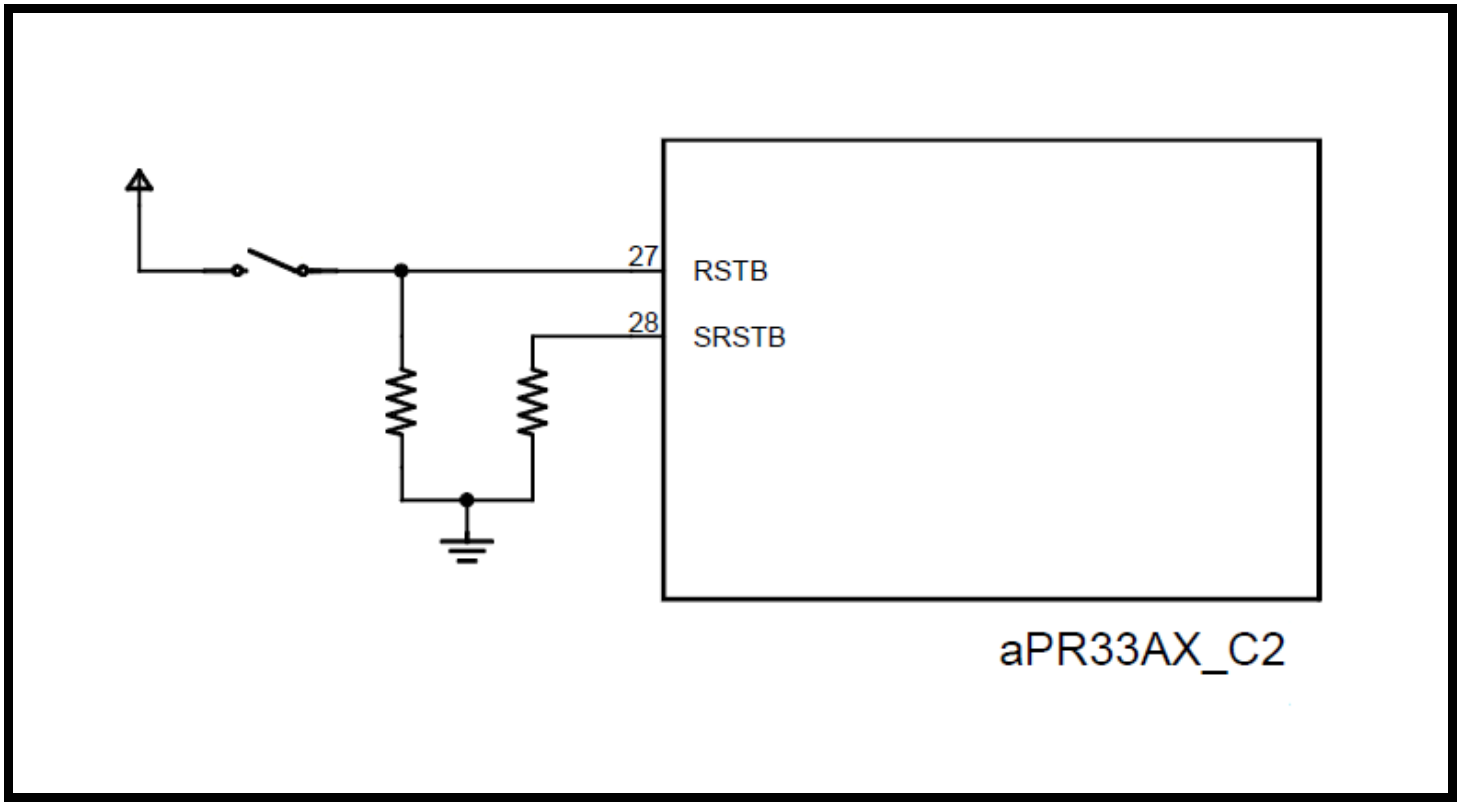


■ RESET

aPR33A series can enter standby mode when RSTB pin drive to low. During chip in the standby mode, the current consumption is reduced to I_{SB} and any operation will be stopped, user also can not execute any new operate in this mode.

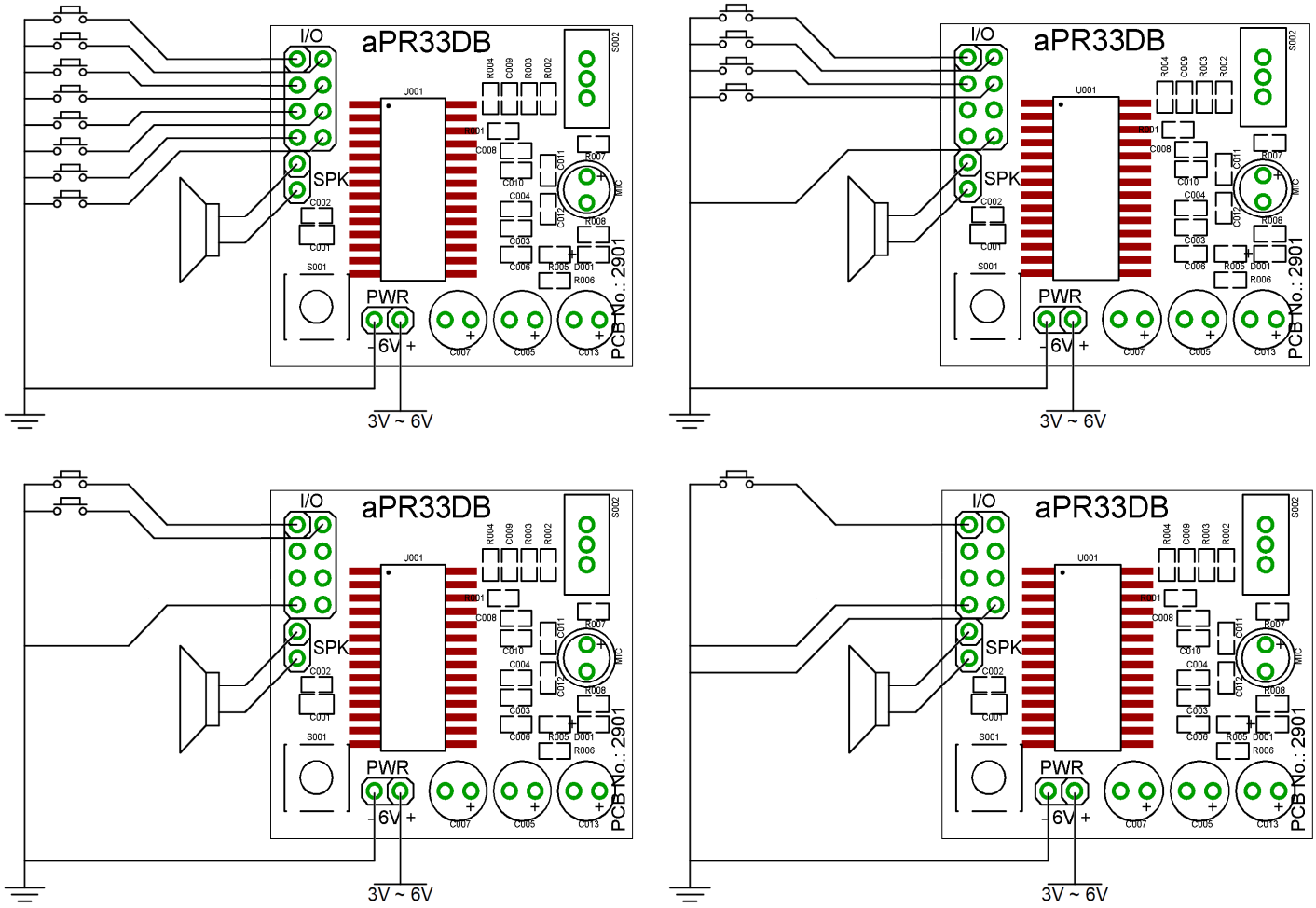
The standby mode will continue until RSTB pin goes to high, chip will be started to initial, and playback “beep” tone to indicate enter idle mode.

User can get less current consumption by control RSTB pin specially in some application which concern standby current.



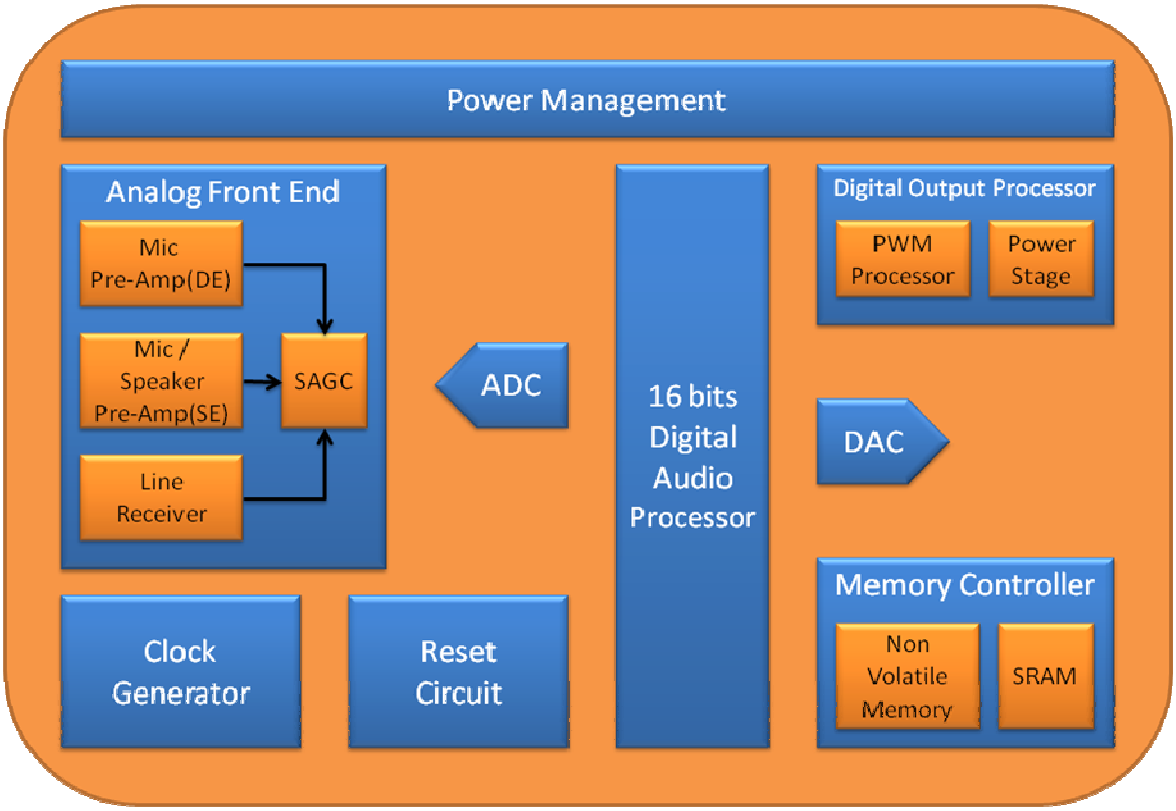
■ EXAMPLE

The aPR33DB is one of the simplest solutions for achieve fixed 1/ 2/ 4/ 8 message mode demo. The circuit board already includes the peripheral circuit which containing microphone. Developers only need to notice how to connect with their development environment. It can effectively decrease the time of circuit connecting & any possible mistakes. Below figure shows how to connect aPR33DB with external key in fixed 1/ 2/ 4/ 8 message mode:



■ BLOCK DIAGRAM

Figure 1. Block Diagram



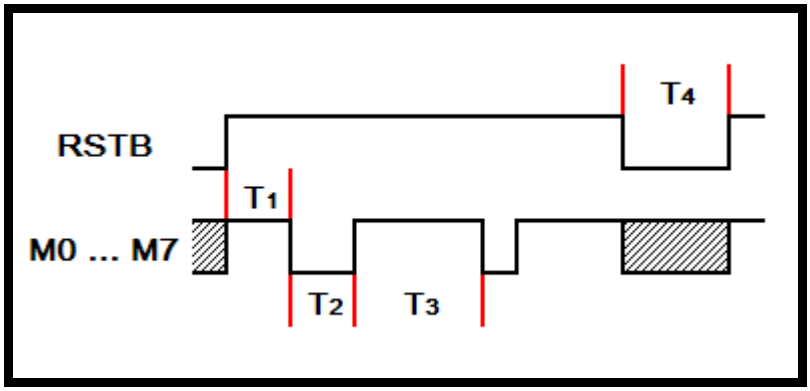
■ ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Unit
VDD – VSS	-0.3 ~ +10.0	V
V_{IN}	VSS-0.3 < V_{IN} < VDD+0.3	V
V_{OUT}	VSS < V_{OUT} < VDD	V
T(Operating)	-40 ~ +85	℃
T(Junction)	-40 ~ +125	℃
T(Storage)	-40 ~ +125	℃

■ DC CHARACTERISTICS

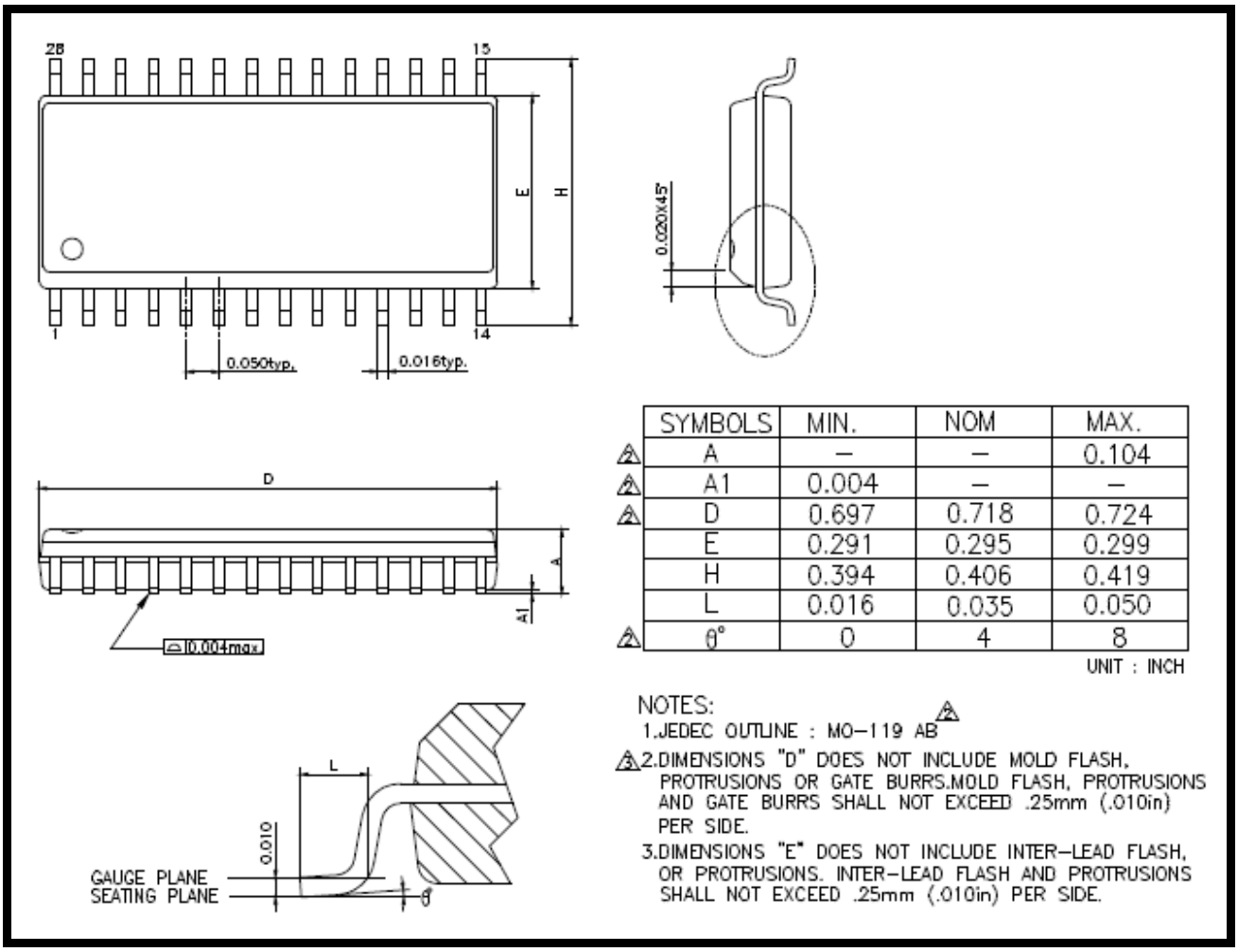
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
VDD	Operating Voltage	3.0		6.5	V	
I_{SB}	Standby Current			1	μA	
I_{PDN}	Power-Down Current		15	20	μA	
$I_{OP(IDLE)}$	Operating Current (Idle)		20		mA	VDD = 5V
$I_{OP(REC)}$	Operating Current (Record)		35		mA	VDD = 5V
$I_{OP(PLAY)}$	Operating Current (Playback)		25		mA	VDD = 5V
V_{IH}	"H" Input Voltage	2.5			V	
V_{IL}	"L" Input Voltage			0.6	V	
I_{VOUT}	VOUT Current		185		mA	
I_{OH}	O/P High Current		8		mA	VDD = 5V / VOH=4.5V
I_{OL}	O/P Low Current		14		mA	VDD = 5V / VOH=0.5V
R_{NPIO}	Input pin pull-down resistance		300		KΩ	External floating or drive low.
			1		MΩ	External drive high.
R_{UPIO}	Input pin pull-up resistance		4.7		KΩ	
△Fs/Fs	Frequency stability			5	%	VDD = 5V ± 1.0V
△Fc/Fc	Chip to chip Frequency Variation			5	%	Also apply to lot to lot variation.

■ AC CHARACTERISTICS



Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T1	/CS Setup Time	100	--	--	mS	VDD=5.0V
T2	Trigger Setup Time	16	--	--	mS	VDD=5.0V
T3	Trigger Hold Time	16	--	--	mS	VDD=5.0V
T4	/CS Hold Time	100	--	--	uS	VDD=5.0V

■ PACKAGE INFORMATION



	SYMBOLS	MIN.	NOM	MAX.
2	A	–	–	0.104
2	A1	0.004	–	–
2	D	0.697	0.718	0.724
	E	0.291	0.295	0.299
	H	0.394	0.406	0.419
	L	0.016	0.035	0.050
2	θ°	0	4	8

UNIT : INCH

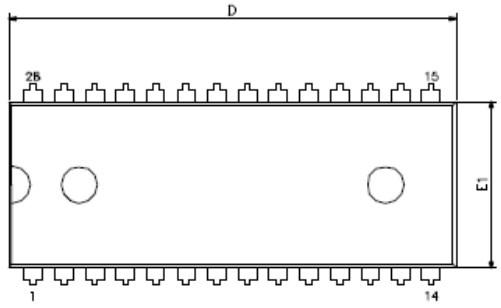
NOTES:

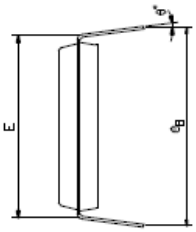
1.JEDEC OUTLINE : MO-119 AB 2

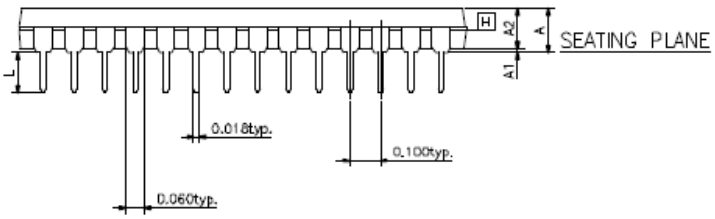
2 2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

28Pin 600mil DIP Package







SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.220
A1	0.015	–	–
A2	0.150	0.155	0.160
D	1.455	1.460	1.470
E		0.600 BSC	
E1	0.540	0.545	0.550
⚠ L	0.115	0.158	0.200
e_B	0.630	0.650	0.670
θ°	0	7	15

UNIT : INCH

NOTE:
1.JEDEC OUTLINE : MS-011 AB
2.E1 DOES NOT INCLUDE MOLD FLASH.