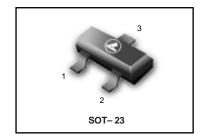


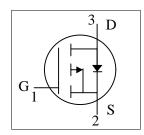
20V P-Channel Enhancement-Mode MOSFET

•FEATURES

- 1) VDS =-20V
- 2) RDS(ON), Vgs@-2.5V, Ids@-2.0A=150m Ω
- 3) RDS(ON), Vgs@-4.5V, Ids@-2.8A=100m Ω
- 4) Advanced trench process technology
- 5) High Density Cell Design For Ultra Low On-Resistance
- 6) Fully Characterized Avalanche Voltage and Current
- 7) Improved Shoot-Through FOM
- 8) Simple Drive Requirement
- 9) Small Package Outline
- 10) Surface Mount Device
- 11) We declare that the material of product compliant with RoHS requirements and Halogen Free .

LP2301LT1G





DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LP2301LT1G	01	3000/Tape&Reel
LP2301LT3G	01	10000/Tape&Reel

ullet MAXIMUM RATINGS(Ta = 25 $^{\circ}$ C)

Parameter		Symbol	Limits	Unit		
Drain-to-Source Voltage		VDSS	-20	V		
Gate-to-Source Voltage		Vgs	±8	V		
Continuous DrainCurrent		ID	-2.3	Α		
Maximum Power Dissipation	$TA = 25^{\circ}C$	PD	0.9	W		
lviaximum Power Dissipation	$TA = 75^{\circ}C$	PD	0.57			
Pulsed Drain Current		lом	-8	Α		
Operating and Storage Temperature						
Range		TJ, Tstg	−55 to +150	°C		
Thermal Resistance-Junction to						
Ambient(Note1)		RθJA	175	°C/W		

^{1.}The device mounted on 1in² FR4 board with 2 oz copper

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VGS = 0 V,

Is = -0.75A

●ELECTRICAL CHARACTERISTICS (Ta= 25°C)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Static						•
Drain-to-Source Breakdown						VGS = 0 V,
Voltage	V(BR)DSS	-20	_	_	V	ID = -250 μA
						VGS = VDS,
Gate Threshold Voltage	VGS(TH)	-0.4	_	0.9	V	ID = -250 μA
						VDS=-9.6V,
Zero Gate Voltage Drain Current	IDSS	_	_	-1	μΑ	VGS=0V
Gate-to-Source Leakage						VDS = 0 V,
Current	IGSS		_	±100	nA	VGS = ±8 V
						VGS = -4.5 V,
		_	69	100	$m\Omega$	ID =-2.8 A
Drain-to-Source On Resistance	_					VGS = -2.5 V,
(Note2)	RDS(on)	_	83	150	mΩ	ID = -2 A
					•	VDS = -5 V,
Forward Transconductance	g_{fs}	_	6.5	_	S	ID = -4 A
DVALARAIO						
DYNAMIC Total Cata Charge	0.		45.00			VGS =-4.5 V,
Total Gate Charge	Qg		15.23	_	20	VGS =-4.5 V, VDS = -6 V
Gate-to-Source Gate Charge	Qgs		5.49		nC	ID = -2.8 A
Gate-to-Drain Charge	Qgd		2.74	_		ID = -2.0 A
Turn-On Delay Time	td(on)		17.28	_		\/D0_0\/\ D1_=0.0
Rise Time	tr		3.73	_	ns	VDS=-6V, RL =6 Ω
Turn-Off Delay Time	td(off)		36.05	_		RGEN=6 Ω , VGS=-4.5V
Fall Time	tf Oine		6.19	_		=
Input Capacitance	Ciss		882.5			VGS = 0 V, f = 1.0
Output Capacitance	Coss		145.5		pF	MHz,
Reverse Transfer Capacitance	Crss		97.26			VDS= -6 V
SOURCE-DRAIN DIODE						
Max. Diode Forward Current	Is		l <u>_</u>	-2.4	A	
vian. Diodo i di wala dalibil	10	_	. –		$\overline{}$	i

Forward Diode Voltage

VSD

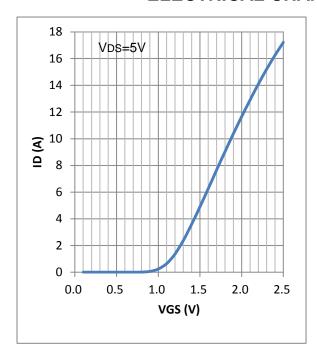
-0.8

-1.2

^{2.} Pulse Test: Pulse width $\!\!\leqslant\! 300\mu s,$ duty cycle $\!\!\leqslant\! 2\%.$



ELECTRICAL CHARACTERISTIC CURVES



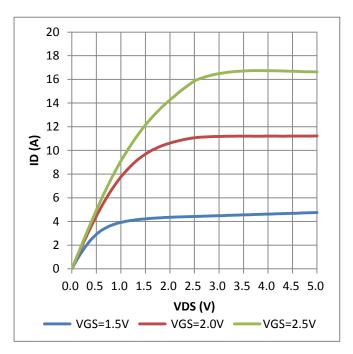
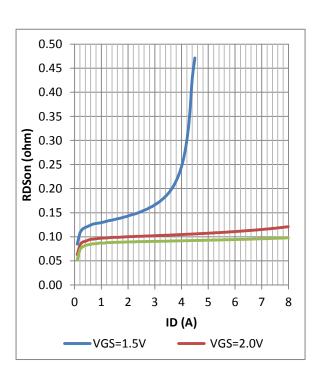


FIG.1 Transfer Characteristics

FIG.2 On-Region Characteristics



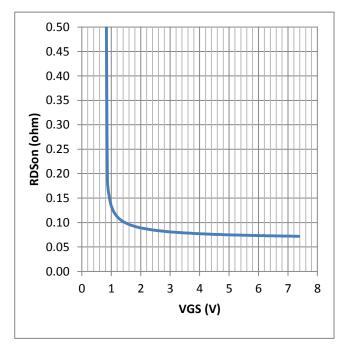


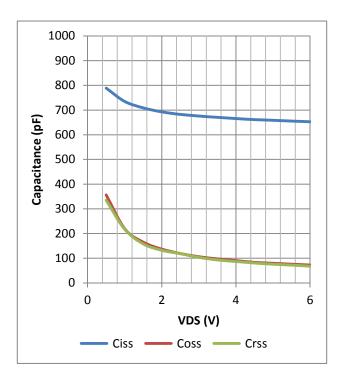
FIG.3 On-Resistance versus Drain Current

FIG.4 On-Resistance vs. Gate-to-Source Voltage

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ELECTRICAL CHARACTERISTIC CURVES



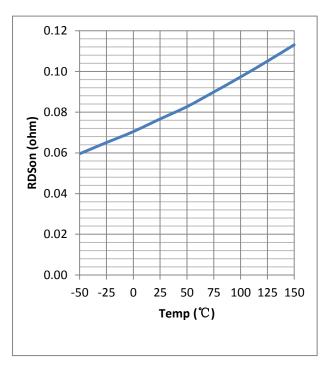


FIG.6 Capacitance

FIG.7 On-Resistance vs. Junction Temperature

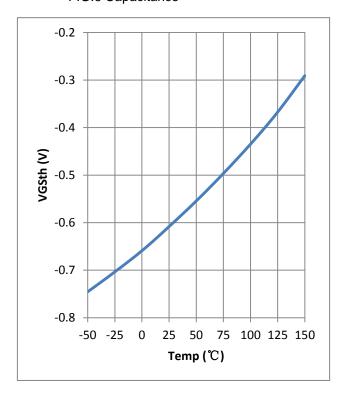
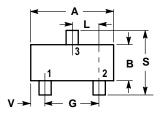


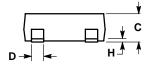
FIG.8 Vth vs. Junction Temperature

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SOT-23



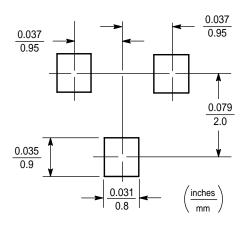




NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M,1982
- 2. CONTROLLING DIMENSION: INCH.

DIM	IN	ICHES	MILLIMETERS		
D.I.V.	MIN	MAX	MIN	MAX	
Α	0.1102	0.1197	2.80	3.04	
В	0.0472	0.0551	1.20	1.40	
С	0.0350	0.0440	0.89	1.11	
D	0.0150	0.0200	0.37	0.50	
G	0.0701	0.0807	1.78	2.04	
Н	0.0005	0.0040	0.013	0.100	
J	0.0034	0.0070	0.085	0.177	
K	0.0140	0.0285	0.35	0.69	
L	0.0350	0.0401	0.89	1.02	
S	0.0830	0.1039	2.10	2.64	
V	0.0177	0.0236	0.45	0.60	



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