

# Understanding ZigBee transmission

A transmitter model with digital VHDL models, Verilog-AMS analog models and SPICE descriptions can be used to accurately simulate the transmitter path of a ZigBee device.

By Cyril Descleves

**T**oday's high technology marketplace demands more capability and reliability from wireless technologies. This is especially true of low-cost, low-power wireless communications with relatively low data rates for applications such as home automation systems, games and automotive controls. Requirements for these radio transceiver systems make a highly integrated CMOS implementation an obvious choice. ZigBee wireless technology and its underlying IEEE 802.15.4 standard is an attractive low-cost, low-power wireless solution designed to fulfill these needs.

From a design point of view, the high integration level of this type of CMOS device means that analog, RF and DSP functions must be tightly connected and operating together. To fully understand the device's transmitter path, it is necessary to simulate the entire system, which includes a collection of different signals and functional blocks. A comprehensive simulation tool must be used that handles such a wide variety of signal types.

## Understanding the ZigBee architecture

The physical level (PHY) of the 802.15.4 standard specifies two bands of operation—2.4 GHz and 868 MHz to 915 MHz. This article will address the case for 802.15.4 2.4 GHz operation.

The standard specifies how the data coding, spreading and modulation must be performed for the 2.4 GHz PHY. Starting from the raw baseband bit stream, bits are examined by groups of four bits. Each four-bit sequence is mapped to one symbol out of 16

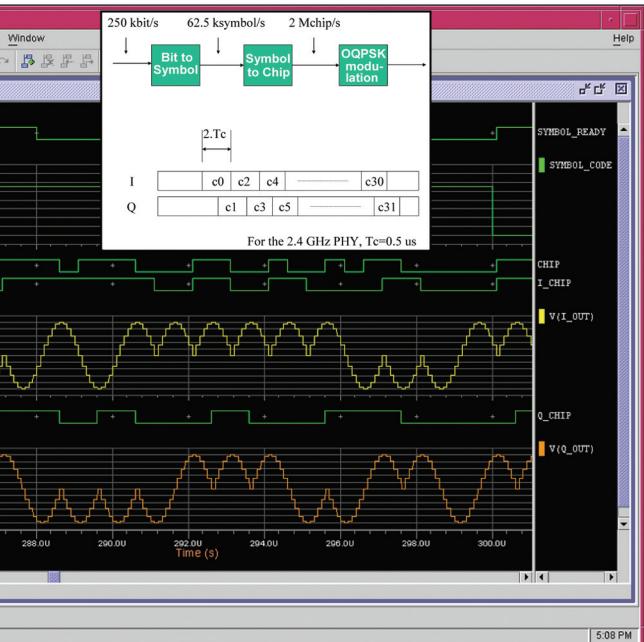


Figure 1. Shown here is the I/Q chip sequence generation and O-QPSK modulation with half-sine pulse shaping.

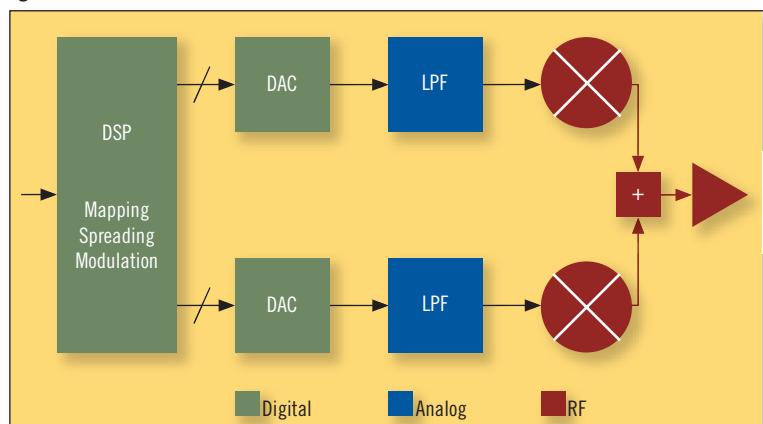


Figure 2. This graphic depicts the simplified transmitter architecture to be simulated.

possible symbols. Each symbol is in turn mapped to a 32-chip sequence. These sequences are pseudo random and nearly orthogonal. Note that the 16 different 32-chip

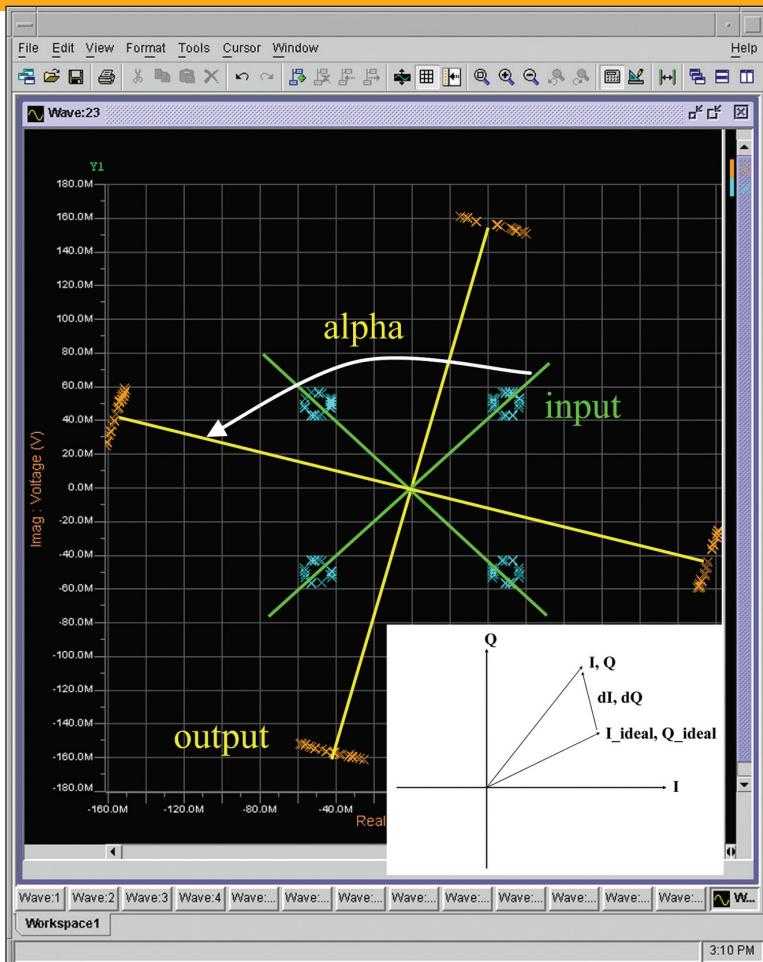
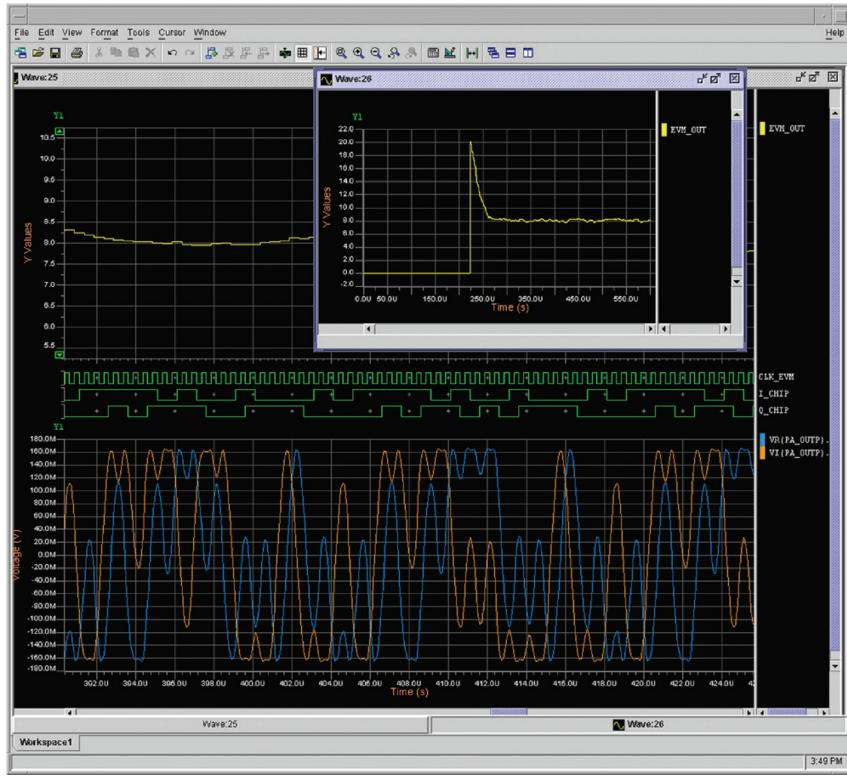


Figure 3. The constellation diagram function of the waveform viewer graphically depicts input and output constellation diagrams.



random sequences corresponding to the 16 possible symbols are specified in the 802.15.4 standard and are implemented in the simulation test bench. The chip stream itself is offset quadrature phase shift keying (O-QPSK) modulated with half-sine pulse shaping. This modulation format is also known as minimum shift keying (MSK).

Odd and even chip streams are generated the same way they would be for standard QPSK, with the exception that for O-QPSK they are shifted by one chip period (Figure 1). The shifting avoids having I and Q simultaneously crossing the 0 value, which could cause large amplitude variations in the envelope.

As shown in Figure 2, the architecture of the ZigBee transmitter used for this simulation is inspired from an article published in the November 2004 issue of *RF Design* by Khanh Tuan Le, entitled, “Designing a ZigBee-ready IEEE 802.15.4-compliant radio transceiver.” In this implementation, the I and Q data is low-pass filtered to smooth out the effect of the digital-to-analog conversions and passed to upconverting quadrature mixers. The RF signal is then combined and passed through the power amplifier (PA). The digital-to-analog converters (DACs) are embedded in the modulator model. The number of bits used for the conversion is programmable and appears as a model parameter. The oversampling rate is programmable and it is set to 10 MHz.

The transmitter’s digital processing section includes the clock and reset generators, a pseudo random bit generator, the chip sequence generation, and the O-QPSK modulation with half-sine pulse shaping. The signals

Figure 4. The simulation results in this graphic show the digital baseband IQ data, the O-QPSK modulation with half-sine pulse shaping, and the low-pass filtering and amplification. The EVM output is shown using the full simulation scale in the small inner window. The sharp transition occurs because the model starts writing out data at a certain time, when enough symbols have been sampled to compute a realistic EVM estimate. Before that time, the output is arbitrarily forced to zero. The output quickly converges to a stable percentage value, which is the estimated EVM.

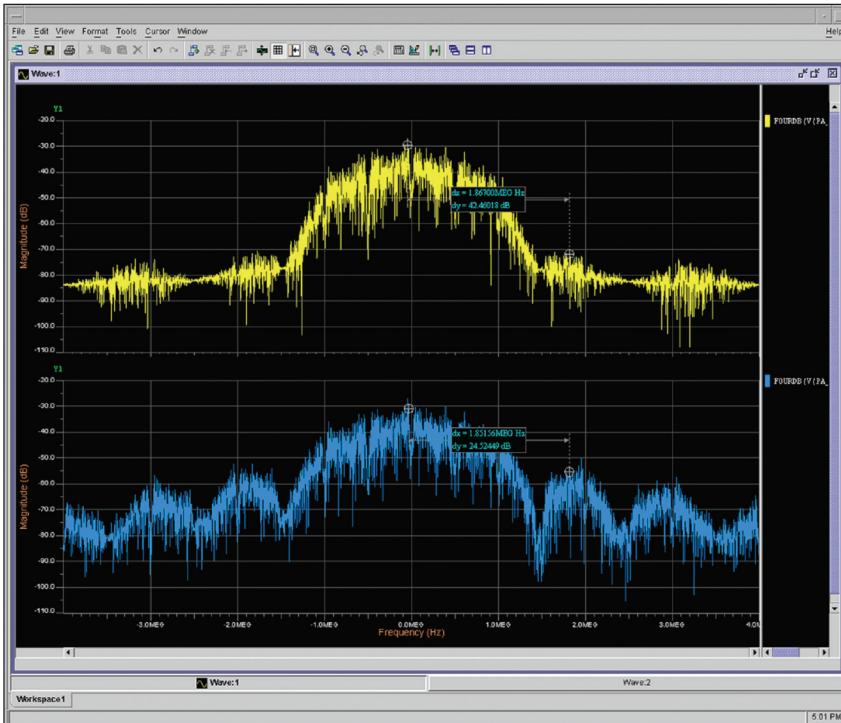


Figure 5. The modulation spectrum at the PA's output will differ depending on the filtering configuration.

out of the O-QPSK modulator are ‘real’ type VHDL signals. The number of conversions per chip period is programmable to easily explore the impact of this parameter on the overall performance and modulation spectrum.

The digital signal processing is modeled with VHDL. Several blocks are directly borrowed from a library of behavioral models that are available in VHDL-AMS and Verilog-AMS. The documented source code for the models is provided with the simulator. In addition, application-specific models need to be coded manually. For example, a VHDL model is used to generate the exact pseudo-random nearly orthogonal chip sequences from the 802.15.4 standard.

The transmitter’s analog section consists of low-pass filters to smooth out the ‘steps’ in the I and Q signals out of the DACs before driving the upconversion mixers. These filters are VHDL-AMS models and come directly from the behavioral model library. They have a programmable order, cut-off frequency and gain. By default, the order is set to four,

the cut-off frequency is set to 5 MHz and the gain is unity.

White noise sources are also included in the test bench and may be used to add white noise to the signals in order to monitor the impact on the error vector magnitude (EVM). It is also possible to simulate IQ imbalance by using slightly different gains for the I and Q filters, or different conversion gains for the I and Q upconverting mixers. IQ imbalance will distort the constellation diagram and contribute to EVM degradation.

In the RF section of the ZigBee implementation, the upconversion mixers are behavioral models coded in Verilog-AMS. The in-phase and quadrature components of the 2.4 GHz carrier are generated from ideal sources. The PA is a transistor-level (SPICE description) implementation using a 0.25 µm RF process. It is a simple differential structure, so the PA can operate in Class A if properly biased.

The PA can be tailored to operate either in a linear or non-linear regime. Since the modulation is a constant amplitude scheme, non-linear PAs are possible candidates as long as

they do not cause unacceptable EVM or modulation spectrum degradation through adjacent-channel power regrowth (ACPR). The chosen PA can be easily configured to operate in the linear region or in compression. The test bench allows changing the input level and the bias current so that either mode of operation is selected, allowing the examination of possible alternatives.

When used in its linear region, the voltage gain is about 7 dB and the delivered power is 0 dBm. The 802.15.4 standard specifies –3 dBm, but this design is ‘oversized’ to take into account the fact that many reasons for losses are not modeled.

The compression characteristics are obtained with an RF simulator using a sweep statement to sweep the input level. The large signal behavior is obtained from a steady-state analysis (SST). At up to 100 mV input level, the PA shows linear operation and the output phase is independent of the power. Above this input level, compression occurs and the phase is shifted. If the PA is biased in the compression region, this phase shift affects the constellation diagram by rotating the entire diagram. Since the modulation is a constant amplitude scheme, this phase shift does not introduce any measurable distortion.

### Error vector magnitude estimation

The 802.15.4 standard specifies the required performance of RF transmission in terms of EVM. The metric reflects the dispersion of the received or transmitted symbols in the IQ space from their ideal location.

The error vector (dI, dQ) represents the difference between the actually transmitted symbol and the ‘ideal’ one. The ideal location is the location corresponding to a noiseless system with no low-pass filtering. This error vector is potentially different for each transmitted symbol. The EVM metric measures the rms value of the normalized error over a large number of transmitted symbols. For

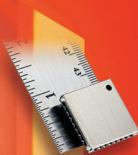
# INSTANT WIRELESS FOR INDUSTRY

## PRICE



Priced as low as \$99 per unit, ConnexLink™ is the easiest, most affordable way to "cut the cables."

## SIZE



Tiny 1x1-inch transceivers put the power of RF into the smallest, most cost-sensitive applications.

## EASE



Embedded RF232™ transparent protocol makes modules drop-in ready for seamless installation.

## RANGE



High transmit power is your key to long range plus reliability. One full watt output power at 900MHz.

**AEROCOMM**

1-800-492-2320  
[www.aerocomm.com](http://www.aerocomm.com)

FLEXIBLE · DURABLE · AFFORDABLE  
2.4GHZ · 900MHZ · 868MHZ  
SERVER/CLIENT · PEER-TO-PEER  
FCC · IC · ETSI      RS232 · RS485

## ZigBee

It is possible to set up the test bench so that conditions are changed at some point; thereby allowing the impact on the EVM to be dynamically monitored.

In the simulation test bench, the EVM is estimated at the output of the analog section and also at the output of the PA.

the 2.4 GHz PHY, the maximum EVM is 35% over 1000 symbols.

To estimate the EVM in the transmitter model, a VHDL model is used that continuously computes an EVM estimate from the last few hundred transmitted symbols. The model assumes that it is an O-QPSK IQ constellation. It computes the four ideal locations as the centers of gravity of the four clusters it processes, as well as the EVM estimate (Figure 3).

As the model processes I and Q information continuously, using a dedicated clock signal to trigger the model at the symbol rate, the EVM estimate also provides continuous information. This data can be displayed vs. time, as a signal waveform, and is more useful than a single final number computed by post-processing of the results following simulation. The EVM estimate initially provides a raw estimation. Then, as the number of symbols processed becomes statistically significant, it gradually stabilizes.

It is possible to set up the test bench so that conditions are changed at some point; thereby allowing the impact on the EVM to be dynamically monitored. In the simulation test bench, the EVM is estimated at the output of the analog section and also at the output of the PA.

### Simulation results

The simulator uses the VHDL, Verilog-AMS and SPICE standard design languages to run a simulation of the transmitter path for the ZigBee 802.15.4 standard and to perform a high-level analysis of the system. Run time for the simulation is five minutes on a 3 GHz Linux system. This is a mixed, fully integrated analog, digital and RF simulation.

All key model parameters such as frequencies, filter orders, gains and IQ imbalance are programmable and can be easily changed for rapid 'what-if' analysis. Figure 4 shows the successful simulation of the transmitter path.

Because the EVM model outputs a time-domain waveform, as opposed to a mere number, its average value must be considered to get an estimate of the EVM. The results shown in Figure 4 correspond to a non-linear PA, as the saturated I and Q waveforms denote. The EVM is around 9%, which is well below the 35% of the specification.

### Generating constellation diagrams

Using the constellation diagram function of the waveform viewer, the constellation diagrams corresponding to RF signals are easily generated. The clusters of points at the PA output are radially compressed. The rotation of the constellation corresponds to the phase shift of the PA.

This phase shift creates a potential problem for the EVM estimator model. Because the model assumes that the IQ data is located in one of the four O-QPSK quadrants, it only looks at the positive or negative sign of the I and Q components for each vector in determining to which cluster the symbol belongs. If an arbitrary phase shift occurs, this assumption is no longer true and the calculation might give erroneous results. To accommodate this phase rotation, the EVM model has an 'angle' parameter that rotates the incoming IQ data by a certain angle to compensate for the phase shift.

### Extracting modulation spectrum

It is possible to extract the modu-

lation spectrum out of the transmitter by setting up a Fast Fourier Transform (FFT) analysis on the complex signal. As an example, Figure 5 shows two modulation spectra obtained with different low-pass filtering configurations. Although both exhibit a familiar ‘sin(x)/x’ shape and show the same 3 MHz bandwidth and zeroes spaced by 1 MHz, the attenuation of the main sidelobes are different due to the impact of the filtering.

The upper spectrum corresponds to fourth-order filtering with 1 MHz cut-off frequency. The spectrum has low sidelobes at -40 dB because the filtering cuts off undesired components and narrows the otherwise relatively wide bandwidth of the modulated signal. The lower spectrum corresponds to second-order filtering and 5 MHz cut-off frequency, which is much less filtering. In this case, the bandwidth is still about 3 MHz but the sidelobes are much higher, approximately -25 dB.

### Summary

Using standard design languages, only five minutes are required to successfully run a high-level analysis of a transmitter path for the ZigBee 802.15.4 standard. All key parameters are programmable and, therefore, may be easily changed for ‘what if’ analysis. Digital encoding, spreading and O-QPSK modulation are performed digitally and simulated with VHDL models. Analog filtering uses VHDL-AMS models, while the RF section is modeled with Verilog-AMS and SPICE transistor-level models. An EVM analysis is performed using a VHDL model. Constellation diagrams and modulation spectra are easily generated. **EWT**

*Cyril Descleves is a product marketing manager in charge of the analog and RF simulation products in the deep submicron division of Mentor Graphics. Prior to joining Mentor, Descleves was the engineering manager at Dolphin Integration. He also managed several projects in digital and mixed-signal IC design, device characterization and CAD methodology. Descleves graduated from the Ecole Supérieure d'Electricité, France, in 1985.*

CompXs

INTEGRATION

## USB ZigBee™ Dongle



Z-Mode™ module enables desktops, notebooks, and PDAs to monitor and control ZigBee devices

For further details visit  
[www.integration.com](http://www.integration.com)

Or call Integration at  
(650) 969 4100

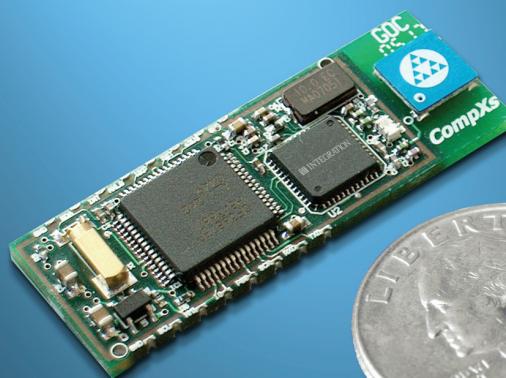
INTEGRATION

- USB 1.1/2.0
- Compact and lightweight
- ZigBee-ready device drivers for OEM integration

CompXs

INTEGRATION

## Serial ZigBee™ Module



Z-Mode™ serial module  
enables any existing  
RS232 device  
to communicate  
over a ZigBee  
network

For further details visit  
[www.integration.com](http://www.integration.com)

Or call Integration at  
(650) 969 4100

INTEGRATION

- Fully integrated ZigBee software
- End-device, router or coordinator
- Enhanced “AT” commands
- 868/915MHz and 2.4GHz