

# DCSYNTH: Guided Reactive Synthesis with Soft Requirements for Robust Controller and Shield Synthesis

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**Abstract.** DCSYNTH is a tool for the synthesis of controllers from safety and bounded liveness requirements given in interval temporal logic QDDC. It investigates the role of soft requirements (with priorities) in obtaining high quality controllers. A QDDC formula specifies past time properties. In DCSYNTH synthesis, hard requirements must be invariantly satisfied whereas soft requirements may be satisfied "as much as possible" in a best effort manner by the controller. Soft requirements provide an invaluable ability to guide the controller synthesis. In the paper, using DCSYNTH, we show the application of soft requirements in obtaining robust controllers with various specifiable notions of robustness. We also show the use of soft requirements to specify and synthesize efficient runtime enforcement shields which can correct burst errors. Finally, we discuss the use of soft requirements in improving the latency of controlled system.

**Keywords:** Discrete Duration Calculus (QDDC), Reactive Controller Synthesis, Soft Requirements, Guided Synthesis, Robustness, Shield Synthesis, Latency Measurement.

## 1 Introduction

A temporal logic formula implicitly specifies the allowed sequence of inputs and outputs. In reactive synthesis the aim is to construct a controller (say a Mealy Machine) which explicitly computes the value of the output sequence for any given input sequence, in an online fashion, such that the requirement is met. Reactive synthesis is typically a much harder problem than the monitor synthesis. Considerable research has been carried out on the reactive synthesis problem and there are several tools which implement and experiment with reactive synthesis [6].

During development systems are often under specified and several different controllers with distinct behaviors may all meet the specification. In this case “guidance” must be provided to the synthesizer to choose amongst them. A critical parameter in acceptance of automatic synthesis technique is the *quality* of the synthesized controller [1, 2]. Thus, just correct-by-construction synthesis is not sufficient.

Requirements are typically structured as a set of assumptions  $A$  and a set of commitments (guarantees)  $C$ . Much of the research has addressed “Be-Correct” goal [2] for synthesis which states that if assumptions hold for throughout the behavior then commitment holds for the behavior. For safety formulas this would take the form  $G A \Rightarrow G C$ .

**Robustness** pertains to the ability of the controller to meet commitments even when (some) environmental assumptions are violated, and the ability of the controller to recover from transient environmental errors. Laying down such criteria, Bloem et. al. have defined “don’t-be-lazy” and “never-give-up” as desirable synthesis goals [2]. Other criteria include various notions of resilience [5].

A related problem is synthesis of run time enforcement **shield** [3, 5, 13, 14] for critical correctness properties. The diagram 4 depicts the use of shield, which receives both input  $I$  and output  $O$  from a (occasionally incorrect) controller. The aim of the shield is to generate modified output  $O'$  which always meets the requirement  $Req(I, O')$  even if system output intermittently fails to meet  $Req(I, O)$ . Moreover,  $O'$  must deviate from  $O$  “as little as possible” [3]. Bloem et. al. proposed a notion  $k$ -shield for “as little as possible” whereas Wu et. al. [13] proposed an alternative notion of “safety shield” which tolerates burst errors.

This paper describes a tool DCSYNTH which allows synthesis of controllers from safety and bounded liveness requirements given in interval temporal logic **QDDC**. The paper mainly investigates the role of **soft requirements** (with priorities) in obtaining high quality controllers. A QDDC formula specifies past time properties, and it holds at a position in behavior if the past satisfies the property. Its (bounded) counting and regular expression like primitives allow complex quantitative properties to be specified elegantly. In DCSYNTH synthesis, hard requirements must be invariantly satisfied whereas soft requirements may be satisfied “as much as possible” in a best effort manner by the controller. In DCSYNTH specification, the soft requirements (which are QDDC formulas) can be given weights and the tool selects from all permissible outputs which meet the hard requirements, the one which satisfies a maximal subset of soft requirements, in a “locally optimal fashion”. We present the case studies

of bus arbiter and mine pump specification to illustrate the use of soft requirements in synthesis specification.

Soft requirements provide a powerful and practically useful ability to guide the controller synthesis. In the paper, we show the application of soft requirements in obtaining robust controllers with various *specifiable* notions of robustness. We also show the use of soft requirements to specify and synthesize efficient run time enforcement shields which can correct burst errors. Finally, we discuss the use of soft requirements in improving the **latency** of controlled system. The main contributions of this paper are as follows:

- We present a tool DCSYNTH for synthesis of controllers from QDDC requirements. This extends the past work [10] on model checking interval temporal logic with synthesis abilities.
- The tool DCSYNTH allows guided synthesis of controllers based on **soft requirements** which are met “as much as possible” in a locally optimal fashion. *To our knowledge DCSYNTH is amongst the first reactive synthesis tool to support soft requirement guided synthesis.*
- We show application of mixture of hard and soft requirements to *specify* various notions of robustness. This includes “never-give-up” and “don’t-be-lazy” criteria of Bloem et. al. [2] as well as  $k, b$ -resilience criterion of Ehler et. al. [5]. DCSYNTH is able to automatically synthesize robust controller from such specification. We give experimental results to evaluate the applicability of our tool for such robust synthesis.
- We show application of hard and soft requirements to *specify* shields. We show how variants of shields of Bloem et. al. and Wu et. al. can be specified and automatically synthesized. We give detailed experimental results and comparison with past work to illustrate that DCSYNTH is able to synthesize very compact shields which tolerate burst errors.
- Soft goals impact the latency of the controller. An associated tool, CTLDC, allows measurement of worst case latencies using symbolic techniques for finding longest and shortest paths [11]. We give experimental results to show how soft requirements indirectly impact the latencies.

The remainder of this paper is organized as follows. Section 2 gives a motivating example of synchronous bus arbiter with hard and soft requirements. Logic QDDC as well as DCSYNTH syntax are introduced in Section 3. Section 4 gives the guided synthesis method from given DCSYNTH

specification. Experimental results in synthesizing controllers using the DCSYNTH tool are also reported. Section 5 deals with robustness and Section 6 deals with shield synthesis. Both these include experimental results. We conclude with Section 7 on experiments examining impact of soft requirements on controller latencies. The tool is available for download from <http://www.tcs.tifr.res.in/~pandya/dcsynth/dcsynth.html>. The input files for all the experiments reported in this paper as well as corresponding outputs of the tool DCSYNTH are also available there for examination.

## 2 Motivating Example

In this section we illustrate the main advantage of guided reactive synthesis with *soft requirement* with an example of synchronous bus arbiter.

An  $n$ -cell synchronous bus arbiter with  $req_i$  as inputs and  $ack_i$  as corresponding outputs (where  $1 \leq i \leq n$ ), is a circuit that arbitrates between a subset of requests at each cycle by setting one of the acknowledgments *true*. Hard requirements include the following three invariant properties.

$$\begin{aligned} Mutex &= [[ \bigwedge_{i \neq j} \neg(ack_i \wedge ack_j) ]] \\ NoLoss &= [[ (\bigvee_i req_i) \Rightarrow (\bigvee_j ack_j) ]] \\ NoSpurious &= [[ \bigwedge_i (ack_i \Rightarrow req_i) ]] \\ ARBINV &= Mutex \wedge NoLoss \wedge NoSpurious \end{aligned} \tag{1}$$

In QDDC  $[[P]]$  denotes that proposition  $P$  is invariantly *true*. Thus, *Mutex* gives mutual exclusion of acknowledgments. *NoLoss* states that if there is at least one request then there must be an acknowledgment. *NoSpurious* states that acknowledgment is only given to a requesting cell.

In literature GR(1) synthesis has been used to specify fairness between cells of arbiter [4]. We consider here other variants with concrete bounds on the arbiter response.

- We can specify response time of  $k$  cycles as a bounded liveness property: let  $Resp(req, ack, k)$  denote that if request has been high for last  $k$  cycles there must have been at least one acknowledgment in the last  $k$  cycles (next section gives the QDDC formula for this). Let  $ArbResp(n, k)$  state that for each cell  $i$  and for all observation intervals the formula  $Resp(req_i, ack_i, k)$  holds.

$$\begin{aligned} ArbResp(n, k) &= \bigwedge_{1 \leq i \leq n} [[(Resp(req_i, ack_i, k))]] \\ ARBHARD(n, k) &= ARBINV \wedge ArbResp(n, k) \end{aligned} \tag{2}$$

- Consider the following specification with only hard requirements and no soft requirements,

$$Arb^{hard}(n, k) = (ARBHARD, \langle - \rangle) \quad (3)$$

DCSYNTH can synthesize a controller say  $ArbCntrl^{hard}(n, k)$  for given values of  $n, k$ .

- Moreover, we can also include *soft requirements* giving priority to cells, e.g.  $(ARBHARD(6, 6), \langle ack_6, ack_2 \rangle)$  which gives acknowledgment  $ack_6$  as first preference and  $ack_2$  as second preference as far as these don't conflict with the hard response requirements. Table. 1 gives experimental results for synthesis with several such soft requirements.
- If we use  $ARBHARD(6, 2)$  in place of  $ARBHARD(6, 6)$  the specification becomes unrealizable as expected (as we cannot guarantee response within two cycles for all 6 cells). The tool reports this with a diagnostic counter-strategy.
- However, we can specify the requirements of response in 2 cycles as *soft requirements with priority* as  $Arb^{soft}(6, 2)$  where

$$Arb^{soft}(n, k) = (ARBINV, \langle Resp(req_6, ack_6, 2), \dots, Resp(req_1, ack_1, 2) \rangle) \quad (4)$$

Using DCSYNTH we get a controller called  $ArbCntrl^{soft}(6, 2)$  which “tries” to give every cell acknowledgment within 2 cycles as far as possible with highest priority given to cell 6, followed by cell 5, and so on. Table. 1 gives the time taken compute this controller. Table. 5 gives a detailed account of the robust behavior of this complex arbiter. The latency measurement of  $ArbCntrl^{soft}(6, 2)$  using tool CTLDC shows that the worst case response time for cell 6 is 2 cycles, for cell 5 is 3 cycles and for all other cells it is  $\infty$ .

- Consider an  $Arb^{hard}(n, k)$  like arbiter working under the assumption  $Assume(n, i)$  which states that in current cycle at most  $i$  requests are true simultaneously. Consider the arbiter specification with no soft requirement as follows.

$$Arb_{assume}^{hard}(n, k, i) = ((Pref(Assume(n, i)) \Rightarrow ARBHARD(n, k)), \langle - \rangle) \quad (5)$$

Synthesis of various *robust* arbiters which function even in presence of *intermittent violation* of the assumption is reported in Table. 3.

- Section 6 gives experimental results in specifying and synthesizing run time enforcement shields from diverse specifications (see Table. 4).

Above examples show that DCSYNTH can fruitfully use soft requirements to synthesize better performing, more robust controllers as well as shields.

### 3 QDDC and DCSynth Specification

We now give the QDDC formula  $Resp(req, ack, k)$  for the response time of the arbiter. We refer the reader to §A in Appendix for a discussion on the logic QDDC [10].

We define  $Resp(req, ack, k) = (\text{true}^{\sim}([\text{req}]] \&\&(\text{slen}=k-1)) \Rightarrow (\text{true}^{\sim}(\text{slen}=k-1 \&\&(\text{true}^{\sim}\langle ack \rangle^{\sim}\text{true})))$ . In QDDC the only temporal modality is the *chop operator* ( $\sim$ ) and is interpreted over a word  $\sigma$  and a closed interval  $[i, j]$ ,  $0 \leq i \leq j < \text{len}(\sigma)$ , as follows:  $\sigma, [i, j] \models D_1 \hat{\sim} D_2$  iff  $\exists k : i \leq k \leq j : \sigma, [i, k] \models D_1$  and  $\sigma, [k, j] \models D_2$ . For a propositional formula  $p$ ,  $\sigma, [i, j] \models \langle p \rangle$  iff  $i = j$  and  $p$  holds at position  $i$  in  $\sigma$ . Finally  $\sigma, i \models D$  iff  $\sigma, [0, i] \models D$ .

The term  $\text{slen} = k$  holds for an interval  $[i, j]$  if  $j - i = k$  and *scount*  $p$ , where  $p$  is a propositional formula, counts the number of positions in the interval where  $p$  holds. Thus, as *true* holds for any word and any interval,  $Resp$  states that if  $req$  holds throughout the last  $k$  positions in the word then at least at one of the last  $k$  positions  $ack$  should hold. With  $\square$  being *for all sub-intervals* operator, the formula  $ArbResp(n, k)$  says that  $Resp(req, ack, k)$  must be *true* for all intervals and for all the cells from 1 to  $n$ .

The tool DCSYNTH takes a *DCSYNTH spec* as input and outputs a controller. Formally, a *DCSYNTH spec* is a tuple

$$S = (I, O, D^h, \bigwedge_{i=1}^{i=k} (w_i \Leftrightarrow D_i^s), \langle P_1, \dots, P_l \rangle)$$

where  $I$  and  $O$  are *input* and *output* variables of the controller, respectively. The QDDC formula  $D^h$  which is over  $I \cup O$ , specifies *hard requirement* on the synthesized controller, i. e. every execution of a controller must satisfy  $D^h$  invariantly. We have a list of indicator definitions  $D_1, \dots, D_k$  where each  $D_i^s$  specifies a *soft requirement* over  $I \cup O$ . Each  $D_i$  is associated with the *indicator variable*  $w_i$  which witnesses whether  $D_i^s$  holds for the execution so far, i. e.  $\sigma, i \models w_i$  iff  $\sigma, [0, i] \models D_i^s$ . Let  $W = \{w_i \mid 1 \leq i \leq k\}$ . The *soft requirements* are specified as lexicographically ordered list of propositions  $\langle P_1, \dots, P_l \rangle$  where each  $P_i$  is a propositional formula over  $I \cup O \cup W$ . Each  $P_i$  represents a soft requirement with priority higher than all  $P_j$ 's,  $1 \leq i < j \leq l$ .

*Example 1.* A DCSYNTH spec for an  $n$  cell arbiter with soft requirement of  $k$  cycle response  $ArbResp(n, k)$  for all the cells is as follows: let  $I =$

$\{req_i \mid 1 \leq i \leq n\}$  and  $O = \{ack_i \mid 1 \leq i \leq n\}$ . Let  $L = \langle w_6, w_5, \dots, w_1 \rangle$  which gives the higher numbered cell the higher priority. Then

$$Arb^{prio}(n, k) = (I, O, ARBINV, \bigwedge_{i=1}^{i=n} (w_i \Leftrightarrow Resp(req_i, ack_i, k)), L).$$

## 4 Guided Reactive Synthesis Algorithm

Given  $S = (I, O, D^h, \bigwedge_{i=1}^{i=k} (w_i \Leftrightarrow D_i^s), \langle P_1, \dots, P_l \rangle)$ , a DCSynth spec, we synthesize a controller as below.

- The formula  $D^{Ind} = pref(\bigwedge_{i=1}^{i=k} (\mathbf{true} \hat{<w_i>=>D_i^s}))$  states that at every point in execution, the value of  $w_i$  equals the truth-value of  $D_i^s$ . We construct a language equivalent symbolic DFA, called  $A^{Hard+Ind}$ , for the formula  $D^{hard} \wedge D^{Ind}$  using tools DCVALID and MONA. From [10], it is known that for every QDDC formula  $D$ , we can effectively construct a equivalent finite state automaton  $A(D)$ , such that a word is accepted by  $A(D)$  iff it satisfies formula  $D$ . Tool DCVALID implements this procedure.
- A *safety monitor automaton*  $A^{mon}$  is obtained by computing the prefix closure of  $A^{Hard+Ind}$ . This automaton has the alphabet  $2^{I \cup O \cup W}$ . The automaton is reduced to its minimal deterministic form. This automaton forms the arena on which further synthesis is carried out.
- The *Maximally Permissive Non deterministic Controller* (MPNC) is computed from the safety automaton using standard safety synthesis algorithm. This algorithm iteratively removes those states from which there exists an input combination for which all output combinations lead to bad states. The resulting automaton is again represented as a symbolic automaton  $A^{mpnc}$ . If the initial state gets pruned in construction, the specification is unrealizable. A counter-strategy in tree form is displayed as explanation of unrealizability.
- Note that in  $A^{mpnc}$  each edge is labelled by a bit vector giving truth values of variables  $I \cup O \cup W$ . The value of witness variable  $w_i \in W$  specifies whether QDDC formula  $D_i^s$  holds for all behaviours leading to this transition.
- For each state  $s$  and each input combination  $ip \in 2^I$ , we select output cum witness variable combination  $op \in 2^{O \cup W}$  such that  $\delta(s, ip \cup op)$  is a valid transition of MPNC and  $val_{ip \cup op}(\langle P_1, \dots, P_l \rangle)$  is lexicographically maximal amongst all such  $op$ . Here,  $val_{ip \cup op}(\langle P_1, \dots, P_l \rangle)$  is  $l$ -bit vector with  $i$ -th bit representing truth (1 or 0) of  $P_i$  under  $ip \cup op$ . If there are more than one choice of  $op$  giving the same maximal value,

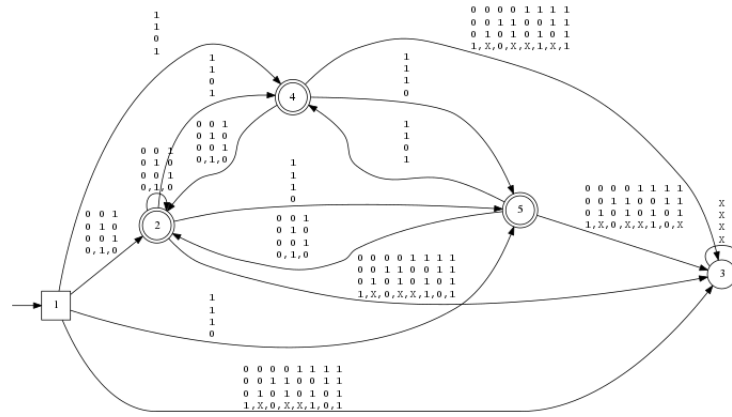
we choose one arbitrarily. This gives the *Locally Optimal Deterministic Controller* (LODC) which satisfies the lexicographically maximal subset of soft requirements at each step. This greedy strategy does not guarantee global optimality.

- The LODC can then be encoded as controller in any target language. We provide the encoding of LODC to LUSTRE/SCADE or NuSMV, which allows us to do simulation and model checking on the generated controller.

*Example 2.* Synthesis of 2 Cell Arbiter with Soft Requirements giving high priority to lower numbered request. Fig. 1 gives the safety monitor automaton for 2-cell arbiter for following specification

$$(\langle req_1, req_2 \rangle, \langle ack_1, ack_2 \rangle, ARBINV \wedge ArbResp(2, 2), \langle \rangle, \langle ack_1, ack_2 \rangle).$$

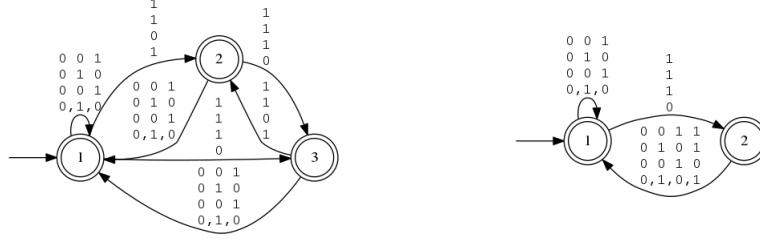
Each transition is labeled by 4 bit vector giving values of  $req_1, req_2, ack_1, ack_2$ . Fig. 2(a) gives the MPNC automaton for the 2-cell arbiter computed from the safety monitor automaton of Fig. 1. In the example, the soft requirements are  $\langle ack_1, ack_2 \rangle$  which give  $ack_1$  priority over  $ack_2$ . We obtain the pruned LODC controller automaton of Fig. 2(b) from the MPNC of Fig. 2(a). Note that we minimize the automaton at each step.



**Fig. 1.** Safety Monitor Automaton: 2 Cell Arbiter

*Tool Implementation* Internally, the monitor automaton, MPNC and LODC are all stored as symbolic DFA. The transition table of the DFA is represented as MTBDD using the DFA library of tool MONA [8]. Internal data structures and algorithms can be found in the full version of the paper (see Appendix B).





**Fig. 2.** (a) *MPNC: 2 Cell Arbiter* (b) *LODC: 2 Cell Arbiter*

#### 4.1 Experimental Results

Several case studies for synthesis have been carried out using DCSYNTH. Table. 1 enlists the results of two of the case studies: **(a)**: controllers for bus arbiter in §2 with various soft and hard requirements, and **(b)**: a minepump controller for the specification *MINEPUMP* (cf. Appendix. C.1 for details). The controller operates a pump to get rid of water based on water level and methane presence (which prevents pump from being used). Soft requirements impact the quality of the pump controller. For example, for the soft requirement `!PumpOn` the controller will try to keep pump *off* as much as possible. On the other hand, the soft requirement `PumpOn` aggressively gets rid of water by keeping the pump *on* whenever possible. The analysis of worst case time for the controllers to get rid of water with different soft requirements is given in §7.

**Table 1.** DCSYNTH Controller Synthesis with Soft Requirements.

Hard Requirement	Soft Requirement	Controller Generation		
		states	time (Sec)	Memory (MB)
<i>ARBHARD</i> (4, 4)	<code>ack4 &gt;&gt; ... &gt;&gt; ack1</code>	50	0.014	3.3
<i>ARBHARD</i> (5, 5)	<code>ack5 &gt;&gt; ... &gt;&gt; ack1</code>	432	0.33	22.4
<i>ARBHARD</i> (6, 6)	<code>ack6 &gt;&gt; ... &gt;&gt; ack1</code>	4802	14.8	334.5
<i>ARBINV</i> ( $1 \leq i, j \leq 6$ )	<code>Resp(req6,ack6,2) &gt;&gt; ... &gt;&gt; Resp(req1,ack1,2)</code>	62	1.05	9.8
<i>ARBINV</i> ( $1 \leq i, j \leq 5$ )	<code>Resp(req5,ack5,3) &gt;&gt; ... &gt;&gt; Resp(req1,ack1,3)</code>	511	5.4	32.4
<i>MINEPUMP</i> (MPV1)	<code>PumpOn &gt;&gt; !Alarm</code>	31	0.07	9.1
<i>MINEPUMP</i> (MPV2)	<code>(CH4<sub>Last2Cyc</sub> =&gt; !PumpOn) &gt;&gt; PumpOn</code>	34	0.09	8.9
<i>MINEPUMP</i> (MPV3)	<code>!PumpOn &gt;&gt; !Alarm</code>	83	0.04	9.1

## 5 Robustness

We consider various notions of robustness. Table. 2 summarizes the robustness that we consider along with hard and soft requirements to obtain robust controllers.

- **Be-Correct** If assumption has held invariantly so far then commitment must hold now.

- **Be-Currently-Correct** If assumption holds intermittently, the commitment must hold whenever assumption holds.
- **Degraded-Performance** Let  $Ad \subseteq A$  and  $Cd \subseteq C$ , where  $Ad, Cd$  denote reduced set of assumptions and commitments which specify degraded behaviour of system when fewer assumptions hold.
- **Never-Give-Up** In addition to Be-Correct, all the commitments are asserted as soft requirements. This makes the controller synthesizer attempt to make them true even when assumptions do not hold, and for as many inputs as possible.
- **Greedy** Here commitments are given as soft goals ignoring the assumptions. The synthesis algorithm tries to make as many commitments true as possible at each step in a greedy fashion.

Resilient synthesis requires synthesis of controller which works under weaker assumptions than Be-Correct notion in order to tolerate errors in assumptions. For example, Be-Currently-Correct requires commitment to hold at now if assumption holds now irrespective of whether it has held in past. Several other notions of resilience are given below. A notion of  $k, b$ -resilience was proposed by Ehler and Topcu [5], and further adapted by Bloem as  $k$ -robustness [3].

**Table 2.** Robust synthesis notions and their specifications.

In the table  $A$  denotes conjunction of assumptions and  $C$  denotes conjunction of commitments. Thus,  $!A$  denotes violation of at least one assumption.

Robustness Criterion	Hard Requirement	Soft Requirement
Be-Correct( $A, C$ )	$G(\text{Pref}(A) \Rightarrow C)$	
Be-Currently-Correct( $A, C$ )	$G(A \Rightarrow C)$	
Degraded-Performance( $A, C, Ad, Cd$ )	$G((A \Rightarrow C) \ \&\& \ (Ad \Rightarrow Cd))$	
Never-Give-Up( $A, C$ )	$G(A \Rightarrow C)$	$C$
Greedy( $C$ )		$C$
$k$ -Bounded( $A, C, k$ )	$G((\text{scount } !A < k) \Rightarrow C)$	
$k, b$ -Resilient( $A, C, k, b$ )	$G(\text{KBREZ}(A) \Rightarrow C)$	
$k, b$ -Variant( $A, C, k, b$ )	$G([\ ]((\text{slen} = b \ \&\& \ \text{scount } !A \leq k) \Rightarrow C))$	

where  $\text{KBREZ}(A) = !(true^((\text{scount } !A \geq k) \ \&\& \ [\ ]([A] \Rightarrow \text{slen} < b)) \wedge true)$

- **$k$ -Bounded** If in past assumptions have been violated at most  $k$  times so far then commitment must be met.
- **$k, b$ -Resilient** A subinterval where assumption is continuously true for  $b$  or more cycles is called a recovery period. Formula  $\text{KBREZ}(A)$  in Table. 2 states that between any two recovery periods, the maximum

number of assumption violations is at most  $k$ . A controller which guarantees commitments  $C$  at every point where past satisfies  $\text{KBREZ}(\mathbf{A})$  is called  $k, b$ -resilient (see [5]).

- **$k, b$ -Variant** If in past in any period of length  $b$  the assumption has been violated at most  $k$  times then the commitment must hold.

Note that criterion such as Never-Give-Up can be combined with Resilient synthesis. Moreover, designer may selectively apply these criteria to specific assumptions and commitments. DCSYNTH permits full flexibility in making such choices. Table. 3 gives the synthesis of arbiter specifications under various notions of robustness in DCSYNTH for the assumptions  $\text{Assume}(n, i)$  and commitments  $\text{ARBHARD}(n, k)$  for the specification  $\text{Arb}_{\text{assume}}^{\text{hard}}(n, k, i)$  in Equation. 5.

**Table 3.** Synthesis of Robust Arbiters in DCSynth

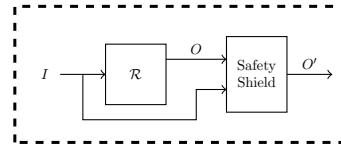
Specification		LODC	
Robustness Specification	Priorities of Soft Requirements	States	Time
Be-Correct( $\text{Assume}(4, 2), \text{ARBHARD}(4, 2)$ )	-	6	0.02
Be-Currently-Correct( $\text{Assume}(4, 2), \text{ARBHARD}(4, 2)$ )	-	Unrealizable	
Never-Give-Up( $\text{Assume}(4, 2), \text{ARBHARD}(4, 2)$ )	$(\text{ARBINV} \gg \text{Resp}(\text{req}_1, \text{ack}_1, 2) \gg \dots \gg \text{Resp}(\text{req}_4, \text{ack}_4, 2))$	15	0.73
Greedy( $\text{ARBHARD}(4, 2)$ )	$(\text{ARBINV} \gg \text{Resp}(\text{req}_1, \text{ack}_1, 2) \dots \gg \text{Resp}(\text{req}_4, \text{ack}_4, 2))$	15	0.07
$k$ -Bounded( $\text{Assume}(4, 2), \text{ARBHARD}(4, 3), 2$ )	-	29	0.06
$k, b$ -Resilient( $\text{Assume}(4, 2), \text{ARBHARD}(4, 3), 2, 3$ )	-	39	0.09
$k, b$ -Variant( $\text{Assume}(4, 2), \text{ARBHARD}(4, 3), 2, 3$ )	-	27	0.22

The simulation of controller produced for Never-Give-Up Strategy is given in Figure 3. The assumptions starts violating after step 15, where more than request are true simultaneously, but the controller tries to meet as many requirements as possible.

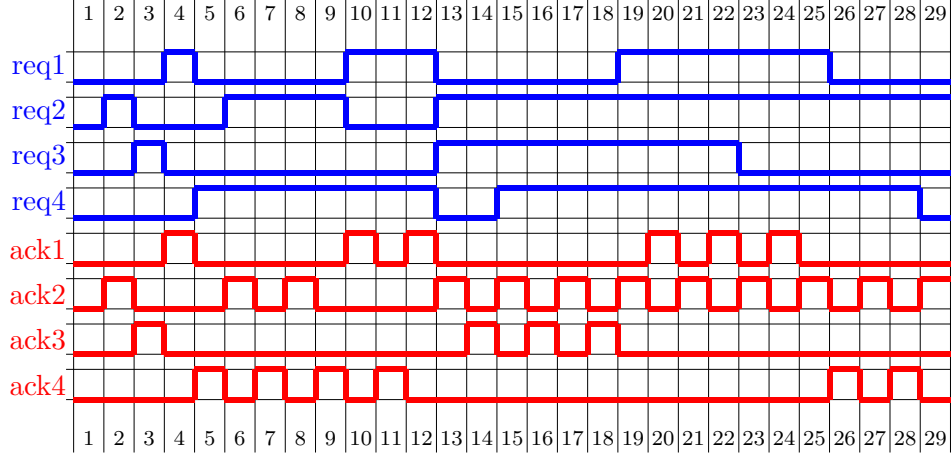
## 6 Shield Synthesis

A *safety shield* is a run time enforcer that can be attached to a reactive system design  $\mathcal{R}$  to detect the property violations by the design and correct them run time [3, 13]. Fig. 4 gives the schematic of a safety shield for  $\mathcal{R}$ .

We assume the definitions of a reactive system design and their serial composition



**Fig. 4.** Safety shield.



**Fig. 3.** Example Simulation of Robust Controller for Never-Give-Up

(cf. [13] for details). Let  $D$  be a QDDC formula over  $I \cup O$ . Let  $O = \{o_1, \dots, o_n\} \subseteq \Sigma$  and let  $O' = \{o'_1, \dots, o'_n\}$ . Then we define  $D[O/O']$  to be the formula  $D'$  obtained by replacing every occurrence of  $o_i$  in  $D$  by  $o'_i$  for all  $1 \leq i \leq n$ . We can now define a safety shield.

**Definition 1 (Safety shield).** [3, 13] Let  $\mathcal{R}$  be a reactive system design and let  $D$  be a safety specification, both over  $(I, O)$ . Then a safety shield for  $\mathcal{R}$  and  $D$  is a reactive system  $\mathcal{S}$  over  $(I, O')$  satisfying:

- $\mathcal{R} \circ \mathcal{S} \models D[O/O']$ .
- For all input traces  $\alpha = \alpha_0 \alpha_1 \dots$   $(\mathcal{R} \circ \mathcal{S})(\alpha_i)$  “deviates” from  $\mathcal{R}(\alpha_i)$  as seldom as possible.

The word “deviates” assumes different meaning in the literature. For example, in [3] Bloem et. al. proposed *K-shield* which can disagree with the design for at most  $K$  consecutive steps provided the design recovers immediately after an error and does not violate the specification for next  $K$  cycles. Since the shield is allowed a window of  $K$  cycles to deviate from the design output in the event of an output error by the design it is not suited to handle burst errors. In [13] Wu et. al. proposed a *burst error shield* which is resilient to burst error and matches the design output whenever it meets the specification. However, this strategy of matching the design output until a violation occurs makes the synthesis algorithm “non-conservative” in the sense that it may fail to generate a shield even if specification is realizable.

To overcome these issues we propose *conservative shield synthesis*. The conservative shield synthesis differs from  $K$ -shield synthesis in two key respects: it does not impose any restriction on the design output and it can handle burst errors. It also differs from Wu et. al. as, unlike them, we will always synthesize a shield whenever the specification is realizable.

Shield synthesis criteria can be specified using hard and soft requirements. DCSYNTH can then synthesize the desired shield. We give examples of variants of  $K$ -shield and Burst error shield, and call the “conservative”.

- Conservative  $K$ -shield.
  - Input:  $I \cup O$ . Output:  $O'$
  - Hard requirement:  $\text{REQ}[O/O'] \&\& [] ([[ \vee_{o \in O} (o \neq o') ]]) \Rightarrow \text{slen} < k$ .
  - Soft requirement: None
- Conservative burst error shield.
  - Input:  $I \cup O$ . Output:  $O'$
  - Hard requirement:  $\text{REQ}[O/O']$
  - Soft requirement:  $\bigwedge_{o \in O} (\text{true} \wedge \langle o=o' \rangle)$  with all of formulas assigned same priority.

We emphasize the importance soft requirements here, it forces a conservative burst error shield to try and match the design output as often as possible. This is because when all the soft requirements are assigned same priority DCSYNTH will try to synthesize a controller selecting an output which meets the hard requirement as well as a maximal set of soft requirements at every step.

We have rerun the experiments in [13] in our framework, and the results are as tabulated in Table. 4. For the sake of comparison we use the input files of Wu et. al. [12] as inputs to DCSYNTH<sup>1</sup>. As the table suggests, in most of the cases the shield that we synthesize compares favorably with the corresponding shield synthesized in [3] and [13] both in terms of size and time taken for the synthesis. For instance, for the guarantee AMBA G5+6+9e64+10 our tool synthesize a shield significantly faster and with smaller no. of states than the existing tools [3, 13].

## 7 Quantitative Latency Measurement

Soft requirements are often used as directives to the synthesis algorithm which impact the “latency” of the controller. We give a notation to allow

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<sup>1</sup> Automata as formula

**Table 4.** Comparison of K-Shield and Burst error shield with Conservative safety shield. Columns under *K*-shield and Burst error shield are taken from Wu et. al. [13] and reproduced here for comparison.

Guarantees	Monitor states	K-Shield		Burst error shield		Conservative burst error shield	
		states	time	states	time	states	time
Toyota Powertrain	23	38	0.2	38	0.3	9	0.7
Traffic light	4	7	0.1	7	0.2	4	0.007
$F_{64}p$	67	67	0.7	67	0.5	67	0.002
$F_{256}p$	259	259	46.9	259	10.5	259	0.01
$F_{512}p$	515	515	509.1	515	54.4	515	0.07
$G(\neg q) \vee F_{64}(q \wedge F_{64}p)$	67	67	0.8	67	0.6	67	0.007
$G(\neg q) \vee F_{256}(q \wedge F_{256}p)$	259	259	46.2	259	10.7	259	0.04
$G(\neg q) \vee F_{512}(q \wedge F_{512}p)$	515	515	571.7	515	54.5	515	0.1
$G(q \wedge \neg r \rightarrow (\neg r \cup_4 (p \wedge \neg r)))$	6	15	0.1	145	0.1	6	0.004
$G(q \wedge \neg r \rightarrow (\neg r \cup_8 (p \wedge \neg r)))$	10	109	0.2	5519	4.5	10	0.005
$G(q \wedge \neg r \rightarrow (\neg r \cup_{12} (p \wedge \neg r)))$	14	753	6.3	27338	1414.5	14	0.006
AMBA G1+2+3	12	22	0.1	22	0.1	7	0.008
AMBA G1+2+4	8	61	6.3	78	2.2	8	0.6
AMBA G1+3+4	15	231	55.6	640	97.6	14	0.4
AMBA G1+2+3+5	18	370	191.8	1405	61.8	17	0.05
AMBA G1+2+4+5	12	101	3992.9	253	472.9	12	3.2
AMBA G4+5+6	26	252	117.9	205	26.4	18	0.6
AMBA G5+6+10	31	329	9.8	396	31.4	27	2.6
AMBA G5+6+9e4+10	50	455	17.6	804	42.1	46	5.2
AMBA G5+6+9e8+10	68	739	34.9	1349	86.8	64	7.6
AMBA G5+6+9e16+10	104	1293	74.7	2420	189.7	100	12.5
AMBA G5+6+9e64+10	320	4648	1080.8	9174	2182.5	316	40.9
AMBA G8+9e4+10	48	204	7.0	254	6.1	48	0.3
AMBA G8+9e8+10	84	422	22.5	685	33.7	84	0.5
AMBA G8+9e16+10	156	830	83.7	1736	103.1	156	0.9
AMBA G8+9e64+10	588	3278	2274.2	7859	2271.5	588	3.3

users to specify what is *latency*. Model checking technique, implemented in tool CTLDC [11], can then measure the worst case latency.

For latency measurement, user must specify a QDDC formula  $D^p$  characterizing execution fragments of interest. For example the QDDC formula  $D^p = [[\text{req}]] \&\&(\text{scount ack} < 3)$  specifies fragments of execution with request continuously *true* but with less than 3 acknowledgments (exact syntax is explained in §3). The latency goal  $MAXLEN(D^p, M)$  computes  $\sup\{e - b \mid \rho[b, e] \models D^p, \rho \in Exec(M)\}$ , i. e. it computes the length of the longest interval satisfying  $D^p$  within the executions of  $M$ . For example  $MAXLEN(D^p, Arb)$  specifies the worst case response time of the arbiter *Arb* to get three acknowledgments. Tool CTLDC, which like DCSYNTH is member of DCTOOLS suite of tools, provides efficient computation of  $MAXLEN$  by symbolic search for longest paths as formulated in [11].

Table. 5 gives worst case latency measurements carried out using tool CTLDC for various controllers synthesized using DCSYNTH. The results illustrate the impact of soft goals on controller behaviour as well as controller latency under various scenarios. For example,  $Arb^{soft}(6, 2)$  “tries” to give acknowledgement within 2 cycles with higher priority assigned to higher numbered cell (see the description in §2). Note that response time

is *one* more than that in the column *Computed Response* in the Table. The worst case latency measurement shows that **req6** has response time of 1 cycle whereas **req5** has response time of 2 cycles. For all other cells the response time is  $\infty$  since cells 6 and 5 can consume all the cycles. Note that when **req6** is absent throughout the response time of cell 4 changes from  $\infty$  to 3 cycles as shown in the 4<sup>th</sup> row of the Table. 5. This points to the *robustness* of the synthesized controller.

**Table 5.** Worst Case Latency Analysis using CTLDC using MAXLEN(Response Formula) computation

Sr.No	Example	Response Formula	Computed Response
1	$Arb^{soft}(6, 2)$	$(([req6] \&\& ([!ack6])))$	1
2	$Arb^{soft}(6, 2)$	$(([req5] \&\& ([!ack5])))$	2
3	$Arb^{soft}(6, 2)$ for $1 \leq i \leq 4$	$(([req_i] \&\& ([!ack_i])))$	$\infty$ $\infty$
4	$Arb^{soft}(6, 2)$	$(([req4 \&\& !req6] \&\& ([!ack4])))$	2
5	$Arb^{soft}(5, 3)$	$(([req5] \&\& ([!ack5])))$	2
6	$Arb^{soft}(5, 3)$	$(([req4] \&\& ([!ack4])))$	3
7	$Arb^{soft}(5, 3)$	$(([req3] \&\& ([!ack3])))$	4
8	MINEPUMP(MPV1)	$[[AssumptionOk \&\& HH2O]]$	4
9	MINEPUMP(MPV2)	$[[AssumptionOk \&\& HH2O]]$	7
10	MINEPUMP(MPV3)	$[[AssumptionOk \&\& HH2O]]$	8

For the *MINEPUMP* case study rows 8,9,10 give the maximum amount of time (in cycles) for which the water level can remain high (indicated by the variable *HH2O*) without violating the assumptions (indicated by *AssumptionOk*). Here, *MINEPUMP*(*req*) denotes *MINEPUMP* specification with soft requirement *req* as given in Appendix . For example, soft requirement MPV3 is **!PumpOn** which tries to keep pump *off* as much as possible where as soft requirement MPV1 is **PumpOn** which tries to keep pump *on* as much as possible. As a result *MINEPUMP*(MPV1) gets rid of water in 4 cycles compared to 8 cycles for *MINEPUMP*(MPV3).

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## A Logic QDDC

Let  $\Sigma$  be a finite non empty set of propositional variables. A *word*  $\sigma$  over  $\Sigma$  is a finite sequence of the form  $P_0 \cdots P_n$  where  $P_i \subseteq \Sigma$  for each  $i \in \{0, \dots, n\}$ . Let  $len(\sigma) = n+1$ ,  $dom(\sigma) = \{0, \dots, n\}$  and  $\forall i \in dom(\sigma) : \sigma(i) = P_i$ .

The syntax of a *propositional formula* over  $\Sigma$  is given by:

$$\varphi := 0 \mid 1 \mid p \in \Sigma \mid \varphi \wedge \varphi \mid \varphi \vee \varphi \mid \neg \varphi,$$

and operators such as  $\Rightarrow$  and  $\Leftrightarrow$  are defined as usual. Let  $\Omega_\Sigma$  be the set of all propositional formulas over  $\Sigma$ .

Let  $i \in dom(\sigma)$ . Then the satisfaction relation  $\sigma, i \models \varphi$  is defined inductively as follows:

$$\begin{aligned} \sigma, i &\models 1, \\ \sigma, i &\models p \quad \text{iff } p \in \sigma(i), \\ \sigma, i &\models \neg p \quad \text{iff } \sigma, i \not\models p, \end{aligned}$$

and the satisfaction relation for the rest of the boolean combinations defined in a natural way.

The syntax of a QDDC formula over  $\Sigma$  is given by:

$$\begin{aligned} D := & \langle \varphi \rangle \mid [\varphi] \mid [[\varphi]] \mid \{\{\varphi\}\} \mid D \sim D \mid \neg D \mid D \vee D \mid \\ & D \wedge D \mid D^* \mid \exists p. D \mid \forall p. D \mid \\ & slen \bowtie c \mid scount \varphi \bowtie c \mid sdur \varphi \bowtie c, \end{aligned}$$

where  $\varphi \in \Omega_\Sigma$ ,  $p \in \Sigma$ ,  $c \in \mathbb{N}$  and  $\bowtie \in \{<, \leq, =, \geq, >\}$ .

An *interval* over a word  $\sigma$  is of the form  $[b, e]$  where  $b, e \in dom(\sigma)$  and  $b \leq e$ . An interval  $[b_1, e_1]$  is a sub interval of  $[b, e]$  if  $b \leq b_1$  and  $e_1 \leq e$ . Let  $Intv(\sigma)$  be the set of all intervals over  $\sigma$ .

Let  $\sigma$  be a word over  $\Sigma$  and let  $[b, e] \in Intv(\sigma)$  be an interval. Then the satisfaction relation of a QDDC formula  $D$  over  $\Sigma$ , written  $\sigma, [b, e] \models D$ , is defined inductively as follows:

$$\begin{aligned} \sigma, [b, e] &\models \langle \varphi \rangle && \text{iff } \sigma, b \models \varphi, \\ \sigma, [b, e] &\models [\varphi] && \text{iff } \forall b \leq i < e : \sigma, i \models \varphi, \\ \sigma, [b, e] &\models [[\varphi]] && \text{iff } \forall b \leq i \leq e : \sigma, i \models \varphi, \\ \sigma, [b, e] &\models \{\{\varphi\}\} && \text{iff } e = b + 1 \text{ and } \sigma, b \models \varphi, \\ \sigma, [b, e] &\models \neg D && \text{iff } \sigma, [b, e] \not\models D, \\ \sigma, [b, e] &\models D_1 \vee D_2 && \text{iff } \sigma, [b, e] \models D_1 \text{ or } \sigma, [b, e] \models D_2, \\ \sigma, [b, e] &\models D_1 \wedge D_2 && \text{iff } \sigma, [b, e] \models D_1 \text{ and } \sigma, [b, e] \models D_2, \\ \sigma, [b, e] &\models D_1 \sim D_2 && \text{iff } \exists b \leq i \leq e : \sigma, [b, i] \models D_1 \text{ and } \\ &&& \sigma, [i, e] \models D_2. \end{aligned}$$

We call word  $\sigma'$  a  $p$ -variant,  $p \in \Sigma$ , of a word  $\sigma$  if  $\forall i \in \text{dom}(\sigma), \forall q \neq p : \sigma'(i)(q) = \sigma(i)(q)$ . Then  $\sigma, [b, e] \models \exists p. D \Leftrightarrow \sigma', [b, e] \models D$  for some  $p$ -variant  $\sigma'$  of  $\sigma$  and,  $\sigma, [b, e] \models \forall p. D \Leftrightarrow \sigma, [b, e] \not\models \exists p. \neg D$ . We define  $\sigma \models D$  iff  $\sigma, [0, \text{len}(\sigma)] \models D$ .

*Example 3.* Let  $\Sigma = \{p, q\}$  and let  $\sigma = P_0 \cdots P_7$  be such that  $\forall 0 \leq i < 7 : P_i = \{p\}$  and  $P_7 = \{q\}$ . Then  $\sigma, [0, 7] \models [p]$  but not  $\sigma, [0, 7] \models [[p]]$  as  $p \notin P_7$ .

*Example 4.* Let  $\Sigma = \{p, q, r\}$  and let  $\sigma = P_0 \cdots P_{10}$  be such that  $\forall 0 \leq i < 4 : P_i = \{p\}$ ,  $\forall 4 \leq i < 8 : P_i = \{p, q, r\}$  and  $\forall 8 \leq i \leq 10 : P_i = \{q, r\}$ . Then

$$\sigma, [0, 10] \models [p] \wedge [\neg p \wedge r]$$

because for  $i \in \{8, 9, 10\}$  the condition  $\exists 0 \leq i \leq 10 : \sigma, [0, i] \models [p]$  and  $\sigma, [i, 10] \models [\neg p \wedge r]$  is met. But  $\sigma, [0, 7] \not\models [p] \wedge [\neg p \wedge r]$  as  $\neg \exists 0 \leq i \leq 7 : \sigma, [0, i] \models [p]$  and  $\sigma, [i, 7] \models [\neg p \wedge r]$ .

Entities *slen*, *scount*, and *sdur* are called *terms*. The term *slen* gives the length of the interval in which it is measured, *scount*  $\varphi$  where  $\varphi \in \Omega_\Sigma$ , counts the number of positions including the last point in the interval under consideration where  $\varphi$  holds, and *sdur*  $\varphi$  gives the number of positions excluding the last point in the interval where  $\varphi$  holds. Formally, for  $\varphi \in \Omega_\Sigma$  we have

$$\begin{aligned} \text{slen}(\sigma, [b, e]) &= e - b, \\ \text{scount}(\sigma, \varphi, [b, e]) &= \sum_{i=b}^{i=e} \begin{cases} 1, & \text{if } \sigma, i \models \varphi, \\ 0, & \text{otherwise.} \end{cases} \\ \text{sdur}(\sigma, \varphi, [b, e]) &= \sum_{i=b}^{i=e-1} \begin{cases} 1, & \text{if } \sigma, i \models \varphi, \\ 0, & \text{otherwise.} \end{cases} \end{aligned}$$

In addition we also use the following derived constructs:  $\sigma, [b, e] \models pt$  iff  $b = e$ ;  $\sigma, [b, e] \models ext$  iff  $b < e$ ;  $\sigma, [b, e] \models \Diamond D$  iff  $true \wedge D \wedge true$  and  $\sigma, [b, e] \models \Box D$  iff  $\sigma, [b, e] \not\models \Diamond \neg D$ .

A *formula automaton* for a QDDC formula  $D$  is a *deterministic finite state automaton* which accepts precisely language  $L = \{\sigma \mid \sigma \models D\}$ .

**Theorem 1.** [10] *For every QDDC formula  $D$  over  $\Sigma$  we can construct a DFA  $\mathcal{A}(D)$  for  $D$  such  $L(D) = L(\mathcal{A}(D))$ .*

## B The Algorithm Implementation

The example shows the explicit state representation of the state space to produce the controller for demonstration purpose.

The algorithms are actually designed to work on symbolic data structure to represent the transition function for each automaton. We use Multi-Terminal BDD(MTBDD) to represent the all the automaton.

The psuedocode of our algorithm is given in the following section.

### Algorithm 1 *SYNTHESIZE*:

**Input:**  $S = (I, O, D^h, \bigwedge_{i=1}^{i=k} (w_i \Leftrightarrow D_i^s), \langle P_1, \dots, P_l \rangle)$

**Output:** Controller for  $S$ .

1.  $A^{mon} = \text{GenMonitorAutomaton}(S)$   
*//Generates prefix closed language equivalent safety automaton*
2.  $A^{mpnc} = \text{GenMPNC}(A^{mon}, I, O)$   
*//Generates MPNC from  $A^{mon}$  and Input-output partitioning*
3. IF initial state of  $A^{mpnc}$  is NOT an accepting state THEN  
 $S$  is unrealizable, generate a counter example tree  
ELSE  
Specification is realizable, GOTO step 4.
4.  $A^{lodc} = \text{GenLODC}(A^{mpnc}, \langle P_1, \dots, P_l \rangle)$   
*//Determinizes the MPNC with respect to Soft Requirements.*
5. Encode  $A^{lodc}$  in an implementation language.

The monitor automaton  $A^{mon}$  is obtained by  $\text{GenMonitorAutomaton}()$ , based on the procedure implemented in a tool DCVALID.

The algorithm for construction of  $A^{mpnc}$  from  $A^{mon}$ , is implemented by the function  $\text{GenMPNC}()$ . To illustrate this function, we first define the function  $C_{step}: S \times 2^S \rightarrow \{1, 0\}$  as follows:

$$C_{step}(s, G) = 1 \text{ if } \forall i, \exists o : \delta(s, (i, o)) \in G$$

$$\text{else } C_{step}(s, G) = 0.$$

where  $i \in I$  and  $o \in (O \cup W)$  and  $s \in S$ .

### Algorithm 2 *GenMPNC*:

**Input:**  $A^{mon}, I, O, W$

**Output:**  $A^{mpnc}$ .

$S$  = set of states in  $A^{mon}$ ,

$F$  = set of accepting states in  $A^{mon}$

$\delta: S \times (I \cup O \cup W) \rightarrow S$  be the transition function in  $A^{mon}$ .

$\mathcal{V}: S \rightarrow \{1, 0\}$  be a value function over  $S$   
Initialize  $\mathcal{V}(s)=1 \forall s \in G$ , otherwise  $\mathcal{V}(s) = 0$   
SET  $G = F$   
DO  
     $Pre\_V = V$   
    FOR each  $s \in G$  do  
        IF  $C_{step}(s, G) = 0$  then  
             $\mathcal{V}(s) = 0$   
             $G = G - s$   
    WHILE ( $Pre\_V \neq V$ )  
 $A^{mpnc} = \text{Created from } A^{mon} \text{ by keeping only the states } s \in G \text{ and}$   
transitions  $(s, t)$  s.t.  $s \in G$  and  $t \in G$ .

Now, we give construction of  $A^{lodc}$  from  $A^{mpnc}$ , which is implemented by the function  $GenLODC()$ .  $GenLODC()$  determinizes the automaton such that for any input a unique output can be selected.

We define the function  $evaluateSoftReq(\langle P_1, \dots, P_l \rangle, \text{input output valuation})$ , which takes list of soft requirements and input-output valuation as input and returns the weighted value of the soft requirements being satisfied by the valuation.

We also define  $lookupTable: I \rightarrow (O \times S \times Integer)$ , which contains for each input, the output value and the next state, that maximizes the satisfaction of soft requirements. Similarly a function  $initLookup: lookupTable \times val \rightarrow lookupTable$  initializes the lookupTable to some minimal value val for each input valuation..

**Algorithm 3 *GenLODC*:**

**Input:**  $A^{mpnc}$ ,  $I$ ,  $O$ ,  $\langle P_1, \dots, P_l \rangle$   
**Output:**  $A^{lodc}$ .  
 $S = \text{set of states in } A^{mpnc}$ ,  
 $initLookup(lookupTable, -1)$  initializes the lookupTable by the -1 for each input.  
FOR every state  $s \in S$  DO  
    FOR every valuation  $(i, o, w)$  of  $(I \cup O \cup W)$   
         $val = evaluateSoftReq(\langle P_1, \dots, P_l \rangle, (i, o, w))$   
        IF  $val > lookupTable(i)$  THEN  $lookupTable(i) = \{val, o, next\_state\}$   
Create the Automaton  $A^{lodc}$  with updated transitions with valuation for each input and the corresponding output valuation given in lookupTable for each state.

**Complexity Results:** The algorithms work directly on this symbolic representation, including function  $C_{step}$  used inside GenMPNC. For the algorithm GenMPNC, the worst case complexity is  $\mathcal{O}(N^2 \cdot |BDD|)$ , where  $N$  is the number of states in monitor automaton  $A^{mon}$ . This can be derived from the fact that the maximum number of iterations to reach a fix-point is  $(N - 1)$ , and in each iteration there can be  $\mathcal{O}(N)$  step for each state which are marked as good. Each such state may requires  $\mathcal{O}(|BDD|)$  steps to determine whether the state is winning or not (determined by function  $C_{step}$ ).  $|BDD|$  represents the size of the MTBDD datastructure in terms of the number of BDD nodes.

The function  $C_{step}$  is an important function as it is the core function used to find the winning region. We implement this function over MTBDD data structure *without actually creating a game graph*.

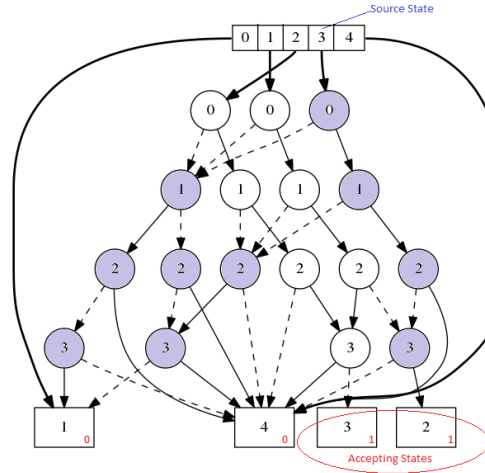
We give the outline of our algorithm as follows:

We assume that safety monitor automaton  $A^{mon}$  is given as a dfa  $M = (Q, \Sigma, \delta, G)$  where  $G \subseteq Q$  is the set of accepting states.  $\Sigma = 2^{(I \cup O \cup W)}$  is the alphabet and  $\delta : Q \times \Sigma \rightarrow Q$  with  $Q - G$  being the reject states. We assume that  $\delta$  is encoded as MTBDD as in MONA.

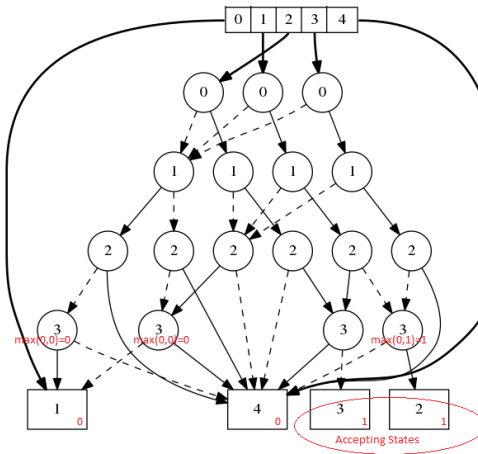
In MTBDD the bdd nodes can be categorized as *internal nodes* or the *terminal node*. The terminal node represent the destination state of the transition. The internal nodes represent the decision on some variable  $v \in (I \cup O \cup W)$ .

Our algorithm start by labelling each terminal node with a value and then propagating this value to the bdd node corresponding to source state to see whether the source state belong to the winning region or not.

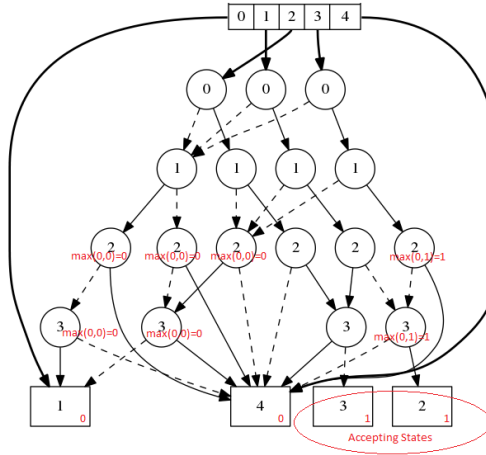
1. We starts by labeling each terminal node. Every terminal node is labelled as 1 if it belongs to accepting states, otherwise it is labelled as 0.
2. then we label the internal bdd nodes whose successors are already labelled as follows: if the internal node represents the decision on an input variable then its lable is minimum of its successors. Otherwise (representing decision on output or indicator variable), the internal node is labeled by maximum of its sucessor.
3. step 2 is performed recursively until we get the bdd node corresponding to sources (starting) state labeled with 0 or 1. If bdd node for source state is labelled as 1 then it is inside the winning region based on current labeling of terminal nodes. If bdd node for source state is labelled as 0 then it's not in the winning region and can be removed during construction of MPNC.



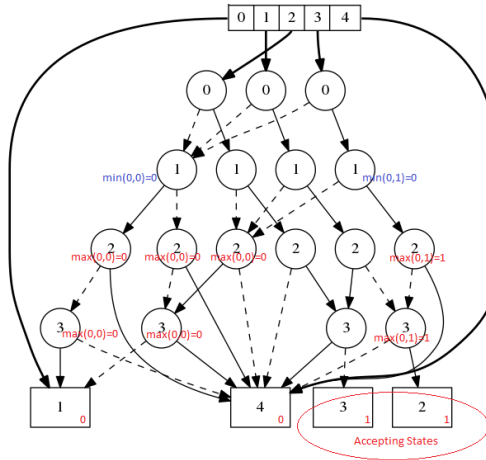
**Fig. 5.** MPNC Computation over MTBDD for state 3: BDD nodes colored purple to be evaluated



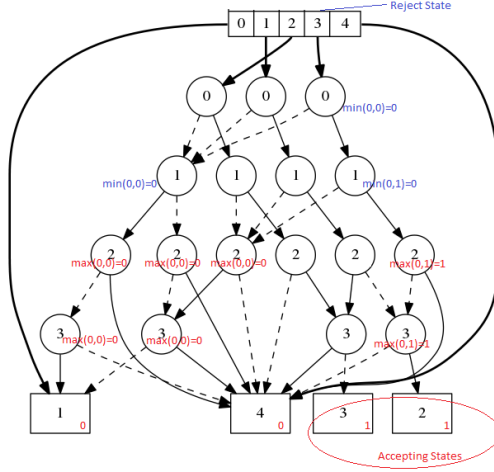
**Fig. 6.** MPNC Computation over MTBDD for variable index 3



**Fig. 7.** MPNC Computation over MTBDD for variable index 2



**Fig. 8.** MPNC Computation over MTBDD for variable index 1



**Fig. 9.** MPNC Computation over MTBDD for variable index 0

The example computation of  $C_{step}$  function of the MTBDD for source state 3 and starting with the winning region states  $\{3, 4\}$  is shown in the figures from B to B. In the MTBDD there are 4 variables indexed as 0,1,2 and 3. The variable indexed 0,1 are inputs and 2, 3 are outputs. All internal nodes are represented by circle and encircled number is the decision variable. All terminal nodes are represented by rectangle and number inside that is the destination state number. The list on the top corresponds to the state numbered 0 to 4.

Similarly the worst case complexity for GenLODC could be calculated as  $\mathcal{O}(N.l.(2^{|I \cup O \cup W|}))$ , where  $N$  is the number of states in MPNC,  $l$  is the number of soft requirements. This can be derived from the fact that maximum number of states in LODC can be equal to MPNC in case MPNC itself is a deterministic automaton. For each state in LODC we have to compute its locally optimal output, which depends on the number of soft requirements to be computed.

Although in worst case  $|BDD|$  can be  $\mathcal{O}(2^{|I \cup O \cup W|})$ , but in most of the practical examples the size of MTBDD is much smaller, and therefore the tool performs much better than the worst case estimation.

In Section B.1 we give an algorithm for GenLODC to exploit the shared bdd nodes in MTBDD. The results show the considerable improvement over the naive explicit path enumeration based algorithm.



## B.1 LODC Optimization

We have also developed an algorithm to efficiently compute the LODC from MPNC. Following section gives the brief overview of algorithm.

**Outline of Optimization Algorithm** We assume that MPNC is given as a dfa  $M = (Q, \Sigma, \delta, r)$  where  $r$  is the unique reject state.  $\Sigma = 2^{(I \cup O)}$  is the alphabet and  $\delta : Q \times \Sigma \rightarrow Q$  with  $r$  being the SINK state. We assume that  $\delta$  is encoded as multi terminal BDD as in MONA. Being MPNC it is assumed that

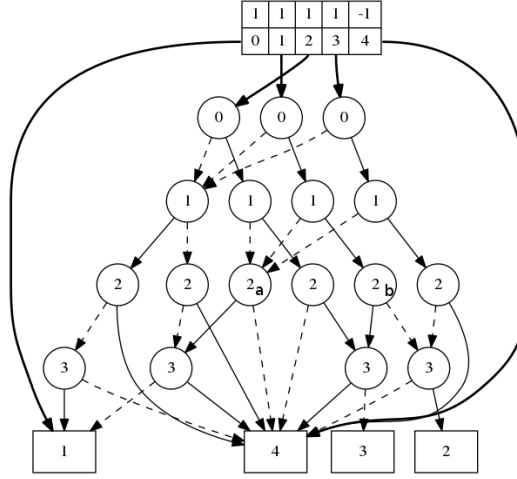
$$\forall q \neq r. \forall i \in 2^I. \exists o \in 2^O. \delta(q, i \cup o) \in Q - \{r\}$$

*Problem* Given MPNC  $M$  and soft goals a sequence of literals  $(l_1, l_2, \dots, l_r)$  where  $l_i = o$  or  $l_i = \neg o$  for  $o \in O$ , aim is to construct LODC  $N$  by choosing exactly one of permitted outputs which maximizes the value of soft goal list (considered lexicographically ordered). Note that LODC satisfies the condition

$$\begin{aligned} &\forall q \neq r. \forall i \in 2^I. \\ &(\exists! o \in 2^O. \delta_{lodc}(q, i \cup o) \in Q - \{r\} \wedge \\ &(\forall o' \in 2^O. \delta_{mpnc}(1, i \cup o') \in Q - \{r\} \Rightarrow val(i \cup o') \leq val(i \cup o))) \end{aligned}$$

**We assume that in the bdd representation all  $O$  occur after  $I$ .** The BDD node which is either terminal or labelled by output variable such that all its ancestors are input labelled is called a **frontier** node. See the example below. In the Figure B.1, bdd nodes marked 0,1,2,3 correspond to variables  $req1$ ,  $req2$ ,  $ack1$  and  $ack2$ . Nodes marked 2 are the frontier nodes. Note that 4 is the reject state. For the leftmost frontier node marked (2), we can see that  $ack1 = true$  as well as  $ack1 = false, ack2 = false$  lead to reject state 4 (these are infeasible paths), where as  $ack1 = false, ack2 = true$  leads to good state 1. Hence  $ack1 = false, ack2 = true$  is the unique feasible path. Now consider the second rightmost frontier node marked (2). It has two feasible paths  $P1 = (ack1 = true, ack2 = false)$  going to target state 3 and  $P2 = (ack1 = false, ack2 = true)$  going to target state 2.

*Step 1* Our algorithm works by assigning to each frontier node  $N$  an output valuation, a reward value to each frontier node and the target state. Note that under given soft goal list, an optimal value can be assigned to a frontier node purely by choosing an output path, from all feasible outputs (i.e. outputs which don't end in reject node  $r$ ), one which maximizes the value of the softgoal list. This path ends in the target state.



**Fig. 10.** BDD-representation of a Transition function.

*Example 5.* For example, in above figure for the second rightmost frontier node marked (2b) has It has two feasible paths  $P1 = (ack1 = true, ack2 = false)$  going to target state 3 and  $P2 = (ack1 = false, ack2 = true)$  going to target state 2. Given soft goal  $(ack1, ack2)$ , path  $P1$  has higher lexicographic value and must be selected as optimal. Thus, the node can be marked with  $optoutput = (ack1 = true, ack2 = false)$ ,  $optvalue = (1, 0)$  and  $optstate = 3$ .

*Step 2* we can systematically enumerate all the paths to frontier nodes (mentioning only source state and the value of variables which occur on the path). It is clear that for any two such paths originating from the same source state the value of at least one of the input variables is different, hence we get distinct cases. (There can be identical input paths starting from different states. see example below.) For each such path, we set the output and next state to the output valuation and target state of the frontier node.

*Example 6.* For the second rightmost frontier node marked (2-b), we have a unique input path  $req1 = true, req2 = true$  which originates from state 1. In conjunction with above above example, we get the scade transition

state=1 AND req1 AND req2 -> ack1=true, ack2=true, state=3

For the third leftmost state marked (2-a) there are three input paths with  $req1 = true, req2 = false$  originating in states either 1,2 or 3.

The psuedocode of our algorithm is given as follows:

```

for each frontier node N
{
    optoutput[N] := bottom, optvalue[N] = -1, optstate := bottom;
    for each output-path, PATH, to a non-rejecting state
    {
        output,value,endstate := maxoutput(PATH,SOFTGOAL)
        if optvalue[N] < value
        {
            optoutput[N] := output;
            optvalue[N] := value;
            optstate[N] := state;
        }
    }
}
// the frontier node now has optimal output and its reward value

//Next we generate LODC DFA below

Initialize a new DFA with same states as MPNC and
    with default transition to the unique reject state r.
    All other states are accept states.

for each each source state,
    for each input path, PATH, to a frontier node N
    {
        add Transition(PATH,optoutput[N],optstate[N]) to DFA
    }

LODC := Minimized(DFA) // this gets rid of unreachable state

```

## C Case studies

In this section we give few sythesis case studies in our logic formalism. We show the controller synthesis from the logic specification and the effect of soft requirements on the sythesized controller. We also compare the sythesized controllers based on our performance measurement algorithm. Performance parameters therefore gives the quantitative matrices of betterness of one controller over the other and can be used as the *formal guarantees* for the sythesized controller with respect to the soft requirements.

### C.1 MinePump

In this section we present the detailed specification of a minepump controller. We first specify some useful generic properties which would used for requirement specification in case studies.

- $lag(P, Q, n)$ : specifies that in any observation interval if  $P$  holds continuously for  $n+1$  cycles and persists then  $Q$  holds from  $(n+1)^{th}$  cycle onwards and persists till  $P$  persists. This specification is represented by following formula.

$$\Box ([P] \ \&\& \ \text{slen} \geq n-1 \Rightarrow \text{slen} = n-1 \wedge [Q])$$

- $tracks(P, Q, n)$ : in any observation interval if  $P$  is continuously true for  $n$  cycles then  $Q$  persists as long as  $P$  persists or for  $n$  cycles whichever is shorter.

$$\{P\} \leq n = \{Q\}$$

- $sep(P, n)$ : any interval which begins with a falling edge of  $P$  and ends with a rising edge of  $P$  then the length of the interval should be at least  $n$  cycles.

$$\Box ([P] \wedge [\neg P] \wedge \langle P \rangle \Rightarrow \text{slen} > n)$$

- $ubound(P, n)$ : in any observation interval  $P$  can be continuously true for at most  $n$  cycles.

$$\Box ([P] \Rightarrow \text{slen} < n)$$

**Case Study Description:** Imagine a minepump which keeps the water level in a mine under control for the safety of miners. The pump is driven by a controller which can switch it *on* and *off*. Mines are prone to methane leakage trapped underground which is highly flammable. So as a safety measure if a methane leakage is detected the controller is not allowed to switch on the pump under no circumstances.

The controller has two input sensors - HH2O which becomes 1 when water level is high, and HCH4 which is 1 when there is a methane leakage; and can generate two output signals - ALARM which is set to 1 to sound/persist the alarm, and PUMPON which is set to 1 to switch on the pump. The objective of the controller is to *safely* operate the pump and the alarm in such a way that the water level is never dangerous, indicated by the indicator variable DH2O, whenever certain assumptions hold. We have the following assumptions on the mine and the pump.

- Sensor reliability assumption:  $ppref(DH2O \Rightarrow HH2O)$  where  $ppref(D) = \neg((\neg D) \wedge ext)$ . If HH2O is false then so is DH2O.
- Water seepage assumptions:  $tracks(HH2O, DH2O, w)$ . The minimum no. of cycles for water level to become dangerous once it becomes high is  $w$ .
- Pump capacity assumption:  $lags(PUMPON, !HH2O, epsilon)$ . If pump is switched on for at least  $epsilon + 1$  cycles then water level will not be high after  $epsilon$  cycles.
- Methane release assumptions:  $sep(HCH4, zeta)$  and  $ubound(HCH4, kappa)$ . The minimum separation between the two leaks of methane is  $zeta$  cycles and the methane leak cannot persist for more than  $kappa$  cycles.
- Initial condition assumption:  $init(<!HH2O> \&\& <!HCH4>, slen = 0)$ . Initially neither the water level is high nor there is a methane leakage.

The commitments are:

- Alarm control:  $lags(HH2O, ALARM, delta)$  and  $lags(HCH4, ALARM, delta)$  and  $lags(!HH2O \&\& !HCH4, !ALARM, delta)$ . If the water level is dangerous then alarm will be high after  $delta$  cycles and if there is a methane leakage then alarm will be high after  $delta$  cycles. If neither the water level is dangerous nor there is a methane leakage then alarm should be off after  $delta$  cycle.
- Safety condition:  $ppref(!DH2O \&\& (HCH4 \Rightarrow !PUMPON))$ . The water level should never become dangerous and whenever there is a methane leakage pump should be off.

We can automatically synthesize a controller for the values say  $w = 8$ ,  $\epsilon = 2$ ,  $\zeta = 10$ ,  $\kappa = 1$ , and  $\delta = 1$ . The complete textual DCSynth specification of minepump is given in figure 14.

**Soft goals and Performance measurement** We could also synthesize the minepump controllers with each one of the following as a **soft requirement** giving three different controllers. (Note that these requirements are mutually contradictory. So they are not given together.)

- **MPV1:** Keep the pump switched on whenever possible (*specified by soft requirement  $PUMPON$* ).
- **MPV2:** Keep pump off if there is a methane leak in last 2 cycles otherwise switch on the pump (*specified by soft requirement  $(CH4_{Last2Cyc} \Rightarrow !PUMPON)$ , where  $CH4_{Last2Cyc}$  indicates that there was a methane leak within last 2 cycles*).
- **MPV3:** Keep pump off as much as possible i. e. delay the switching on the pump as much as possible (*specified by soft requirement  $!PUMPON$* ).

We have measured the performance of the three synthesized controllers each, taking into account one soft requirement at a time. The performance is measured in terms the maximum amount of time (in cycles) for which the water level can remain high without violating the assumptions and the detailed results are tabulated in Table. 5.

**Simulation of Synthesized Minepump Controllers** The controllers are encoded as Lustre specification and Lustre V4 tools are used for simulation. The example simulation for these three variants of Minepump is shown in figures 11, 12 and 13 respectively.

## D Experimental results and Performance Evaluation

This section is divided into two subsections. One deals with the performance of the tools and its comparison with the other state of the art tools. The implementation of tool DCSYNTH is based on the algorithms presented in Section B. The second section deals with the performance evaluation of synthesized controller. This allows the comparison of controllers produced for the same hard requirement with different soft-requirements based on user defined performance measure specified as maxlen of a QDDC formula.

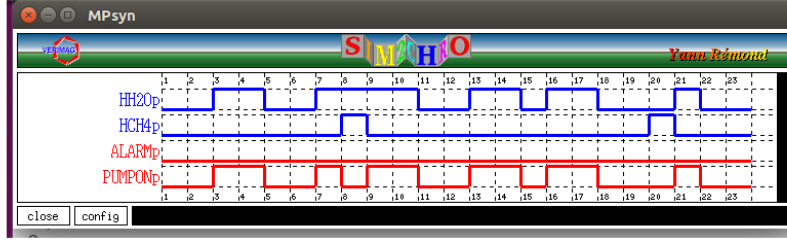


Fig. 11. Simulation of Minepump Controller Variant MP\_V1

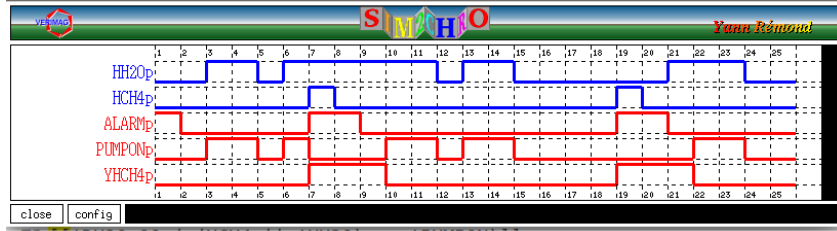


Fig. 12. Simulation of Minepump Controller Variant MP\_V2

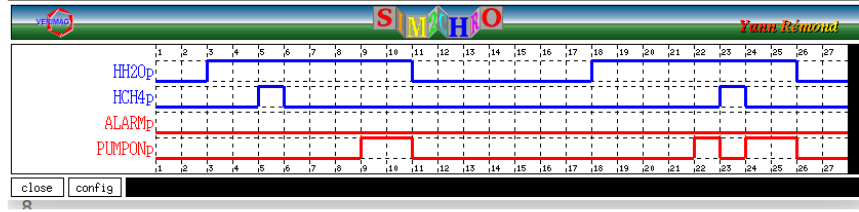


Fig. 13. Simulation of Minepump Controller Variant MP\_V3

## D.1 Tool Performance

Table 6 shows how DCSynth fares against Acacia+, which is a leading tool for synthesis of controllers from temporal logic specification. Acacia+ can handle LTL and PSL specification as well as quantitative synthesis with mean payoff objectives. In contrast, our tool can only handle past time temporal properties but it can handle *soft requirements* which other tools like Acacia+ cannot. Table 6 compares the performance of DCSYNTH against Acacia+ for examples with only hard safety requirements. It is noteworthy that controllers for complex specifications such as *MINEPUMP* could be synthesized with DCSYNTH. Table 1 gives the results of synthesis using DCSYNTH for specifications which include soft requirements.

In the table 6 the example  $Arb^{tok}(n)$  indicates the n cell arbiter, with a token circulating between them. Apart from the three invariant specifications (ARBINV) for the arbiter given in section 2 it specifies the requirement that if a cell has the request line true and it also has the token then it would surely get an acknowledgment. The specification also says that the initially token is with cell 0, in next cycle token is owned by cell 1, then 2 and so on till it reaches the last cell. At this time the token comes back to cell 0.

Similarly MP indicates the minepump example without soft requirement specification as given in section C.1.

**Table 6.** Comparison of Synthesis in Acacia+ and DCSYNTH

Problem	Acacia+		DCSynth	
	time (Sec)	Memory /States	time (Sec)	Memory /States
$Arb^{hard}(4, 4)$	0.4	29.8/ 55	0.08	9.1/ 50
$Arb^{hard}(5, 5)$	11.4	71.9/ 293	5.03	28.1/ 432
$Arb^{hard}(6, 6)$	TO <sup>a</sup>	-	80	1053.0/ 4802
$Arb^{hard}(7, 7)$	TO	-	-	MO <sup>b</sup>
$Arb^{tok}(7)$	9.65	39.1/ 57	0.3	7.3/ 7
$Arb^{tok}(8)$	46.44	77.9/ 73	2.2	16.2/ 8
$Arb^{tok}(10)$	NC <sup>c</sup>	-	152	82.0/ 10
$Arb^{tok}(12)$	NC	-	TO	255.0/ 12
MINEPUMP	NC	-	0.06	50/ 32

<sup>a</sup> TO=timeout

<sup>b</sup> MO=memory out

<sup>c</sup> NC=synthesis inconclusive



## E Minepump Source

```
BEGIN QDDCSYNTH MinePump
INTERFACESPEC
  HH2Op: INPUT
  HCH4p: INPUT
  ALARMp: OUTPUT MONITOR x
  PUMPOp: OUTPUT MONITOR x
  YHCH4p: OUTPUT MONITOR x;
SOFTREQS
  ((!YHCH4p)|(!PUMPOp))>>(PUMPOp) ;
AUXVARS
  DH2O
;
CONSTANTS
  - delta response time of PUMP and ALARMS after trigger
  delta = 1, w = 8, epsilon=2 , zeta=10, kappa=1
;
DEFINE
  - Alarm control
  define alarm1(HH2O, DH2O, HCH4, ALARM, PUMPOp) as
    HH2O = delta => ALARM ;
  define alarm2(HH2O, DH2O, HCH4, ALARM, PUMPOp) as
    HCH4 = delta => ALARM ;
  define alarm3(HH2O, DH2O, HCH4, ALARM, PUMPOp) as
    !HCH4 && !HH2O = delta => !ALARM ;
  - Water seepage Assumptions
  define water1(HH2O, DH2O, HCH4, ALARM, PUMPOp) as
    [] ( [] DH2O => HH2O [] ) ;
  define water2(HH2O, DH2O, HCH4, ALARM, PUMPOp) as
    HH2O <= w = ! DH2O ;
  - Pump capacity assumption
  define pumpcap1(HH2O,DH2O,HCH4,ALARM,PUMPOp) as
    PUMPOp = epsilon => !HH2O ;
  - Methane Release assumptions
  define methane1(HH2O,DH2O,HCH4,ALARM,PUMPOp) as
    [] ( [HCH4]^[!HCH4]^(<HCH4> => slen > zeta ) ;
  define methane2(HH2O,DH2O,HCH4,ALARM,PUMPOp) as
    [] ( [[HCH4]] => slen < kappa ) ;
  - Initial condition assumption
  define initdry(HH2O, DH2O, HCH4, ALARM, PUMPOp) as
    <!HH2O> ^ true ;
  - safety condition
  define safe(HH2O, DH2O, HCH4, ALARM, PUMPOp) as
    [[!DH2O && ( (HCH4 || !HH2O) => !PUMPOp)]];
```

```

define plant(HH2O, DH2O, HCH4, ALARM, PUMPON) as
  initdry(HH2O, DH2O, HCH4, ALARM, PUMPON) &&
  water1(HH2O, DH2O, HCH4, ALARM, PUMPON) &&
  water2(HH2O, DH2O, HCH4, ALARM, PUMPON) &&
  pumpcap1(HH2O, DH2O, HCH4, ALARM, PUMPON) &&
  methane1(HH2O, DH2O, HCH4, ALARM, PUMPON) &&
  methane2(HH2O, DH2O, HCH4, ALARM, PUMPON);
define req(HH2O, DH2O, HCH4, ALARM, PUMPON) as
infer MPsyn as
INDICATORS
  YHCH4p : (slen=2 && <><HCH4p>)
;
ASSUME
  plant(HH2Op, DH2O, HCH4p, ALARMp, PUMPONp)
;
REQUIRES
  req(HH2Op, DH2O, HCH4p, ALARMp, PUMPONp)
;
SYNTHESIZE
SynthG MPsyn
END QDDCSYNTH

```

**Fig. 14.** DCSynth spec for Minepump.

## F Textual Specification of Arbiter Case Study

The DCSynth specification of the 4 cell arbiter is shown in figure 15. It can be easily generalized to n-cells.

```
BEGIN QDDCSYNTH arbiter-4-cell
  INTERFACESPEC
    req1: INPUT
    req2: INPUT
    req3: INPUT
    req4: INPUT
    ack1: OUTPUT MONITOR x
    ack2: OUTPUT MONITOR x
    ack3: OUTPUT MONITOR x
    ack4: OUTPUT MONITOR x
    sr1: OUTPUT MONITOR x
    sr2: OUTPUT MONITOR x
    sr3: OUTPUT MONITOR x
    sr4: OUTPUT MONITOR x
    ;
  SOFTREQS
    (sr4)>>(sr3)>>(sr2)>>(sr1)
    ;
  CONSTANTS
    ;
  AUXVARS
    ;
  DEFINE
    – Acknowledgments should be exclusive
    define exclusion() as
      [!((ack1 => !((ack2 || (ack3 || (ack4))) &&
        (ack2 => !((ack1 || (ack3 || (ack4))) &&
        (ack3 => !((ack1 || (ack2 || (ack4))) &&
        (ack4 => !((ack1 || (ack2 || (ack3))))))]];
    – No lost cycle
    define nolooss() as
      [!(((req1 || (req2 || (req3 || (req4))
        => ((ack1 || (ack2 || (ack3 || (ack4))))];
    – Ack should be granted if there is a request
    define nospuriousack(ack, req) as
      [[ack => req]];
    – 2 cycle response property
    define response(req, ack) as
      [ !(((req) && (slen=k-1)) => <>< ack >);
```

```
infer arbiter4cell as
INDICATORS
sr1 : (response(req1, ack1))
sr2 : (response(req2, ack2))
sr3 : (response(req3, ack3))
sr4 : (response(req4, ack4))
;
ASSUME
;
REQUIRES
exclusion()
noloss()
nospuriousack(ack1, req1)
nospuriousack(ack2, req2)
nospuriousack(ack3, req3)
nospuriousack(ack4, req4)
;
SYNTHESIZE
SynthG arbiter4cell
END QDDCSYNTH
```

**Fig. 15.** DCSynth spec for 4 Cell Arbiter.