



1. Description

1.1. Project

Project Name	AV_ROS
Board Name	NUCLEO-F767ZI
Generated with:	STM32CubeMX 6.6.1
Date	04/17/2023

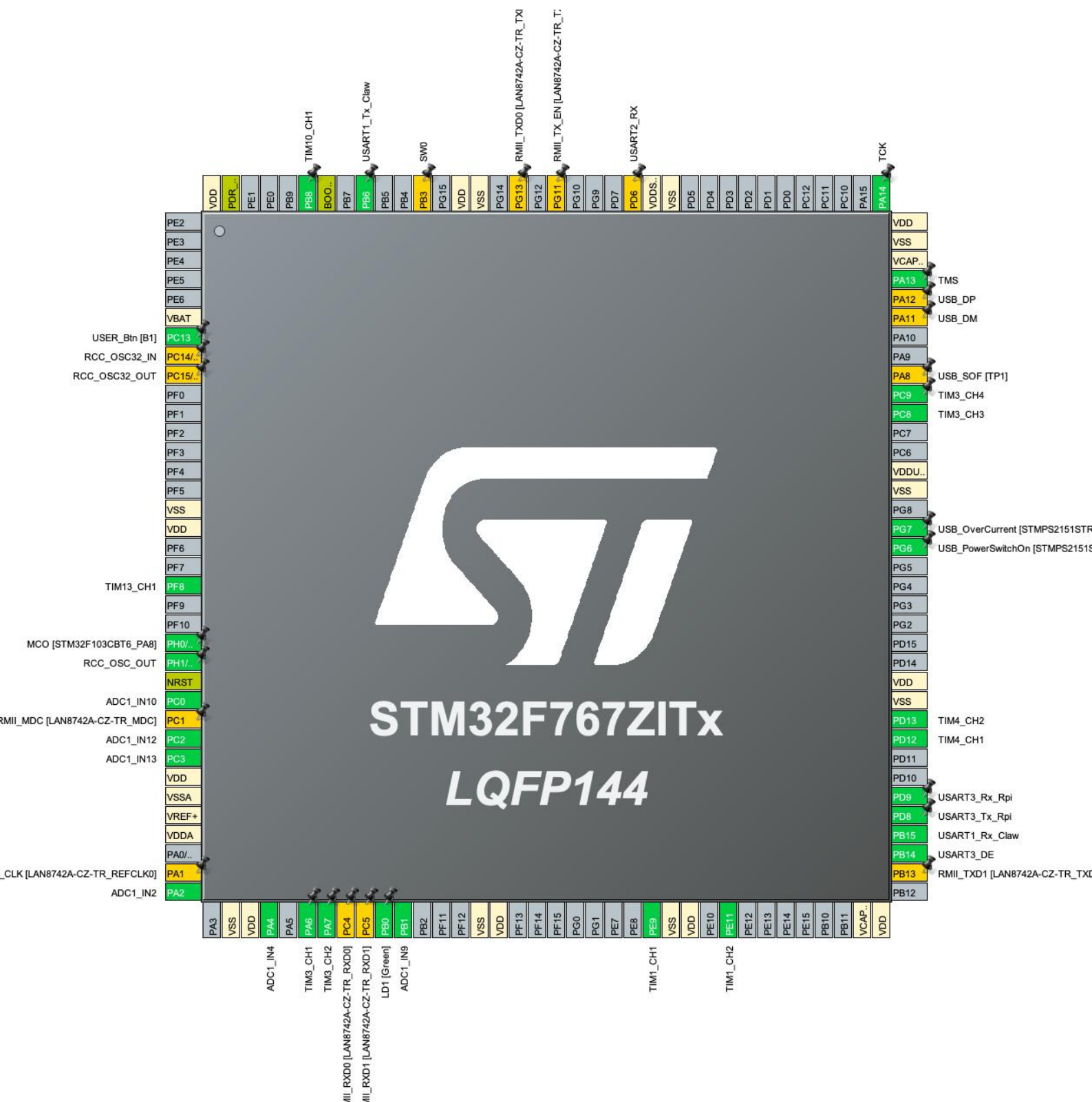
1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767ZITx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M7
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2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	USER_Btn [B1]
8	PC14/OSC32_IN *	I/O	RCC_OSC32_IN	
9	PC15/OSC32_OUT *	I/O	RCC_OSC32_OUT	
16	VSS	Power		
17	VDD	Power		
20	PF8	I/O	TIM13_CH1	
23	PH0/OSC_IN	I/O	RCC_OSC_IN	MCO [STM32F103CBT6_PA8]
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0	I/O	ADC1_IN10	
27	PC1 *	I/O	ETH_MDC	RMII_MDC [LAN8742A-CZ- TR_MDC]
28	PC2	I/O	ADC1_IN12	
29	PC3	I/O	ADC1_IN13	
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
35	PA1 *	I/O	ETH_REF_CLK	RMII_REF_CLK [LAN8742A-CZ- TR_REFCLK0]
36	PA2	I/O	ADC1_IN2	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	ADC1_IN4	
42	PA6	I/O	TIM3_CH1	
43	PA7	I/O	TIM3_CH2	
44	PC4 *	I/O	ETH_RXD0	RMII_RXD0 [LAN8742A-CZ- TR_RXD0]
45	PC5 *	I/O	ETH_RXD1	RMII_RXD1 [LAN8742A-CZ- TR_RXD1]
46	PB0 **	I/O	GPIO_Output	LD1 [Green]
47	PB1	I/O	ADC1_IN9	
51	VSS	Power		
52	VDD	Power		

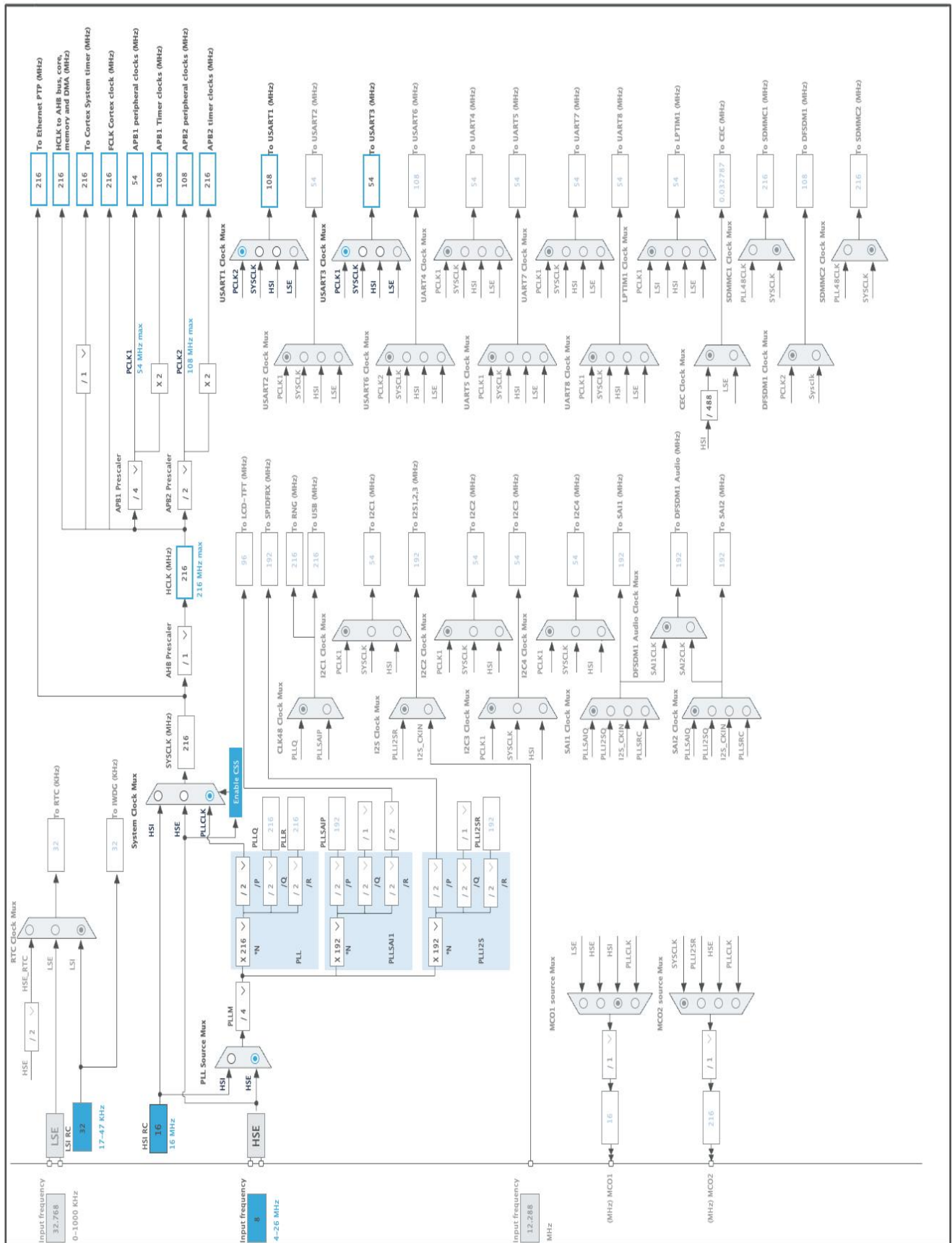
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
60	PE9	I/O	TIM1_CH1	
61	VSS	Power		
62	VDD	Power		
64	PE11	I/O	TIM1_CH2	
71	VCAP_1	Power		
72	VDD	Power		
74	PB13 *	I/O	ETH_TXD1	RMII_TXD1 [LAN8742A-CZ- TR_TXD1]
75	PB14	I/O	USART3_DE	
76	PB15	I/O	USART1_RX	USART1_Rx_Clav
77	PD8	I/O	USART3_TX	USART3_Tx_Rpi
78	PD9	I/O	USART3_RX	USART3_Rx_Rpi
81	PD12	I/O	TIM4_CH1	
82	PD13	I/O	TIM4_CH2	
83	VSS	Power		
84	VDD	Power		
91	PG6 **	I/O	GPIO_Output	USB_PowerSwitchOn [STMPS2151STR_EN]
92	PG7 **	I/O	GPIO_Input	USB_OverCurrent [STMPS2151STR_FAULT]
94	VSS	Power		
95	VDDUSB	Power		
98	PC8	I/O	TIM3_CH3	
99	PC9	I/O	TIM3_CH4	
100	PA8 *	I/O	USB_OTG_FS_SOF	USB_SOF [TP1]
103	PA11 *	I/O	USB_OTG_FS_DM	USB_DM
104	PA12 *	I/O	USB_OTG_FS_DP	USB_DP
105	PA13	I/O	SYS_JTMS-SWDIO	TMS
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	TCK
120	VSS	Power		
121	VDDSDMMC	Power		
122	PD6 *	I/O	USART2_RX	
126	PG11 *	I/O	ETH_TX_EN	RMII_TX_EN [LAN8742A- CZ-TR_TXEN]
128	PG13 *	I/O	ETH_TXD0	RMII_TXD0 [LAN8742A-CZ- TR_TXD0]
130	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
131	VDD	Power		
133	PB3 *	I/O	SYS_JTDO-SWO	SW0
136	PB6	I/O	USART1_TX	USART1_Tx_Claw
138	BOOT0	Boot		
139	PB8	I/O	TIM10_CH1	
143	PDR_ON	Reset		
144	VDD	Power		

** The pin is affected with an I/O function

* The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	AV_ROS
Project Folder	/Users/laglt2/Documents/GitHub/NGCP_UGV_2022/AV_ROS
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F7 V1.17.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_USART1_UART_Init	USART1
5	MX_USART3_UART_Init	USART3
6	MX_TIM11_Init	TIM11
7	MX_TIM3_Init	TIM3
8	MX_TIM4_Init	TIM4
9	MX_TIM1_Init	TIM1
10	MX_TIM13_Init	TIM13
11	MX_TIM10_Init	TIM10

Rank	Function Name	Peripheral Instance Name
12	MX_ADC1_Init	ADC1

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
MCU	STM32F767ZITx
Datasheet	DS11532_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

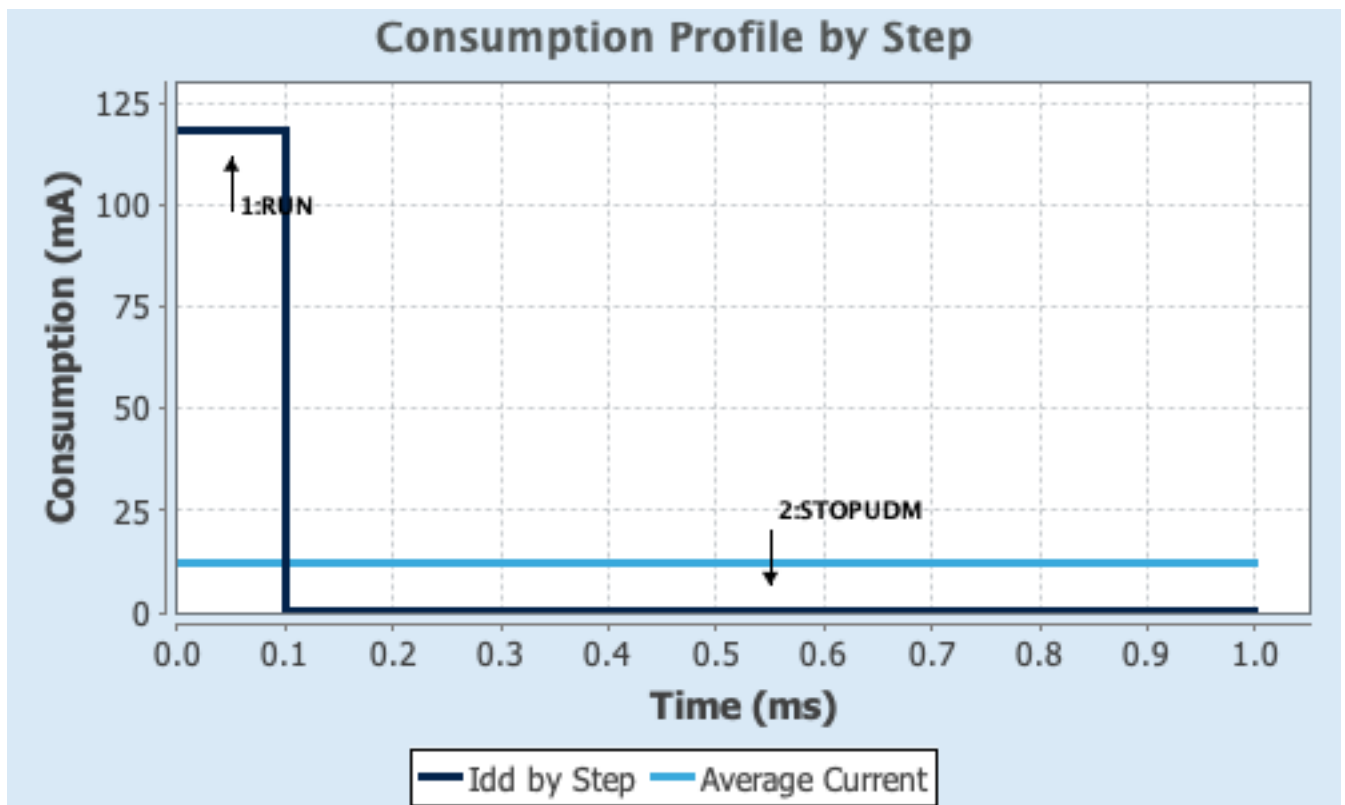
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	ICTM FLASH-SingleBank REGON	n/a
CPU Frequency	216 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	118 mA	130 μ A
Duration	0.1 ms	0.9 ms
DMIPS	462.0	0.0
Ta Max	89.42	104.98
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	11.92 mA
Battery Life	2 days, 4 hours	Average DMIPS	462.24005 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN2

mode: IN4

mode: IN9

mode: IN10

mode: IN12

mode: IN13

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler PCLK2 divided by 4

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment

Scan Conversion Mode Enabled

Continuous Conversion Mode **Enabled ***

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

End Of Conversion Selection EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion **5 ***

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

Rank 1

Channel **Channel 4 ***

Sampling Time 3 Cycles

Rank **2 ***

Channel **Channel 9 ***

Sampling Time 3 Cycles

Rank **3 ***

Channel **Channel 10 ***

Sampling Time 3 Cycles

Rank **4 ***

Channel **Channel 12 ***

Sampling Time 3 Cycles

Rank **5 ***

Channel	Channel 13 *
Sampling Time	3 Cycles
ADC_Injected_ConversionMode:	
Number Of Conversions	0
WatchDog:	
Enable Analog WatchDog Mode	false

7.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.3. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.4. TIM1

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

7.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	1 *
Counter Mode	Up

Counter Period (AutoReload Register - 16 bits value) **32767 ***

Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 16 bits value) 0

auto-reload preload **Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO Reset (UG bit from TIMx_EGR)

Trigger Event Selection TRGO2 Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State Disable

BRK Polarity High

BRK Filter (4 bits value) 0

BRK Sources Configuration

- Digital Input Disable

- DFSDM Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State Disable

BRK2 Polarity High

BRK2 Filter (4 bits value) 0

BRK2 Sources Configuration

- Digital Input Disable

- DFSDM Disable

Break And Dead Time management - Output Configuration:

Automatic Output State Disable

Off State Selection for Run Mode (OSSR) Disable

Off State Selection for Idle Mode (OSSI) Disable

Lock Configuration Off

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

CH Idle State Reset

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

CH Idle State Reset

7.5. TIM3

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0

Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.6. TIM4

Combined Channels: Encoder Mode

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode

Encoder Mode TI1 and TI2 *

____ Parameters for Channel 1 ____

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	10 *

____ Parameters for Channel 2 ____

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	10 *

7.7. TIM10

mode: Activated

Channel1: PWM Generation CH1

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	14 *
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Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	57599 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Enable *

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.8. TIM11

mode: Activated

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	8 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	60000-1 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Enable *

7.9. TIM13

mode: Activated

Channel1: Input Capture direct mode

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	2700-1 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct

Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.10. USART1

Mode: Asynchronous

7.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.11. USART3

Mode: Asynchronous

mode: Hardware Flow Control (RS485)

7.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	57600 *
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
Polarity	High
Assertion Time	0
Deassertion Time	0

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

* **User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN10	Analog mode	No pull-up and no pull-down	n/a	
	PC2	ADC1_IN12	Analog mode	No pull-up and no pull-down	n/a	
	PC3	ADC1_IN13	Analog mode	No pull-up and no pull-down	n/a	
	PA2	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	
	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	MCO [STM32F103CBT6_PA8]
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC8	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC9	TIM3_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM10	PB8	TIM10_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM13	PF8	TIM13_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PB15	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USART1_Rx_Clav
	PB6	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USART1_Tx_Clav
USART3	PB14	USART3_DE	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USART3_Tx_Rpi
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USART3_Rx_Rpi
Single Mapped	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
Signals	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_MDC [LAN8742A-CZ-TR_MDC]
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_REF_CLK [LAN8742A-CZ-TR_REFCLK0]
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_RXD0 [LAN8742A-CZ-TR_RXD0]
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_RXD1 [LAN8742A-CZ-TR_RXD1]
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_TXD1 [LAN8742A-CZ-TR_TXD1]
	PA8	USB_OTG_FS_SOF	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USB_SOF [TP1]
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USB_DM
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USB_DP
	PD6	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_TX_EN [LAN8742A-CZ-TR_TXEN]
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	RMII_TXD0 [LAN8742A-CZ-TR_TXD0]
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	SW0
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USER_Btn [B1]
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD1 [Green]
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_PowerSwitchOn [STMPS2151STR_EN]
	PG7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USB_OverCurrent [STMPS2151STR_FAULT]

8.2. DMA configuration

DMA request	Stream	Direction	Priority
USART3_RX	DMA1_Stream1	Peripheral To Memory	Medium *
USART3_TX	DMA1_Stream3	Memory To Peripheral	Medium *
ADC1	DMA2_Stream0	Peripheral To Memory	Low

USART3_RX: DMA1_Stream1 DMA request Settings:

Mode: Normal
 Use fifo: Disable
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Byte
 Memory Data Width: Byte

USART3_TX: DMA1_Stream3 DMA request Settings:

Mode: Normal
 Use fifo: Disable
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Byte
 Memory Data Width: Byte

ADC1: DMA2_Stream0 DMA request Settings:

Mode: **Circular ***
 Use fifo: Disable
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Half Word
 Memory Data Width: Half Word

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream1 global interrupt	true	0	0
DMA1 stream3 global interrupt	true	0	0
TIM1 trigger and commutation interrupts and TIM11 global interrupt	true	0	0
TIM3 global interrupt	true	0	0
TIM4 global interrupt	true	0	0
USART1 global interrupt	true	0	0
USART3 global interrupt	true	0	0
TIM8 update interrupt and TIM13 global interrupt	true	0	0
DMA2 stream0 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 capture compare interrupt	unused		
EXTI line[15:10] interrupts	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 stream1 global interrupt	false	true	true
DMA1 stream3 global interrupt	false	true	true
TIM1 trigger and commutation interrupts and TIM11 global interrupt	false	true	true
TIM3 global interrupt	false	true	true
TIM4 global interrupt	false	true	true
USART1 global interrupt	false	true	true
USART3 global interrupt	false	true	true
TIM8 update interrupt and TIM13 global interrupt	false	true	true
DMA2 stream0 global interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware						
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
CORTEX_M7 ✓	ADC1 ✓	TIM1 ✓	USART1 ✓			
DMA ✓		TIM3 ✓	USART3 ✓			
GPIO ⚠		TIM4 ✓				
NVIC ✓		TIM10 ✓				
RCC ✓		TIM11 ✓				
SYS ✓		TIM13 ✓				

10. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32f7_bsd1.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32f7_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32f7_svd.zip
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32f7_bsd1.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32f7_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32f7_svd.zip
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
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