FPGA Interface for Arcade Projects

This document will describe how you must design your game in order to interact with the JAMMA interface within the arcade cabinet.

1 What you need to know

You are being provided with a top-level verilog file that allows your game to interact with the arcade cabinet.

In order to do this, the signals used in your game must match the input signals in the top-level module. The signals are named in accordance with the JAMMA standard. Please note that all signals are preceded by an underscore ("_").

You must also add the .ucf file found Section 3 to your project for these signals to be assigned to the proper locations.

All signals coming from the JAMMA harness are ACTIVE LOW.

1.1 Joystick

The joystick can be thought of as four separate buttons: up, down, left and right.

	Player 1	Player 2
Function	Signal Name	Signal Name
Up	_1UP	_2UP
Down	_1DN	_2DN
Left	$_{ extsf{-}1} ext{LFT}$	_2LFT
Right	_1RGT	_2RGT

1.2 Action Buttons

Each player is allocated three buttons to use during gameplay.

	Player 1	Player 2
Function	Signal Name	Signal Name
Button 1	_1S1	_2S1
Button 2	_1S2	_2S2
Button 3	_1S3	_2S3

1.3 Player Select Buttons

The arcade cabinet features two buttons for selecting the number of players in a game.

Function	Signal Name
Select 1 Player	START1
Select 2 Players	START

2 Top-Level Verilog Module

```
'timescale 1ns / 1ps
// Module Name: arcade_wrapper
// Target Devices: Nexys3
// Description: Top-level JAMMA interface for EC551 arcade projects
//
// Revision:
// Revision 0.01 - File Created
module arcade_wrapper(
   input _2LFT,
input _2S3,
input _2DN,
input _2S2,
input _2UP,
   input .2S1,
input .START,
input .2RGT,
input .1LFT,
    input _1S3,
   input _1DN,
input _1S2,
input _1UP,
input _1S1,
    input _START1,
    input _1RGT,
    );
    // Put your code here:
end module \\
```

3 UCF File

Note for Doug: 1RGT signal on joystick has a faulty connection or switch (switch has a difficult time shifting from open to closed and as a result tends to get stuck in the "unpressed" state).

```
##JB
Net "_2LFT" LOC = K2 | IOSTANDARD = LVCMOS33; #Bank = 3, pin name = IO_L38P_M3DQ2,
   Sch name = JB1
Net "_2S3" LOC = K1 | IOSTANDARD = LVCMOS33; #Bank = 3, pin name = IO_L38N_M3DQ3,
    Sch name = JB2
Net ".2DN" LOC = L4 | IOSTANDARD = LVCMOS33; #Bank = 3, pin name = IO_L39P_M3LDQS,
    Sch name = JB3
Net "_2S2" LOC = L3 | IOSTANDARD = LVCMOS33; #Bank = 3, pin name = IO_L39N_M3LDQSN,
   Sch name = JB4
Net "_2UP" LOC = J3 | IOSTANDARD = LVCMOS33; #Bank = 3, pin name = IO_L40P_M3DQ6,
    Sch\ name\ =\ JB7
Net "_2S1" LOC = J1 | IOSTANDARD = LVCMOS33; #Bank = 3, pin name = IO_L40N_M3DQ7,
    Sch\ name\ =\ JB8
Net "START" LOC = K3 | IOSTANDARD = LVCMOS33; #Bank = 3, pin name =
    IO_L42N_GCLK24_M3LDM, Sch name = JB9
Net "_2RGT" LOC = K5 | IOSTANDARD = LVCMOS33; #Bank = 3, pin name =
   IO_L43N_GCLK22_IRDY2_M3CASN, Sch name = JB10
##JC
Net "_1LFT" LOC = H3 | IOSTANDARD = LVCMOS33; #Bank = 3, pin name =
   IO_L44N_GCLK20_M3A6, Sch name = JC1
Net "_1S3" LOC = L7 | IOSTANDARD = LVCMOS33; #Bank = 3, pin name = IO_L45P_M3A3, Sch
    name = JC2
Net "_1DN" LOC = K6 | IOSTANDARD = LVCMOS33; #Bank = 3, pin name = IO_L45N_M3ODT,
    Sch name = JC3
Net "_1S2" LOC = G3 | IOSTANDARD = LVCMOS33; #Bank = 3, pin name = IO_L46P_M3CLK,
    Sch\ name\ =\ JC4
Net "_1UP" LOC = G1 | IOSTANDARD = LVCMOS33; #Bank = 3, pin name = IO_L46N_M3CLKN,
    Sch name = JC7
Net "_1S1" LOC = J7 | IOSTANDARD = LVCMOS33; #Bank = 3, pin name = IO_L47P_M3A0, Sch
    name = JC8
\label{eq:new_constraints} \mbox{Net ".START1" LOC} = \mbox{J6} \ | \mbox{IOSTANDARD} = \mbox{LVCMOS33}; \ \#\mbox{Bank} = \mbox{3}, \ \mbox{pin name} = \mbox{IO\_L47N\_M3A1},
    Sch name = JC9
Net "_1RGT" LOC = F2 | IOSTANDARD = LVCMOS33; #Bank = 3, pin name = IO_L48P_M3BA0,
    Sch name = JC10
```