Manual of compact models for

Ferroelectric Tunnel Junction (FTJ)

SPINLIB: Model FTJ

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I.   General Introduction

With the CMOS fabrication node reach nanometre level (e.g. below 90 nm), the static power increasingly plays a major role of whole power dissipation due to soaring leakage current in memory and logic chip. Emerging non-volatile technologies can keep storage data retention without power supply, thus promising to relieve this issue. Ferroelectric tunnelling junction (FTJ) is recently considered as a potential candidate for next generation non-volatile memory and logic (NVM and NVL) thanks to its excellent performance. A typical FTJ is composed of a ferroelectric ultrathin barrier sandwiched between two different electrodes. As shown schematically in Fig. 1(a), The proposed FTJ structure is fabricated with multilayers including $Co/BaTiO_3(2nm)/La_{0.67}Sr_{0.33}MnO_3(30nm)(Co/BTO/LSMO)$. As a voltage-controlled device, only an external voltage larger than threshold is required to switch polarization orientation of ferroelectric barrier. The reversal of polarization causes the change of barrier potential profile, resulting in the switching of tunnel electroresistance (TER) (see Fig. 1(b)).
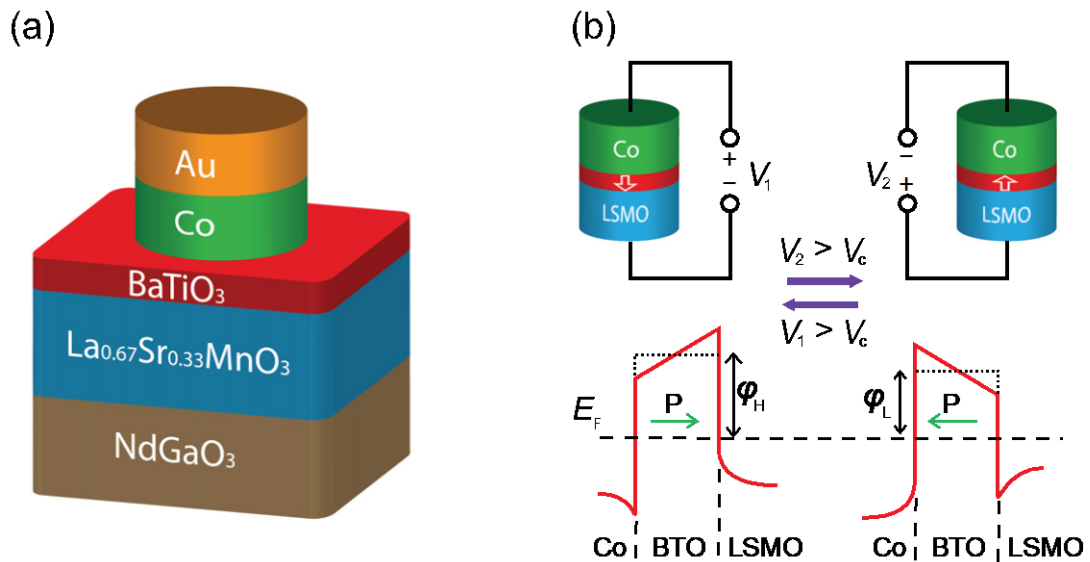

Fig. 1. (a) Schematic viewgraph of a Co/BTO/LSMO FTJ: ferroelectric ultrathin film BaTiO3 is sandwiched between Co and $La_{0.67}Sr_{0.33}MnO_3$, NdGaO3 is used as substrate.

(b) FTJ switching mechanism: when the applied voltage is larger than coercive voltage (V_c), the polarization orientation is switched, resulting in the modulation of barrier potential profile (especially in φ_H and φ_L) and the change of tunnel resistance. (Note that the variation of barrier thickness induced by converse piezoelectric effect is not displayed in this figure.)

Programmed with Verilog-A language

Validated in Cadence 6.1.5 Spectre, CMOS Design Kit 40nm.

II.   Files Provided

Decompress the compressed file Model_BTOFTJ.zip which you have downloaded (Attention: Never rename the model out of Cadence, or a hierarchical problem would occur.), and a folder named "Model_BTOFTJ" will appear, which consists of two subfolders and three files. Three files are Cadence configuration files and don't matter.

The first subfolder named "model_BTOFTJ" includes a script file of the type of Verilog-A, which is the source code of this model, and a symbol file.

Fig. 2 shows the symbol of the developed electrical model on Cadence platform. Three terminals are defined: 'T1' and 'T2' are real terminals corresponding to Co and LSMO electrodes, respectively. 's' is a virtual terminal which outputs the value of s_{OFF} ranging from 0 to 1. The arrows show the polarization orientations corresponding to ON and OFF states. They also indicate the polarities of the applied voltage for two switching directions. If the potential of 'T1' is higher than that of 'T2', the FTJ is programmed towards OFF state and conversely towards ON state.
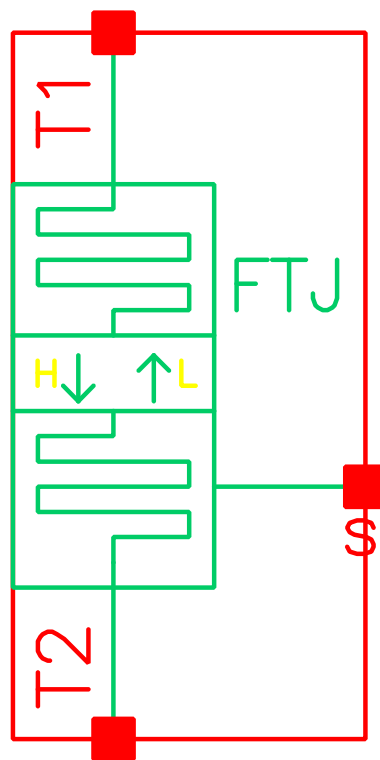

Fig. 2. The electrical model of the FTJ.

The second subfolder named "simu_BTOFTJ" contains two subfolders named "schematicis" and "pwlFiles". The role of them is to realize the single-cell simulation for validating the function of the presented FTJ electrical model. The schematic in "schematicis" shown in Fig .3, where a user-defined pulse in "pwlFiles" is applied to a single FTJ. The current and s_{OFF} are monitored at terminals 'T1' and 's', respectively. The results of pinched I-V hysteresis loop and transient simulations are presented in

Fig. 5 and Fig. 6.

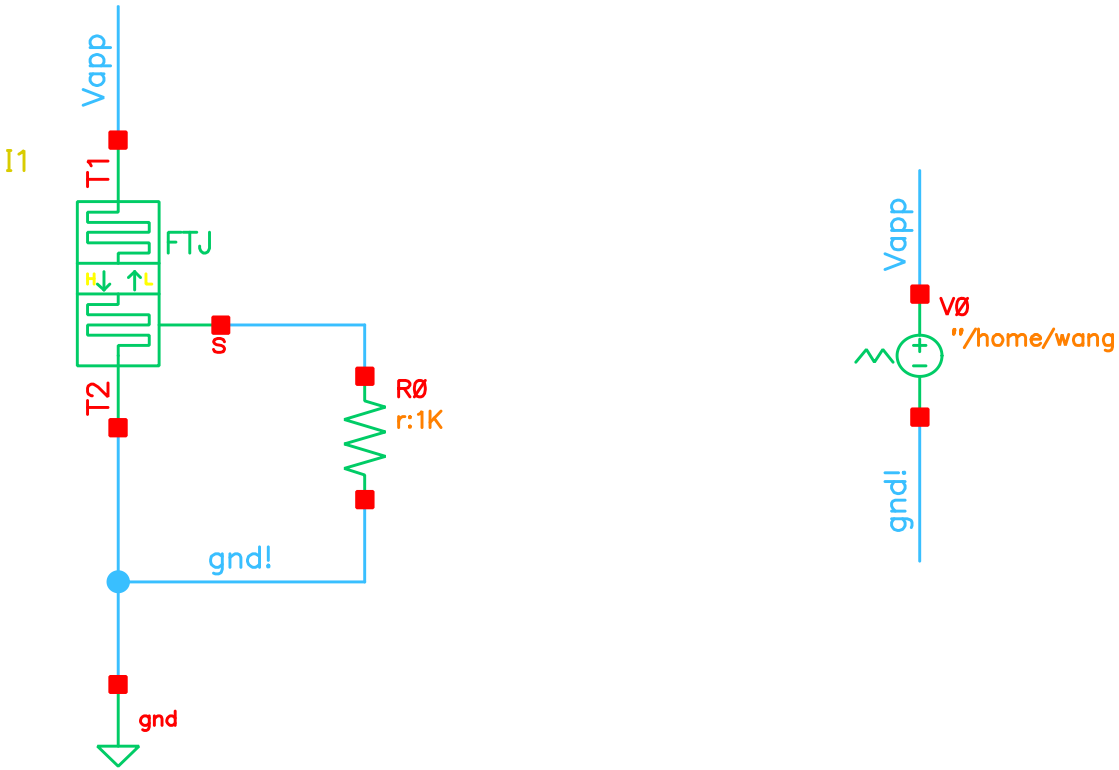
Fig. 3 Schematic for the single-cell simulation. The simulation results are provided in Section. III.
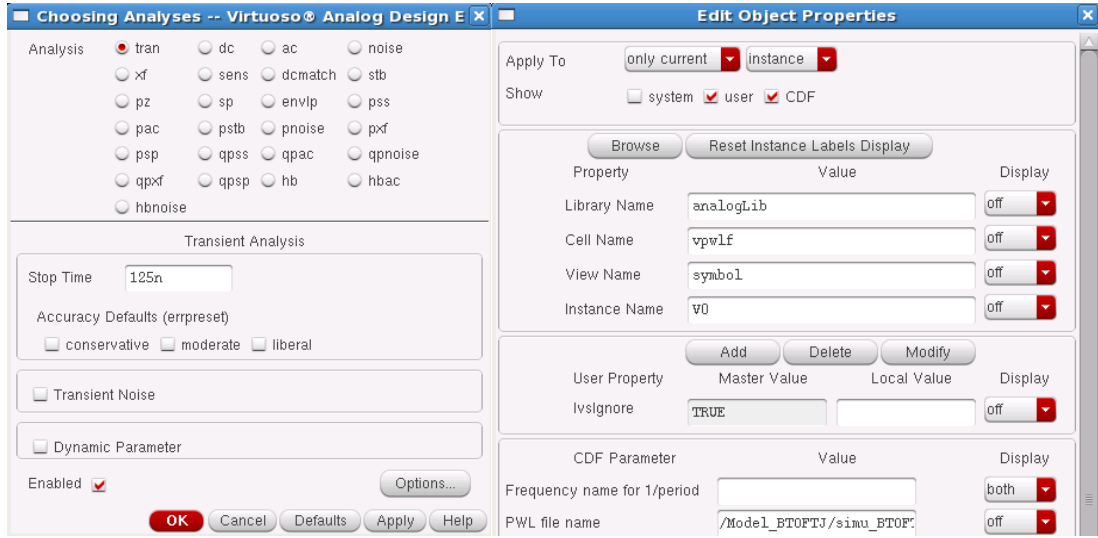
III. Simulations Results

Fig. 4. The set of simulation.

The simulation type can be selected from the "Analysis" part of the ADE L panel. "tran" represent transient. The "Stop Time 125n" means the simulation process will last 125 nanoseconds. The applied pulse can be edited at "Object Properties" of Vsourse "vpwlf" by putting the detailed address of the waveform file in "pwlFiles" folder into the box of PWL file name. For example, "…\Model_BTOFTJ\simu_BTOFTJ\pwlFiles\Transient.txt" means the transient simulation

III. A. Pinched I-V Hysteresis Loop

Pinched I-V hysteresis loop is regarded as the typical characteristic of a memristor, is reproduced by simulation results shown in Fig. 5. These results are obtained by sweeping voltage from –2.5 V to 2.5 V and then back to –2.5 V (as the arrows in Fig. 5 (a) and (d)), at a 0.1 V interval. The initial domain configuration is set to S_{OFF} = 0.9999. The simulation time step is set to $1/(10f)$, where f is the sweeping frequency. The barrier thickness is successively set to 2 nm and 1.6 nm during the simulation. The other parameters are provided in Section. IV.

Fig. 5 (a) and (b) show the comparison of I-V loops between different sweeping frequencies (1 kHz and 100 Hz), while (a) and (c) show the comparison between different barrier thicknesses (2.0 nm and 1.6 nm). Fig. 5 (d) is the same results as Fig. 5 (a) in log scale. It is seen that the profile of I-V loop curve can be adjusted by changing the sweeping frequency and barrier thickness. The switching voltage decreases as the sweeping frequency or barrier thickness decreases, as expected by Merz's law. Moreover, the result in Fig. 5 (a) is in relative good agreement with the experiment measurement.
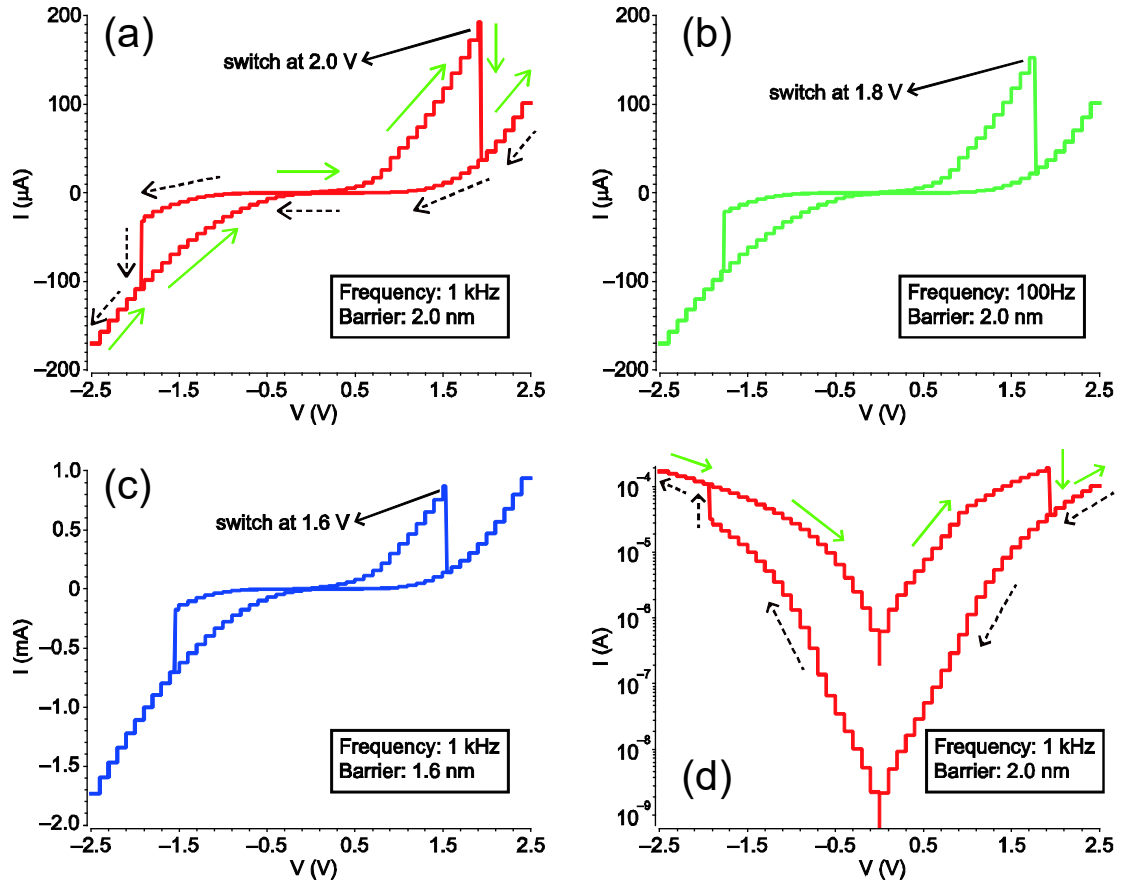
Fig. 5. I-V pinched hysteresis loops simulated with the proposed model.

III.B. The Transient Simulation

The transient simulation is performed to demonstrate the domain growth and resistance variation under the action of a user-defined pulse, as shown in Figure Fig. 6. The purple line represents the applied voltage pulse. The green line shows the domain growth of the FTJ. While the red line indicates the current throughout the FTJ.

During 5~15ns, a negative write pulse of –4 V sets the FTJ to the fully ON state, which is confirmed by s_{OFF} = 0. During 25~35 ns, a positive write pulse of 3.75 V activates the domain nucleation and domain wall propagation. During the domain nucleation, the FTJ is still at fully ON state and thus the resistance does not change, which is verified by an invariable current at 25~27.8 ns of Fig. 6 (c). Then, during 45~125 ns, two negative and two positive write pulses with an amplitude of 3.25 V are successively applied to program the FTJ. As expected, the back-and-forth growth of the domain can be clearly seen. In the whole simulation, each write pulse is followed by a read pulse of 0.1 V, it is seen that the read current increases or decreases with the decrease or increase of s_{OFF}. These results validate the voltage-controlled memristive behavior of the FTJ.
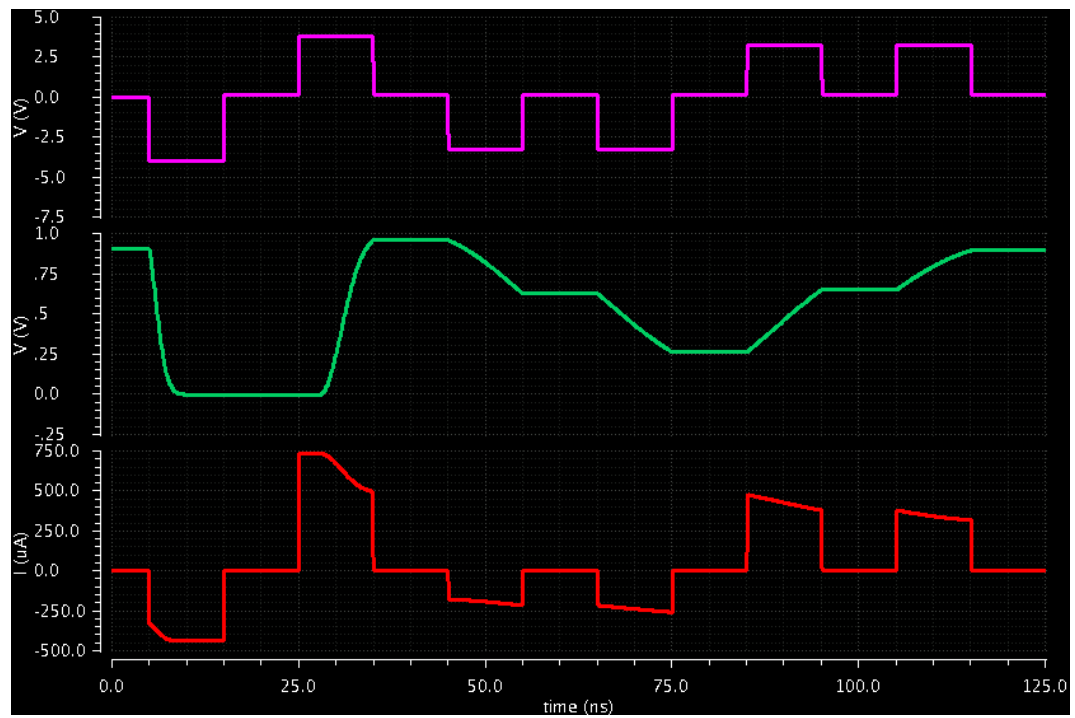
Fig. 6. The waveforms of the Transient simulation results.

IV. Device Parameters

IV. A. CDF

In order to describe the parameters and attributes of the parameters of individual component and libraries of component, we use the Component Description Format (CDF). It facilitates the application independent on cellviews, and provides a Graphical User Interface (the Edit Component CDF form) for entering and editing component information.

Fig. 7. Configuration of the CDF parameters

IV. B. Size Parameters

Parameters	Description	unit	Default value
tB	Barrier thickness	nm	2
r	Junction surface radius	nm	175

IV. C. Simulation environment parameters

Parameters	Description	unit	Default value
Δt	Time step for the simulation	ps	100
s_0	Initial fraction of the OFF-state domain	/	5×10^{-5}

T	Temperature	K	300

IV. D. Parameters for the dynamic switching memristive models

Parameters	Description	unit	Default value
U_N	Creep energy barrier for the domain	eV	0.67
U_P	Creep energy barrier for the domain wall	eV	0.52
τ_{0N}	Attempt time of the domain nucleation	s	2.8×10^{-15}
τ_{0P}	Attempt time of the domain wall	s	9×10^{-14}

IV. E. Parameters for the tunneling resistance model

Parameters	Description	unit	Default value	
			ON state	OFF state
φ_1	Barrier potential height at LSMO/BTO interface	V	0.53	0.678
φ_2	Barrier potential height at Co/BTO interface	V	1.014	0.978
m	Effective electron mass	me	0.437	0.931
F_1	Scaling factor the FNT model for	/	3.549×10^{-4} for V > 0 3.273×10^{-4} for V < 0	2.6×10^{-3} for V > 0 1.2×10^{-3} for V < 0
F_2	Scaling factor for the FNT model	/	9.41×10^{-2} for V > 0 1.2×10^{-3} for V < 0	0.7608 for V > 0 0.283 for V < 0

IV. F. General constants

Constant	Description	unit	Value
me	Free electron mass	kg	9.11×10^{-31}
e	Elementary charge	C	1.6×10^{-19}
$\hbar$	Reduced Planck constant	J·s	1.054×10^{-34}
kB	Boltzmann constant	J/K	1.38×10^{-23}
$E0$	Characteristic field	GV/m	1

Among them, only size parameters and simulation environment parameters are user-reconfigurable. Other parameters are assumed to be dependent on the fabrication process and cannot be modified.

V.   Conclusion

This document introduces the instructions and simulation results of the FTJ model, including four files totally. Pinched I-V hysteresis loop and Transient simulation circuits and waveforms have been provided. Additionally, CDF and device parameters have also been listed in the file to serve as a supplemental information. The model files can be utilized for practical EDA simulation.

VI.   References

[1] Z. Wang, W. Zhao, W. Kang, Y. Zhang, J. O. Klein, D. Ravelosona, and C. Chappert, "Compact modelling of ferroelectric tunnel memristor and its use for neuromorphic simulation," Appl. Phys. Lett., vol. 104, no. 5, pp. 053505, 2014. DOI: 10.1063/1.4864270

[2] Z. Wang, W. Zhao, W. Kang, A. Bouchenak-Khelladi, Y. Zhang, Y. Zhang, J. O. Klein, D. Ravelosona, and C. Chappert, "A physics-based compact model of ferroelectric tunnel junction for memory and logic design," J. Phys. D: Appl. Phys., vol. 47, no. 4, pp. 045001, 2014. DOI: 10.1088/0022-3727/47/4/045001

[3] Zhaohao Wang. Compact modeling and circuit design based on ferroelectric tunnel junction and spin-Hall-assisted spin-transfer torque. Thesis, Universite Paris-Saclay, 2015.