

CSE 205: DIGITAL LOGIC DESIGN

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TEXTBOOK

- Digital Design (5th Edition)
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COMBINATIONAL LOGIC

- Combinational Logic:
 - Output depends only on current input
 - Has no memory



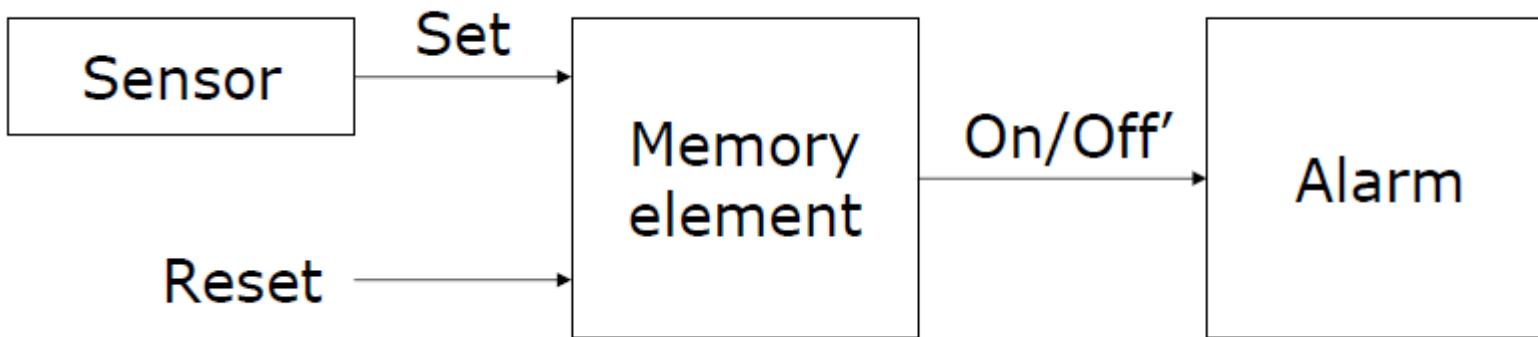
SEQUENTIAL LOGIC

- Sequential Logic:
 - Output depends not only on current input but also on past input values, e.g., design a counter
 - Need some type of memory to remember the past input values



ALARM CONTROL SYSTEM

- Suppose we wish to construct an alarm circuit such that the output remains active (on) even after the sensor output that triggered the alarm goes off
- The circuit requires a memory element to remember that the alarm has to be active until a reset signal arrives



SEQUENTIAL CIRCUITS

- Consist of a combinational circuit to which storage elements are connected to form a feedback path
- State: the state of the memory devices now, also called current state
- Next states and outputs are functions of inputs and present states of storage elements

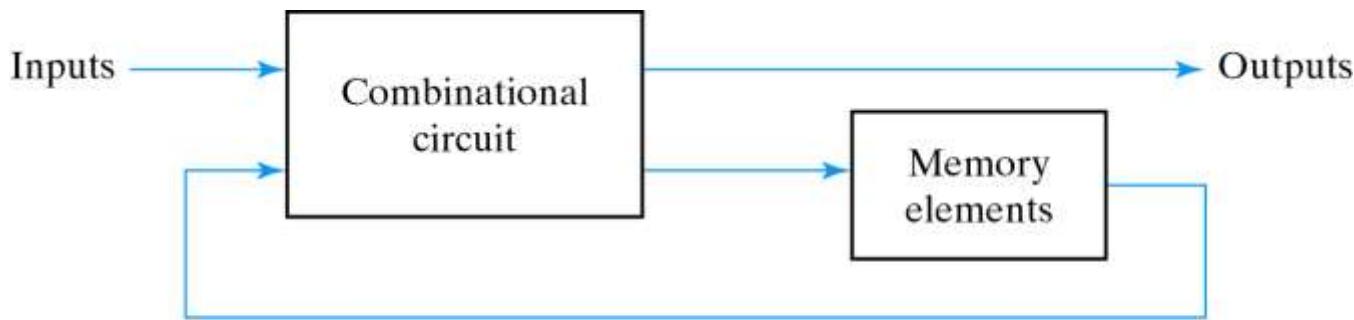


Fig. 5-1 Block Diagram of Sequential Circuit

TWO TYPES OF SEQUENTIAL CIRCUITS

- Synchronous sequential circuit
 - circuit output changes only at some discrete instants of time.
 - Synchronized by a periodic train of clock pulses
 - Much easier to design (preferred design style)
- Asynchronous sequential circuit
 - circuit output can change at **any** time (clockless)
 - May have better performance but hard to design



SYNCHRONOUS SEQUENTIAL CIRCUITS

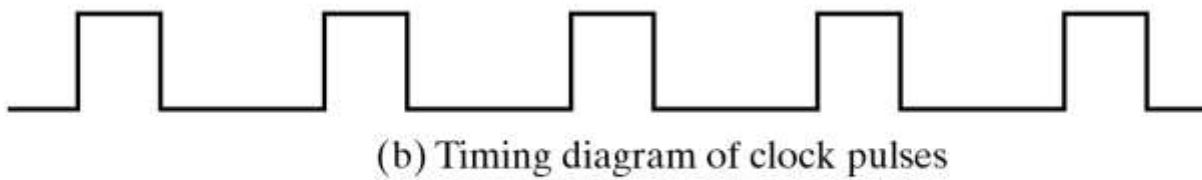
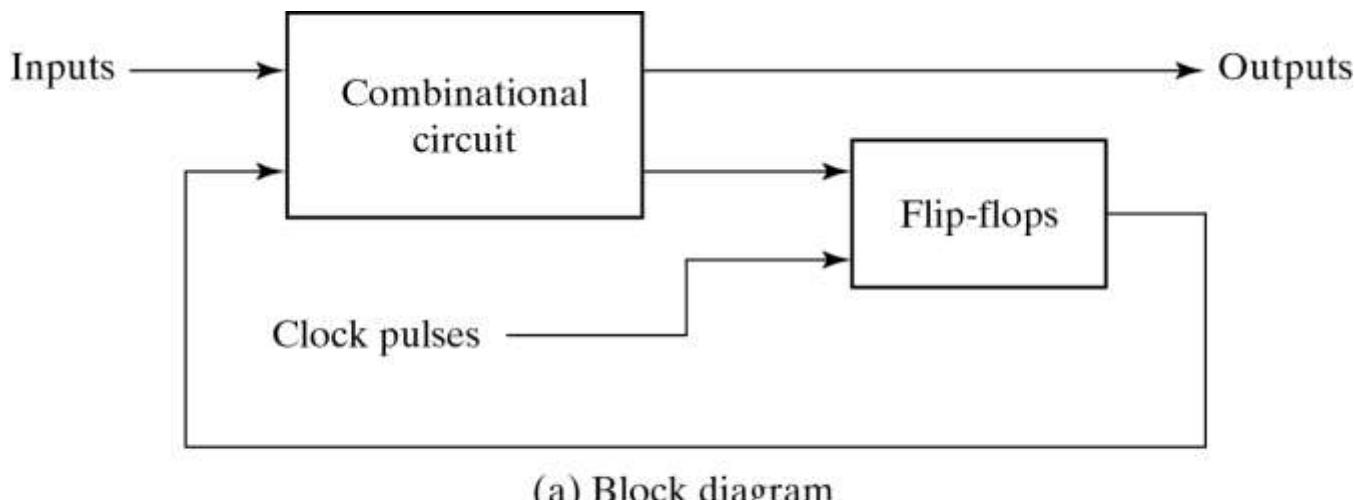


Fig. 5-2 Synchronous Clocked Sequential Circuit

MEMORY ELEMENTS

- A digital circuit that can maintain a binary state indefinitely, until directed by an input signal to switch states
- Differences among different types of storage elements depends on
 - The number of inputs they possess
 - The manner in which the inputs affect the binary state



MEMORY ELEMENTS

- Latch - a level-sensitive memory element
 - SR latches
 - D latches
- Flip-Flop - an edge-triggered memory element
 - Master-slave flip-flop
 - Edge-triggered flip-flop
- RAM and ROM - a mass memory element



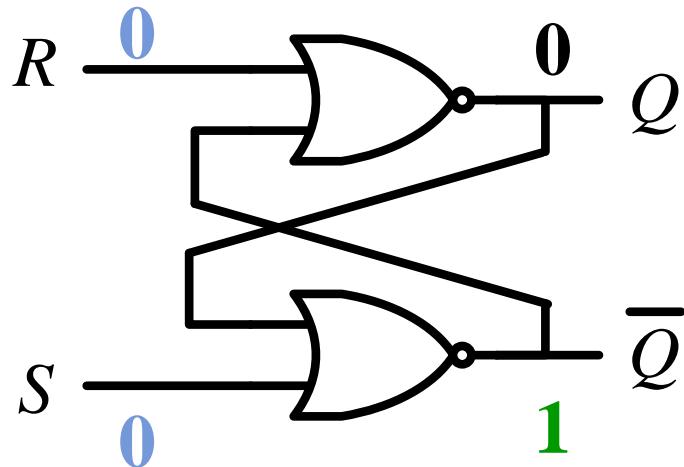
LATCHES

- A latch is binary storage element
- Can store a 0 or 1
- The most basic memory
- Easy to build
- Built with gates (NORs, NANDs, NOT)



LATCHES

- ## ○ SR Latch

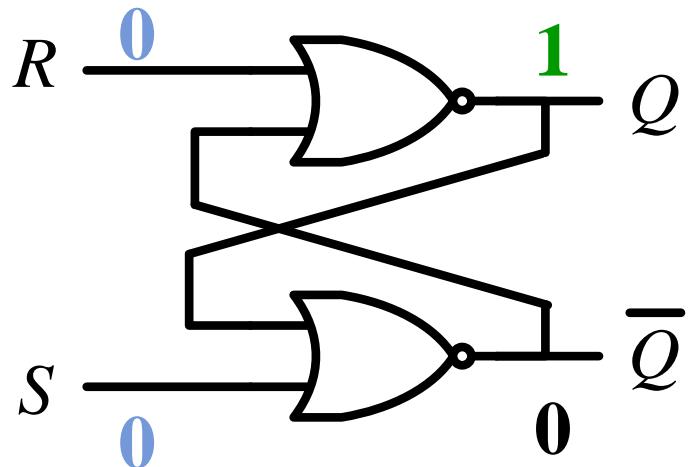


Initial Value

$$Q = Q_0$$

LATCHES

- SR Latch



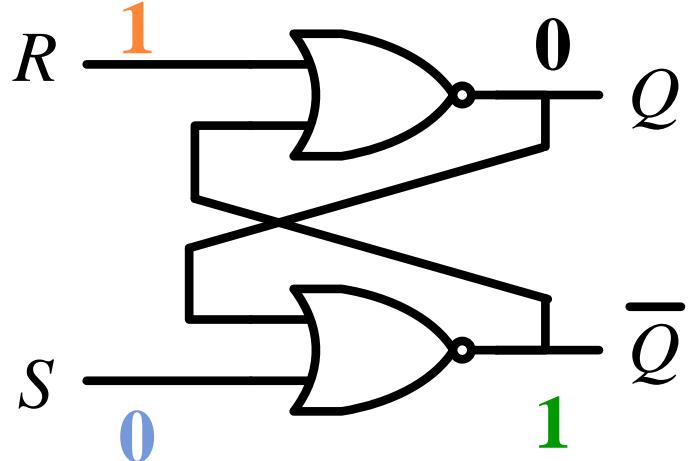
S	R	Q_0	Q	Q'
0	0	0	0	1
0	0	1	1	0

$$Q = Q_0$$
$$Q' = \bar{Q}_0$$



LATCHES

- SR Latch



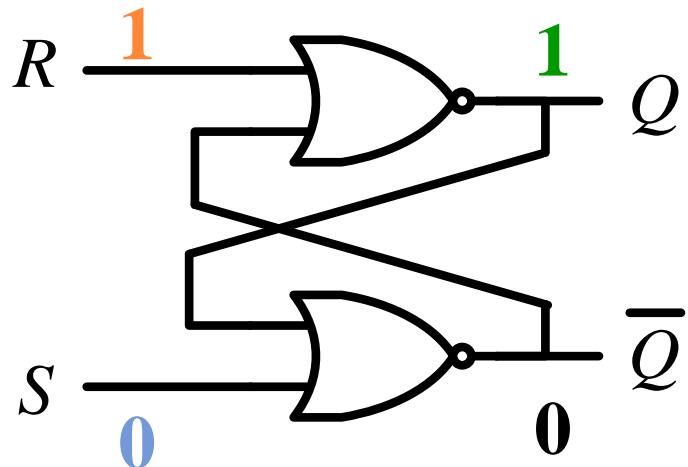
S	R	Q_0	Q	Q'
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1

$\} Q = Q_0$
 $Q = 0$



LATCHES

- SR Latch



S	R	Q_0	Q	Q'
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1
0	1	1	0	1

$Q = Q_0$

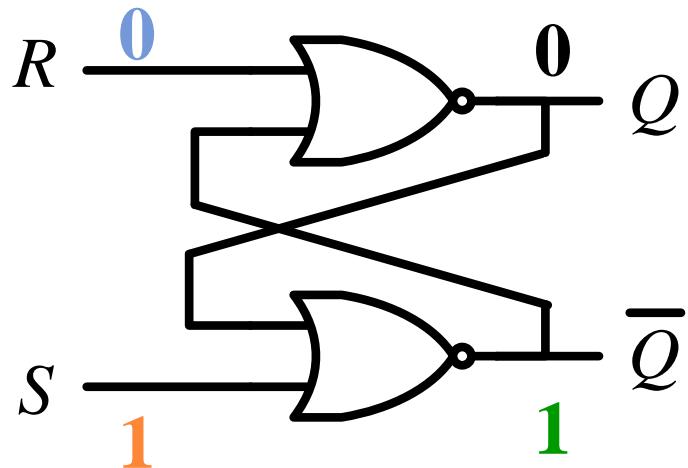
$Q = 0$

$Q = 0$



LATCHES

- SR Latch



S	R	Q_0	Q	Q'
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0

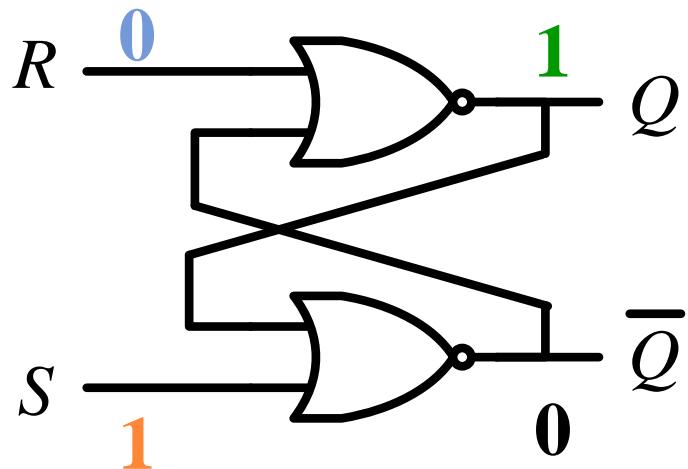
Annotations on the right side of the table indicate the state of Q based on the initial value Q_0 :

- $Q = Q_0$ (for rows 1, 2, 4, and 5)
- $Q = 0$ (for rows 3 and 6)
- $Q = 1$ (for rows 7, 8, and 9)



LATCHES

- SR Latch



S	R	Q_0	Q	Q'
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0

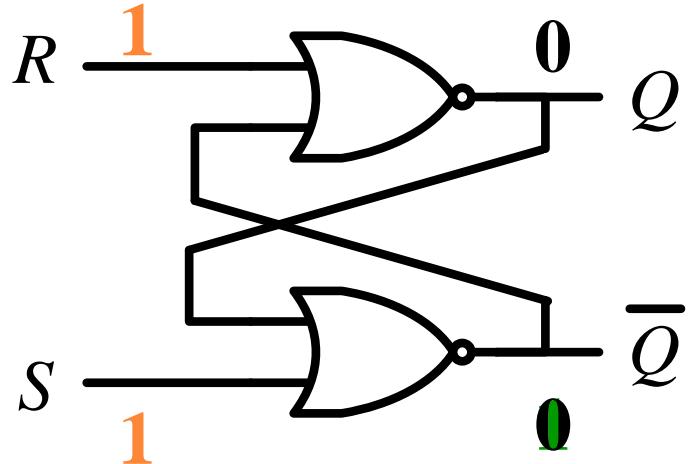
Annotations on the right side of the table explain the behavior based on the initial state Q_0 :

- If $Q_0 = 0$, then $Q = Q_0$ and $Q' = 1$.
- If $Q_0 = 1$, then $Q = 0$ and $Q' = Q_0$.
- If $Q_0 = 0$ and $R = 1$, then $Q = 0$ and $Q' = 1$.
- If $Q_0 = 1$ and $R = 1$, then $Q = 1$ and $Q' = 0$.
- If $Q_0 = 1$ and $S = 1$, then $Q = 1$ and $Q' = 0$.
- If $Q_0 = 0$ and $S = 1$, then $Q = 0$ and $Q' = 1$.



LATCHES

- SR Latch



S	R	Q_0	Q	Q'
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	0	0

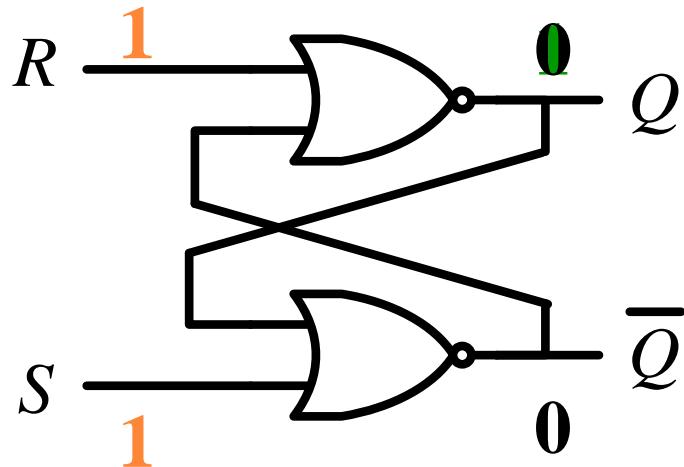
Annotations on the right side of the table indicate the state of Q based on the initial value Q_0 :

- $Q = Q_0$ (for rows 1, 2, 4, 5)
- $Q = 0$ (for rows 3, 6)
- $Q = 1$ (for rows 7, 8)
- $Q = Q'$ (for rows 0, 1, 2, 3, 4, 5, 6, 7, 8)



LATCHES

- SR Latch



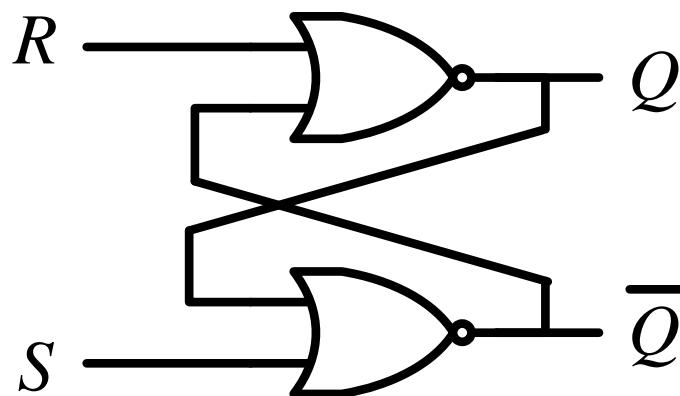
S	R	Q_0	Q	Q'
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	0	0
1	1	1	0	0

Annotations on the right side of the table explain the output states:

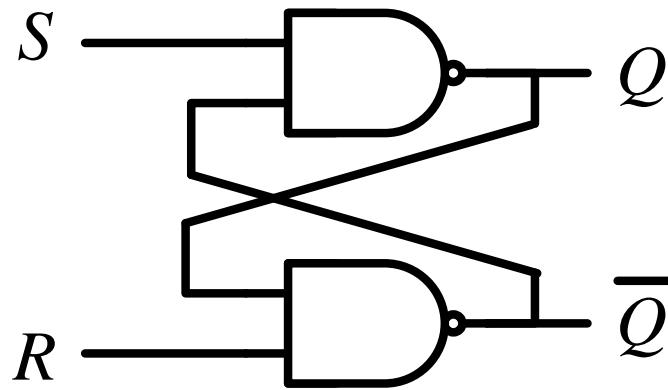
- $Q = Q_0$ (for rows 1, 2, 3, 4)
- $Q = 0$ (for rows 5, 6)
- $Q = 1$ (for rows 7, 8)
- $Q = Q'$ (for row 9)
- $Q = \bar{Q}'$ (for row 10)



SR LATCH

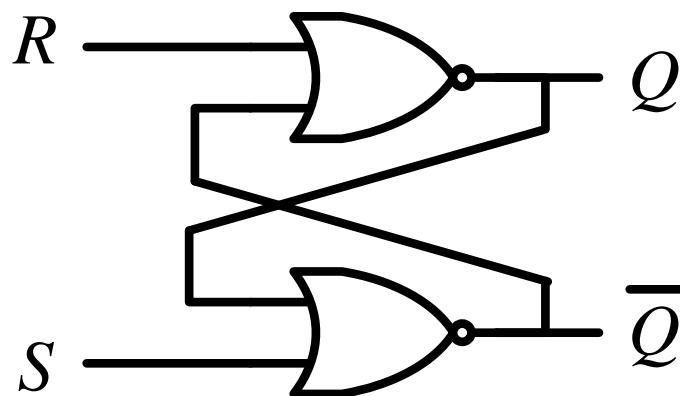


S	R	Q	
0	0	Q_0	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q=Q'=0$	Invalid

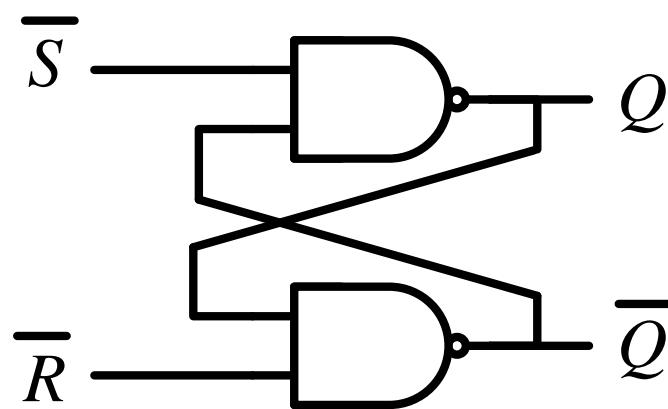


S	R	Q	
0	0	$Q=Q'=1$	Invalid
0	1	1	Set
1	0	0	Reset
1	1	Q_0	No change

SR LATCH



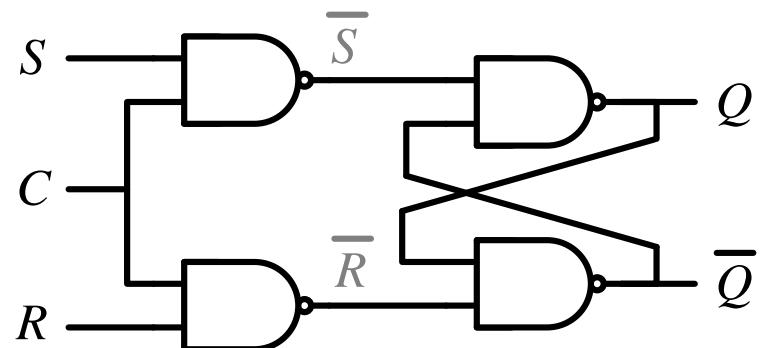
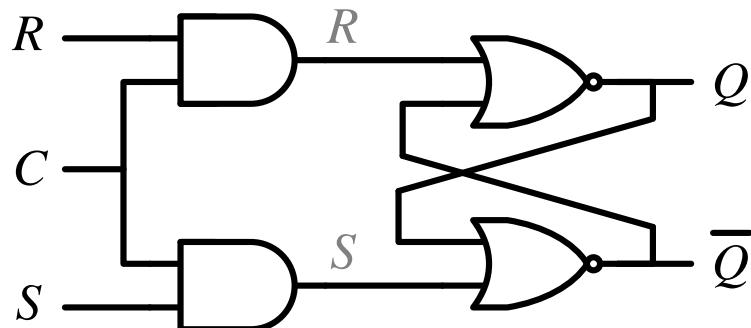
S	R	Q	
0	0	Q_0	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q=Q'=0$	Invalid



S'	R'	Q	
0	0	$Q=Q'=1$	Invalid
0	1	1	Set
1	0	0	Reset
1	1	Q_0	No change

CONTROLLED LATCHES

- SR Latch with Control Input



C	S	R	Q
0	x	x	Q_0
1	0	0	Q_0
1	0	1	0
1	1	0	1
1	1	1	$Q=Q'$

No change

No change

Reset

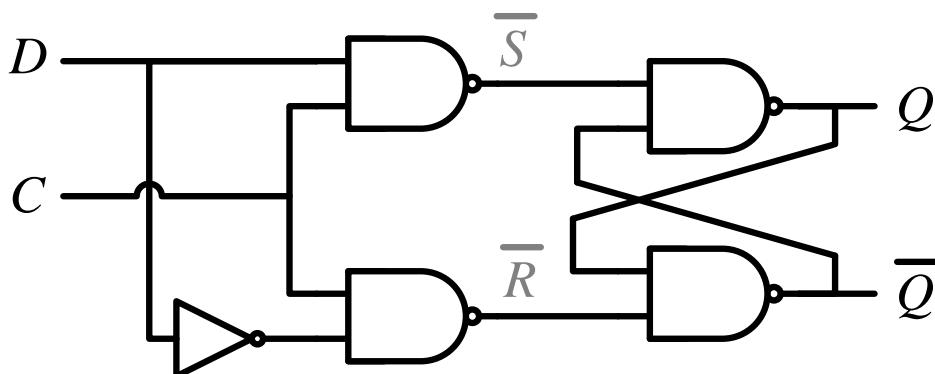
Set

Invalid



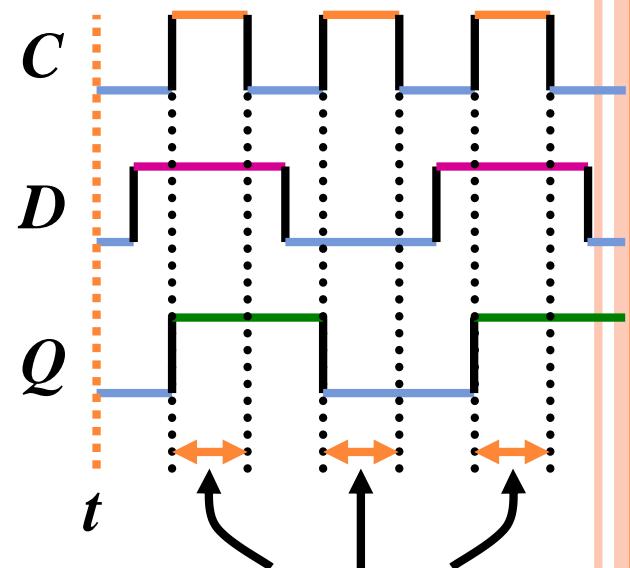
CONTROLLED LATCHES

- D Latch (D = Data)



C	D	Q	
0	x	Q_0	No change
1	0	0	Reset
1	1	1	Set

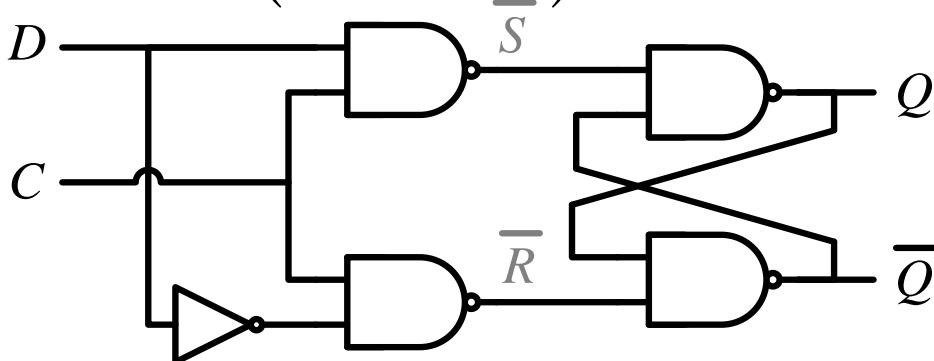
Timing Diagram



*Output may
change*

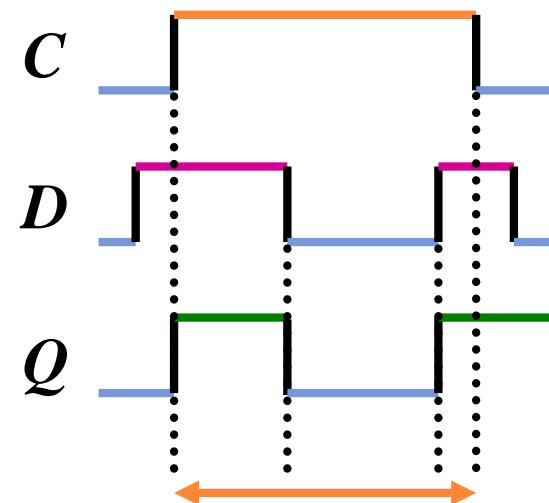
CONTROLLED LATCHES

- D Latch ($D = \text{Data}$)



C	D	Q	
0	x	Q_0	No change
1	0	0	Reset
1	1	1	Set

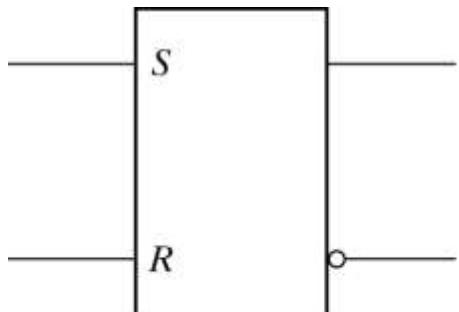
Timing Diagram



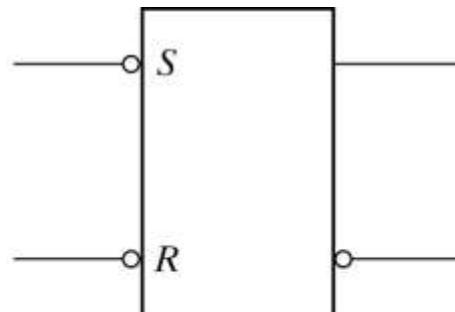
*Output may
change*



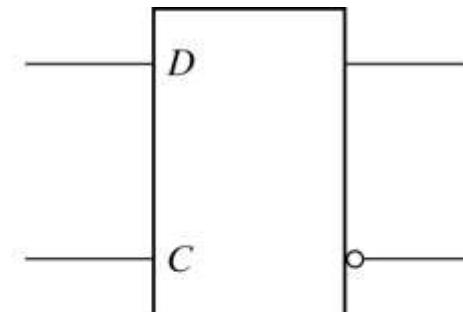
GRAPHIC SYMBOLS FOR LATCHES



SR



$\bar{S}\bar{R}$



D

Fig. 5-7 Graphic Symbols for Latches

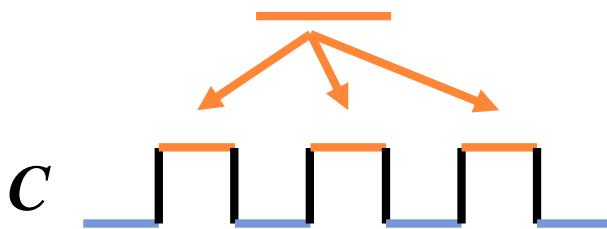
LEVEL VERSUS EDGE SENSITIVITY

- Since the output of the D latch is controlled by the level (0 or 1) of the clock input, the latch is said to be ***level sensitive***
 - All of the latches we have seen have been level sensitive
- It is possible to design a storage element for which the output only changes at the point in time when the clock changes from one value to another
 - Such circuits are said to be ***edge triggered***



FLIP-FLOPS

- Controlled latches are **level**-triggered

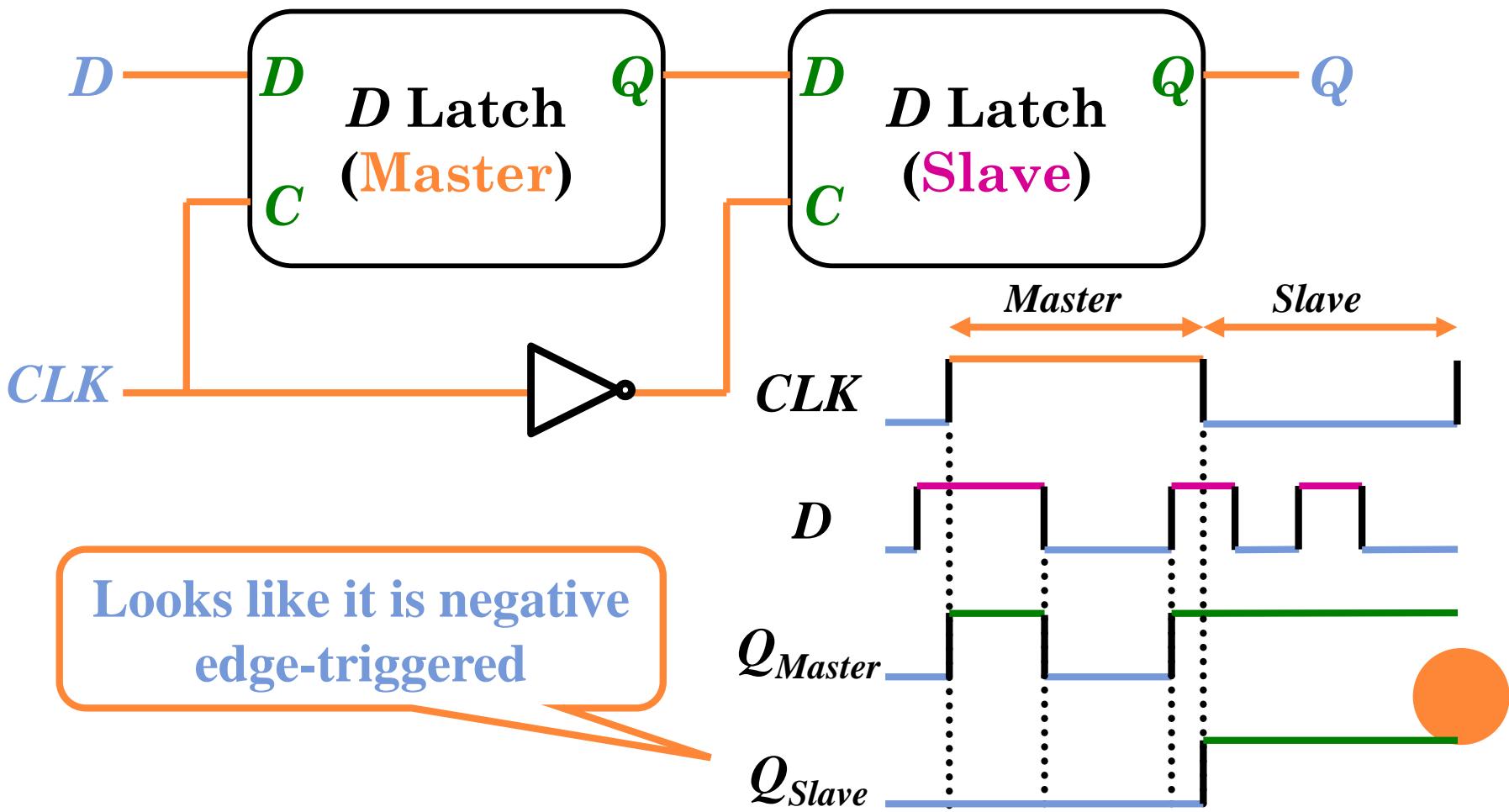


- Flip-Flops are **edge**-triggered



FLIP-FLOPS

- Master-Slave D Flip-Flop

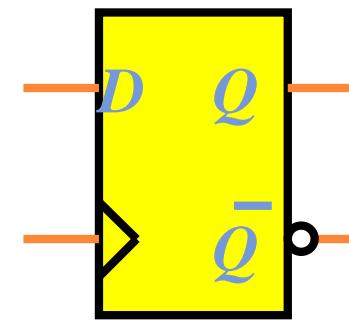
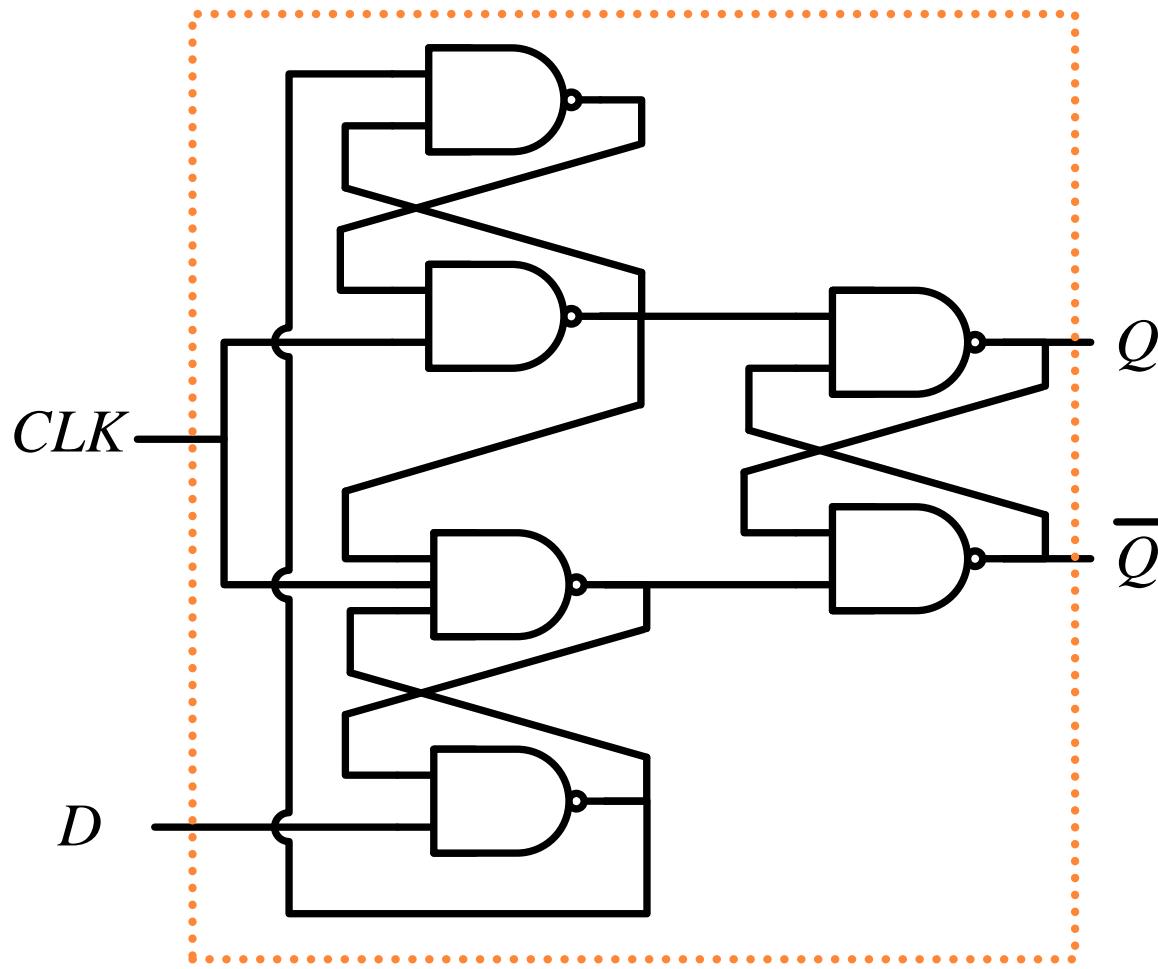


FLIP-FLOPS

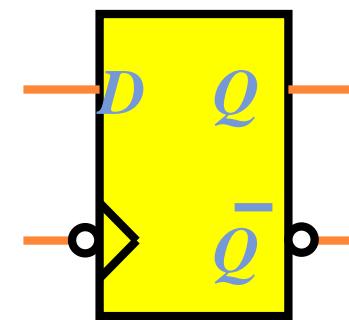
- The circuit samples the D input and changes its output at the negative edge of the clock, CLK .
- When the clock is 0, the output of the inverter is 1. The slave latch is enabled and its output Q is equal to the master output Y . The master latch is disabled ($CLK = 0$).
- When the CLK changes to high, D input is transferred to the master latch. The slave remains disabled as long as CLK is low. Any change in the input changes Y , but not Q .
- The output of the flip-flop can change when CLK makes a transition $1 \rightarrow 0$

FLIP-FLOPS

- Edge-Triggered D Flip-Flop

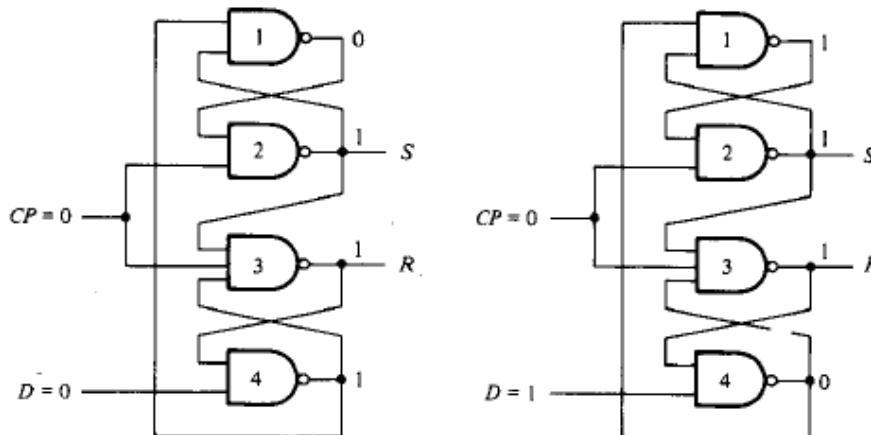


Positive Edge

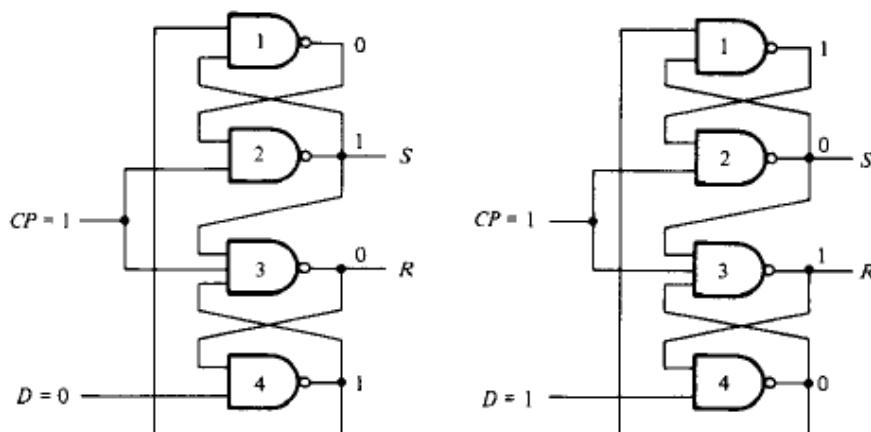


Negative Edge

FLIP-FLOPS: EDGE-TRIGGERED D FLIP-FLOP



(a) With $CP = 0$



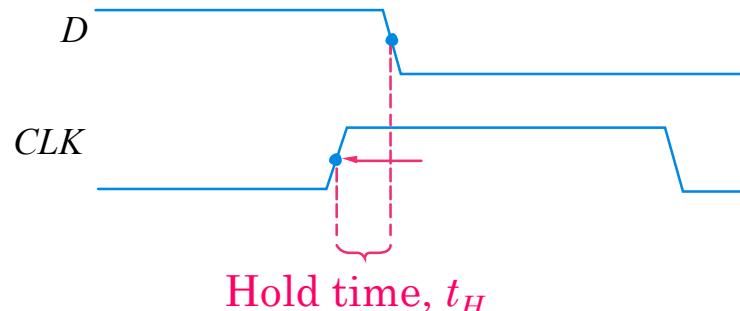
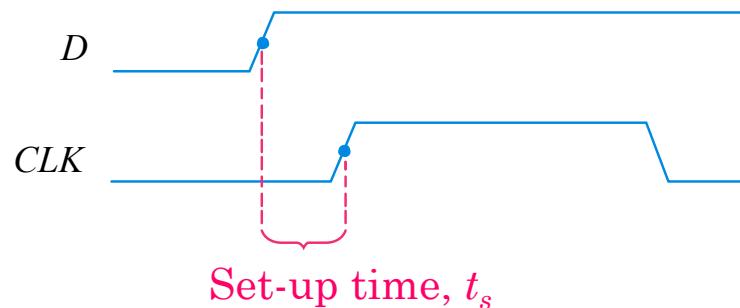
(b) With $CP = 1$

FLIP-FLOPS

Set-up time and **hold time** are times required before and after the clock transition that data must be present to be reliably clocked into the flip-flop.

Setup time is the minimum time for the data to be present *before* the clock.

Hold time is the minimum time for the data to *remain* after the clock.



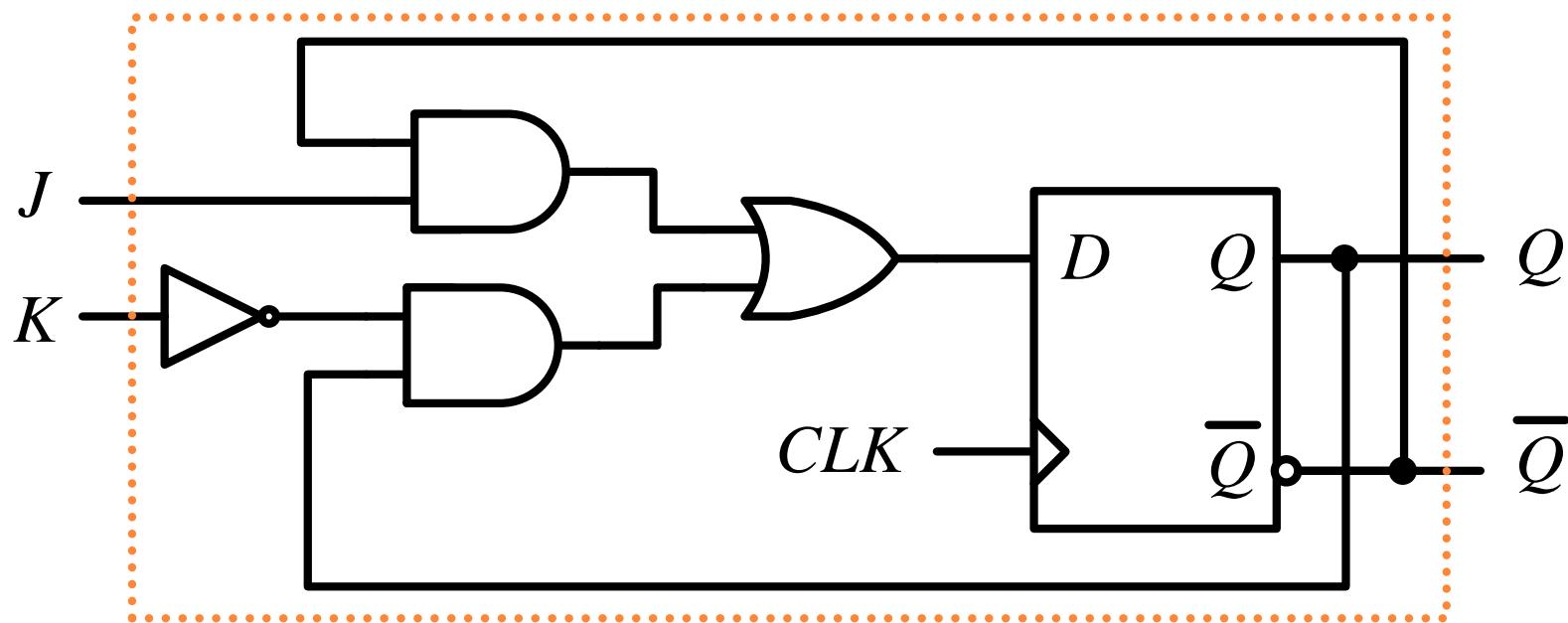
JK FLIP-FLOPS

- JK Flip-Flop : $D = JQ' + K'Q$
- When $J = 1$ and $K = 0$, $D = 1 \rightarrow$ next clock edge sets output to 1.
- When $J = 0$ and $K = 1$, $D = 0 \rightarrow$ next clock edge resets output to 0.
- When $J = 1$ and $K = 1$, $D = Q' \rightarrow$ next clock edge complements output.
- When $J = 0$ and $K = 0$, $D = Q \rightarrow$ next clock edge leaves output unchanged.

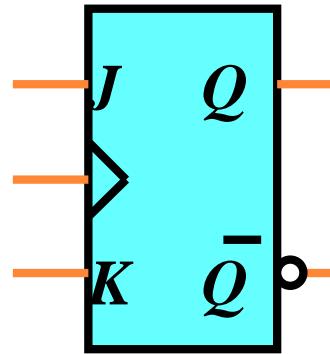


JK FLIP-FLOPS

- JK Flip-Flop

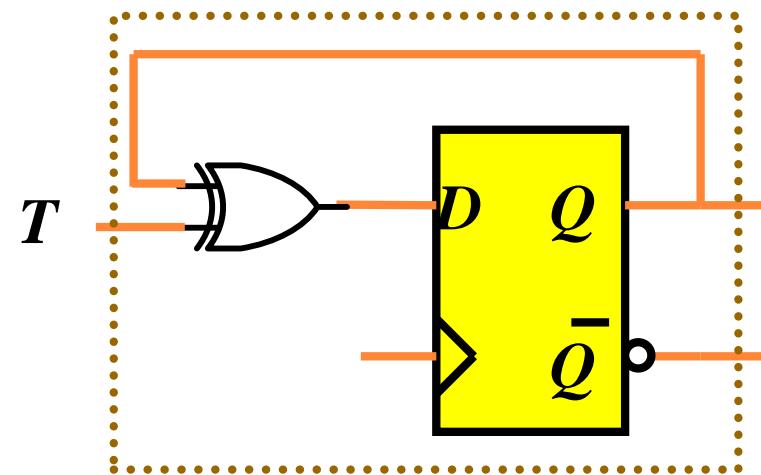
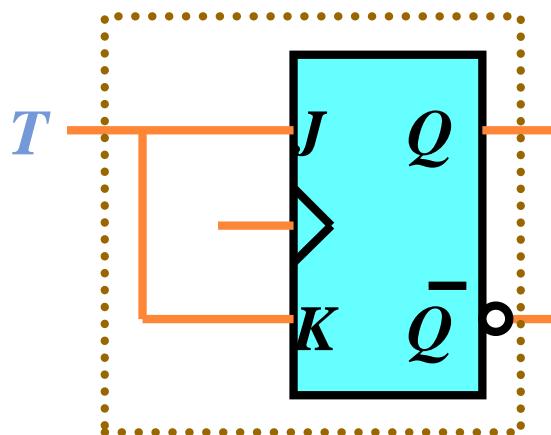


$$D = JQ' + K'Q$$



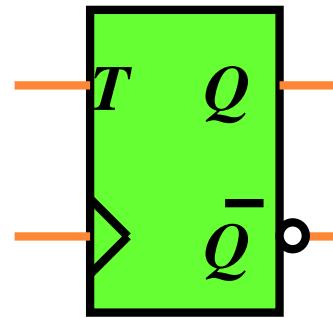
T FLIP-FLOPS

- T Flip-Flop

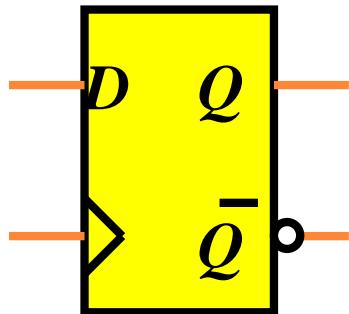


$$D = JQ' + K'Q$$

$$D = TQ' + T'Q = T \oplus Q$$



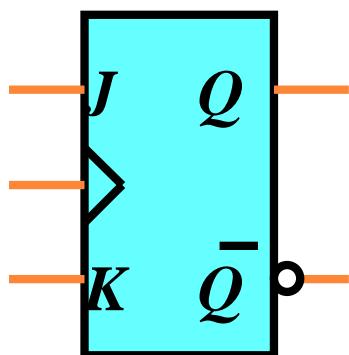
FLIP-FLOP CHARACTERISTIC TABLES



D	$Q(t+1)$
0	0
1	1

Reset

Set



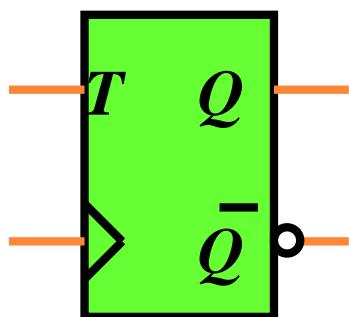
J	K	$Q(t+1)$
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$Q'(t)$

No change

Reset

Set

Toggle



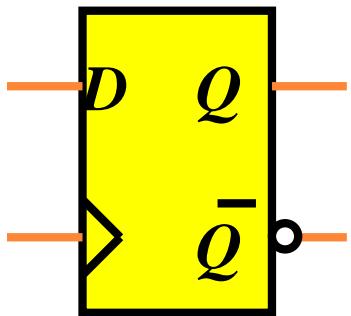
T	$Q(t+1)$
0	$Q(t)$
1	$Q'(t)$

No change

Toggle

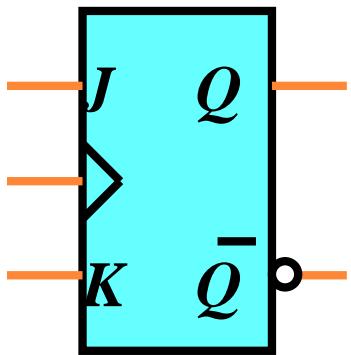


FLIP-FLOP CHARACTERISTIC EQUATIONS



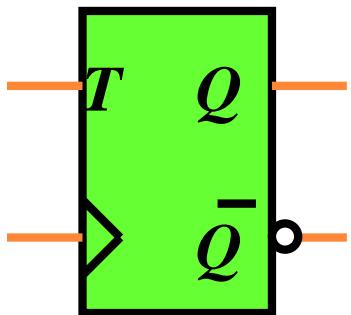
D	$Q(t+1)$
0	0
1	1

$$Q(t+1) = D$$



J	K	$Q(t+1)$
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$Q'(t)$

$$Q(t+1) = JQ' + K'Q$$



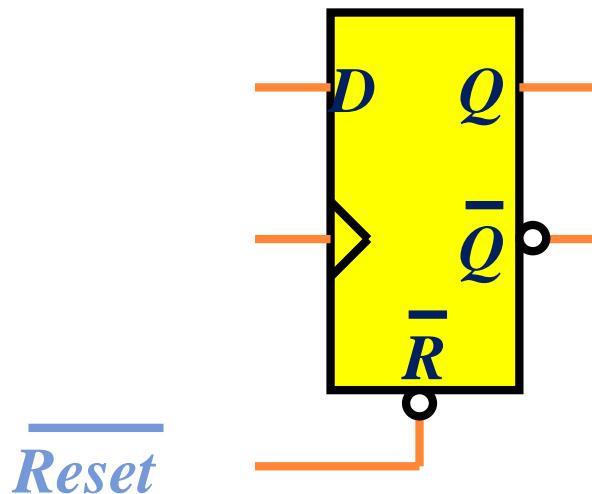
T	$Q(t+1)$
0	$Q(t)$
1	$Q'(t)$

$$Q(t+1) = T \oplus Q$$



FLIP-FLOPS WITH ASYNCHRONOUS/DIRECT INPUTS

- Asynchronous Reset

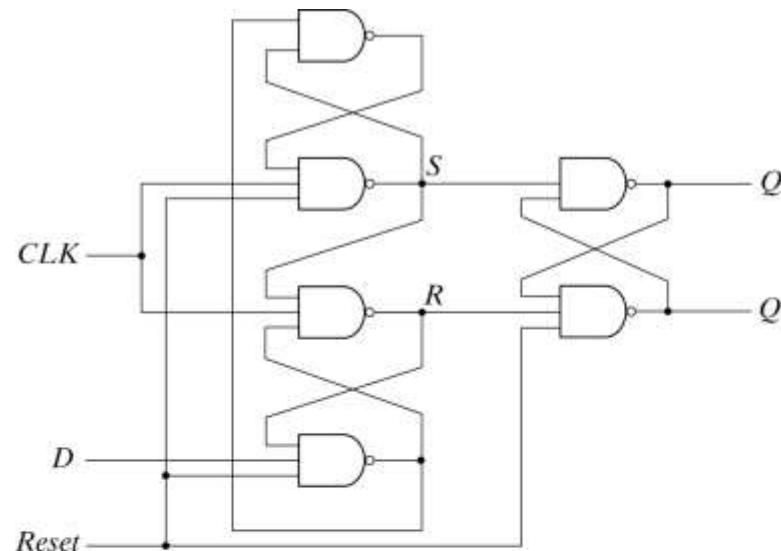


R'	D	CLK	$Q(t+1)$
0	x	x	0
1	0	↑	0
1	1	↑	1

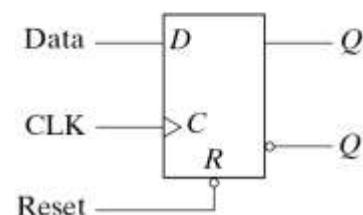


FLIP-FLOPS WITH DIRECT INPUTS

- Asynchronous Reset



(a) Circuit diagram



(b) Graphic symbol

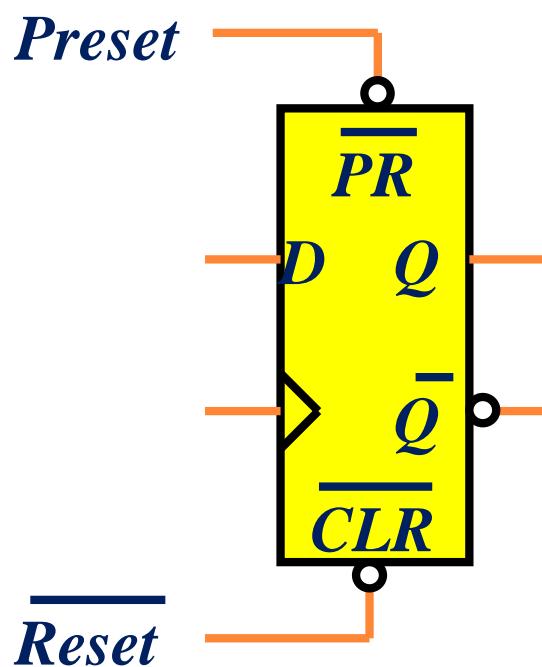
R	C	D	Q	Q'
0	X	X	0	1
1	↑	0	0	1
1	↑	1	1	0

(b) Function table

Fig. 5-14 D Flip-Flop with Asynchronous Reset

FLIP-FLOPS WITH DIRECT INPUTS

- Asynchronous Preset and Clear



PR'	CLR'	<i>D</i>	<i>CLK</i>	$Q(t+1)$
1	0	x	x	0
0	1	x	x	1
1	1	0	↑	0
1	1	1	↑	1

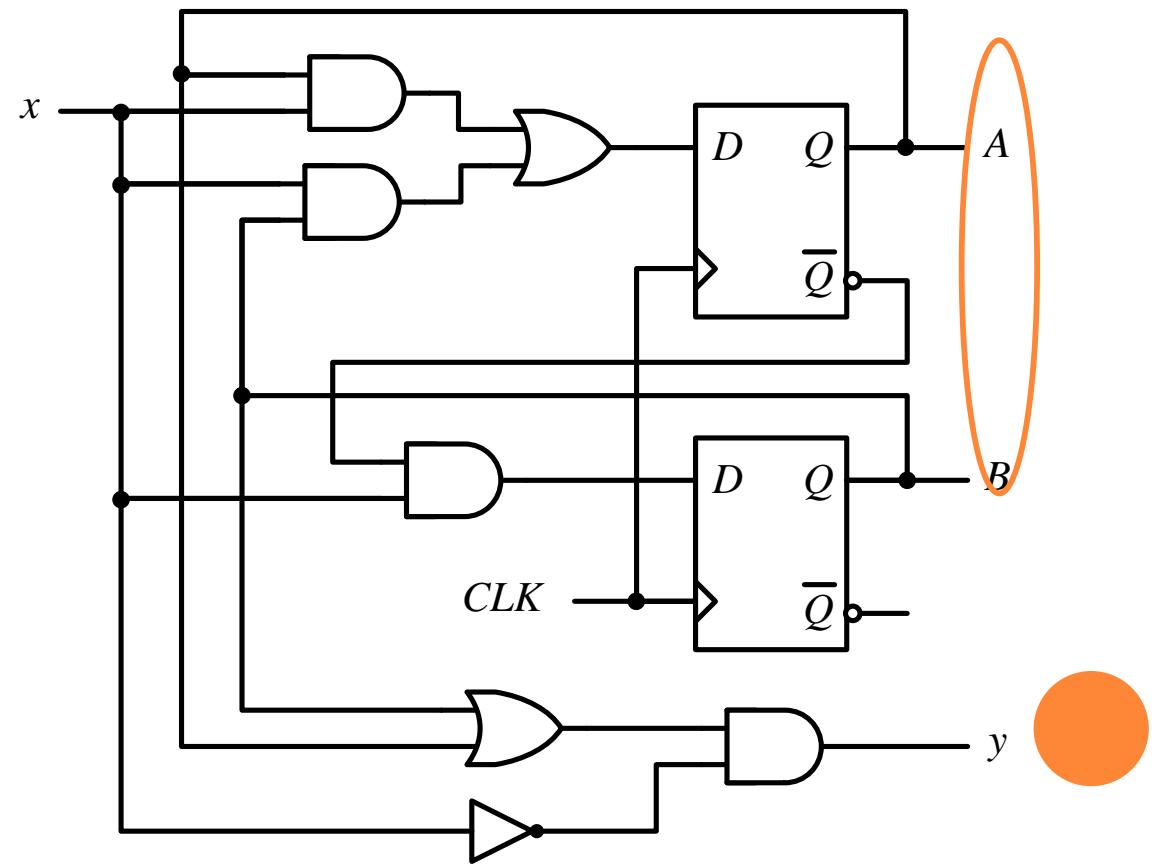


ANALYSIS OF CLOCKED SEQUENTIAL CIRCUITS: THE STATE

- State = Values of all Flip-Flops

Example

$$A \ B = 0 \ 0$$



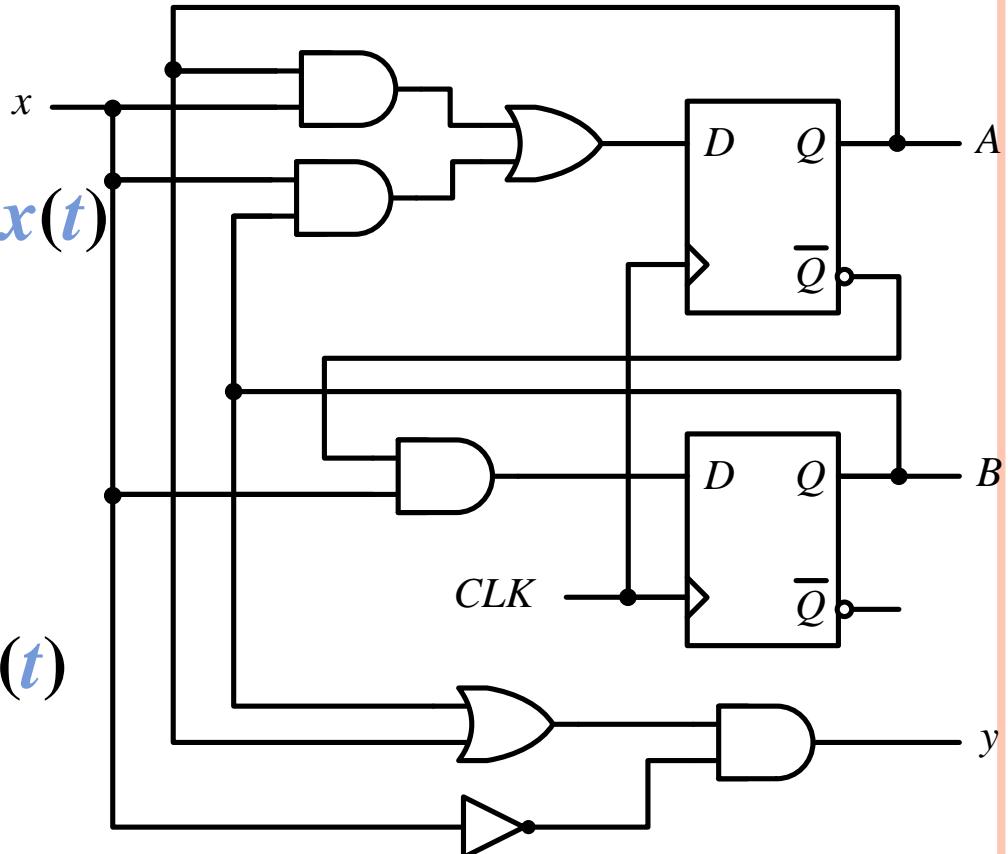
ANALYSIS OF CLOCKED SEQUENTIAL CIRCUITS: TERMINOLOGY

- *State Equation:* A state equation (transition equation) specifies the next state as a function of the present state and inputs.
- *State Table:* A state table (transition table) consists of: present state, input, next state and output.
- *State Diagram:* The information in a state table can be represented graphically in a state diagram. The state is represented by a circle and the transitions between states are indicated by directed lines connecting the circles.



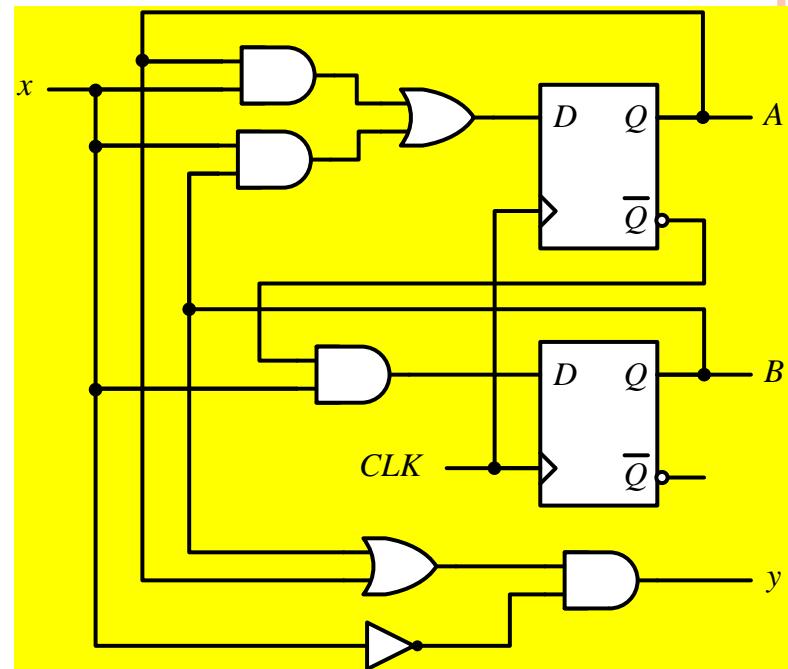
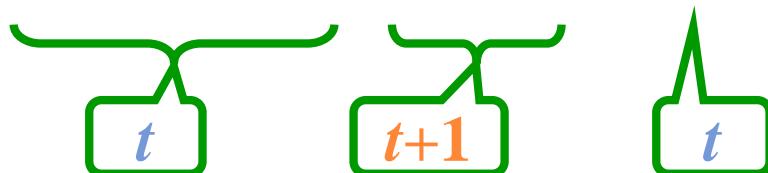
ANALYSIS OF CLOCKED SEQUENTIAL CIRCUITS: STATE/TRANSITION EQUATIONS

$$\begin{aligned}
 A(t+1) &= D_A \\
 &= A(t)x(t) + B(t)x(t) \\
 &= Ax + Bx \\
 B(t+1) &= D_B \\
 &= A'(t)x(t) \\
 &= A'x \\
 y(t) &= [A(t) + B(t)]x'(t) \\
 &= (A + B)x'
 \end{aligned}$$



ANALYSIS OF CLOCKED SEQUENTIAL CIRCUITS: STATE /TRANSITION TABLE

Present State	Input	Next State	Output		
A	B	x	A	B	y
0 0	0	0 0	0		
0 0	1	0 1	0		
0 1	0	0 0	1		
0 1	1	1 1	0		
1 0	0	0 0	1		
1 0	1	1 0	0		
1 1	0	0 0	1		
1 1	1	1 0	0		



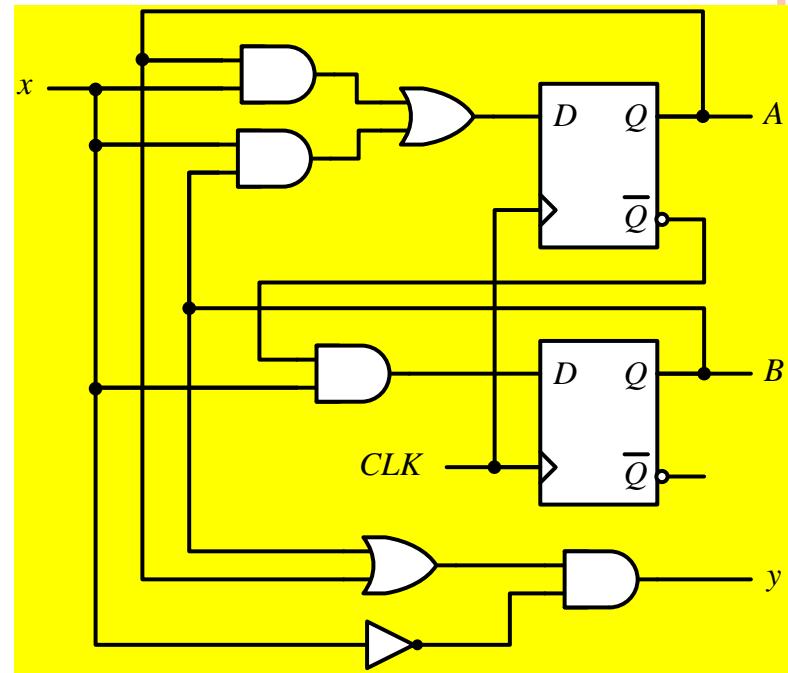
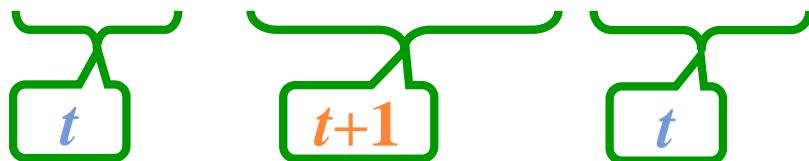
$$A(t+1) = A' x + B x$$

$$B(t+1) = A' x$$

$$y(t) = (A + B) x'$$

ANALYSIS OF CLOCKED SEQUENTIAL CIRCUITS: STATE/TRANSITION TABLE

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
$A \ B$	$A \ B$	$A \ B$	y	y
0 0	0 0	0 1	0	0
0 1	0 0	1 1	1	0
1 0	0 0	1 0	1	0
1 1	0 0	1 0	1	0

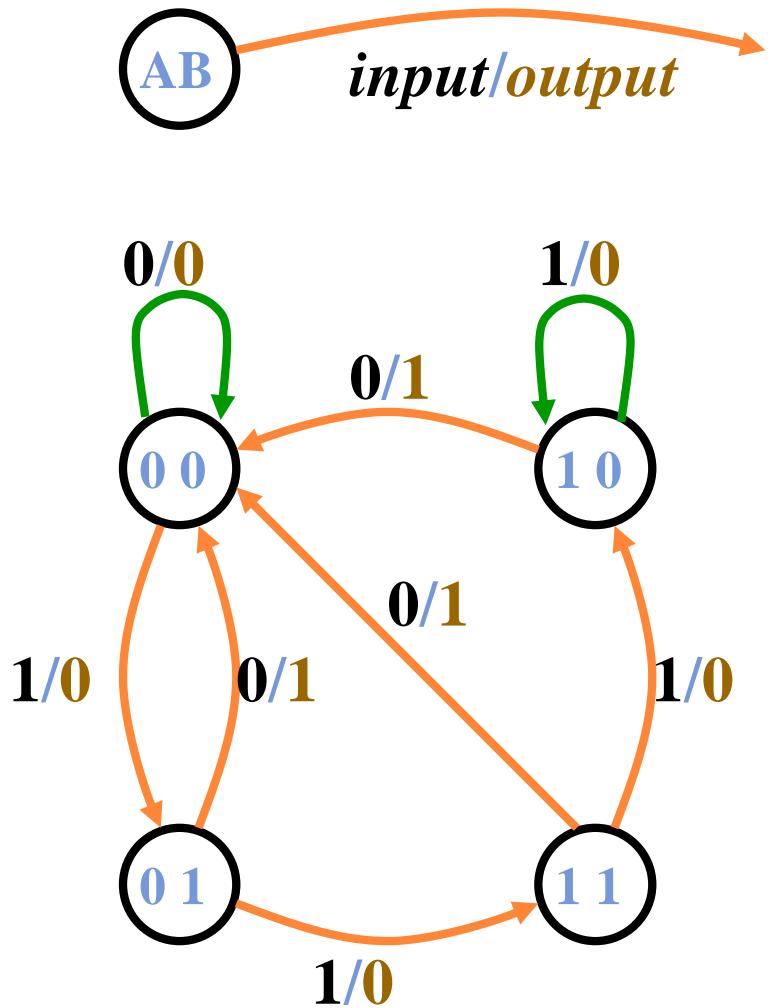


$$A(t+1) = A' x + B x$$

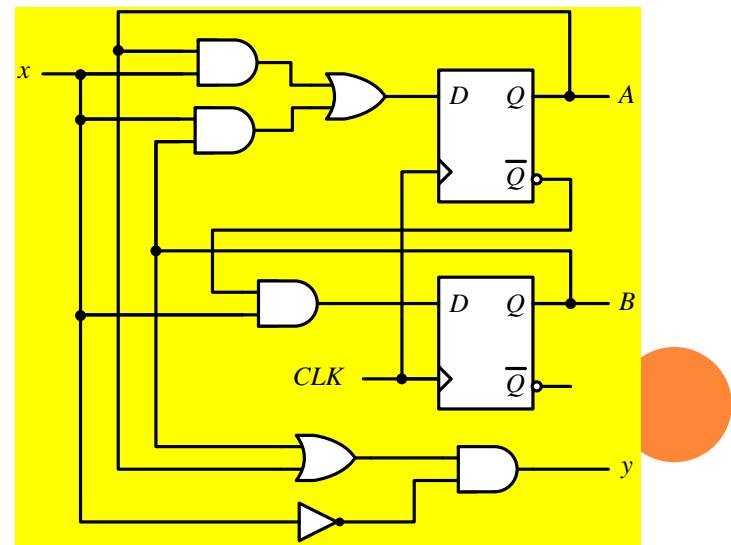
$$B(t+1) = A' x$$

$$y(t) = (A + B) x'$$

ANALYSIS OF CLOCKED SEQUENTIAL CIRCUITS: STATE DIAGRAM



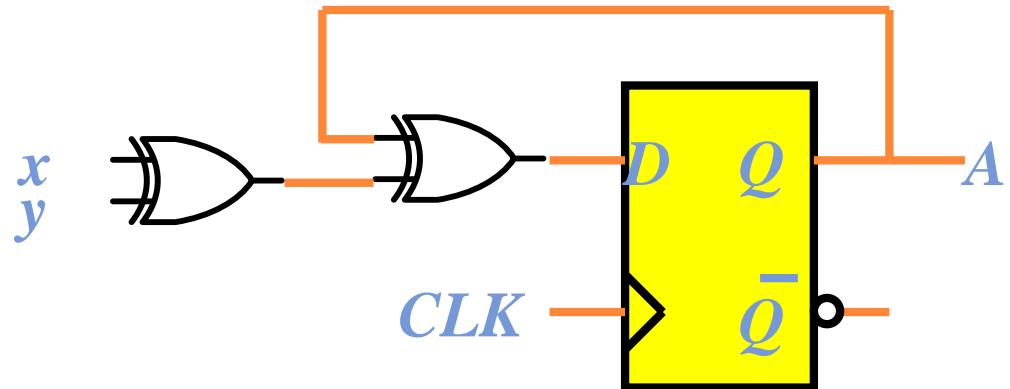
Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
A B	A B	A B	y	y
0 0	0 0	0 1	0	0
0 1	0 0	1 1	1	0
1 0	0 0	1 0	1	0
1 1	0 0	1 0	1	0



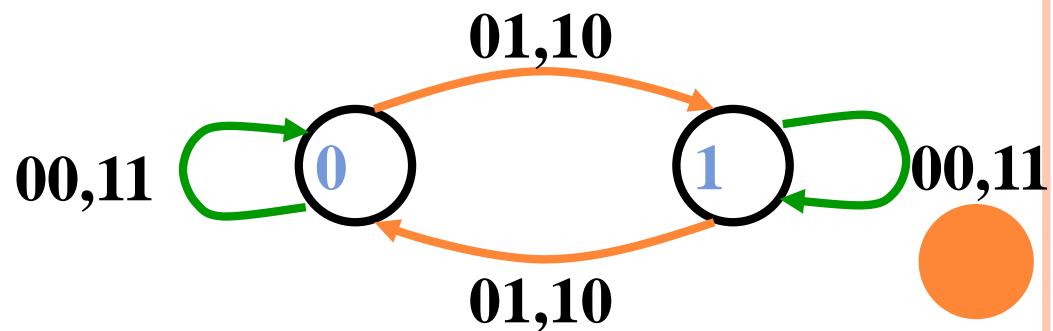
ANALYSIS OF CLOCKED SEQUENTIAL CIRCUITS: D FLIP-FLOPS

Example:

Present State	Input	Next State
A	$x \quad y$	A
0	0 0	0
0	0 1	1
0	1 0	1
0	1 1	0
1	0 0	1
1	0 1	0
1	1 0	0
1	1 1	1



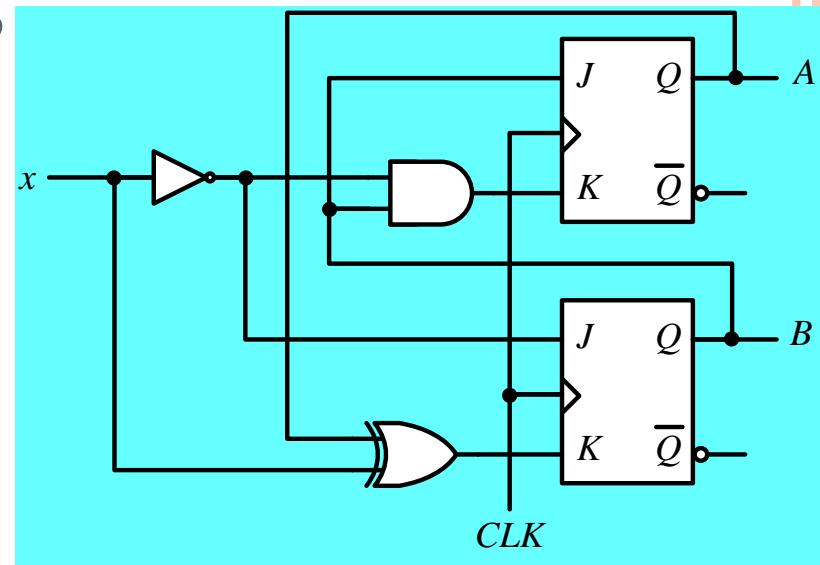
$$A(t+1) = D_A = A \oplus x \oplus y$$



ANALYSIS OF CLOCKED SEQUENTIAL CIRCUITS: *JK* FLIP-FLOPS

Example:

Present State		I/P	Next State		Flip-Flop Inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0



$$J_A = B$$

$$J_B = x'$$

$$K_A = Bx'$$

$$K_B = A \oplus x$$

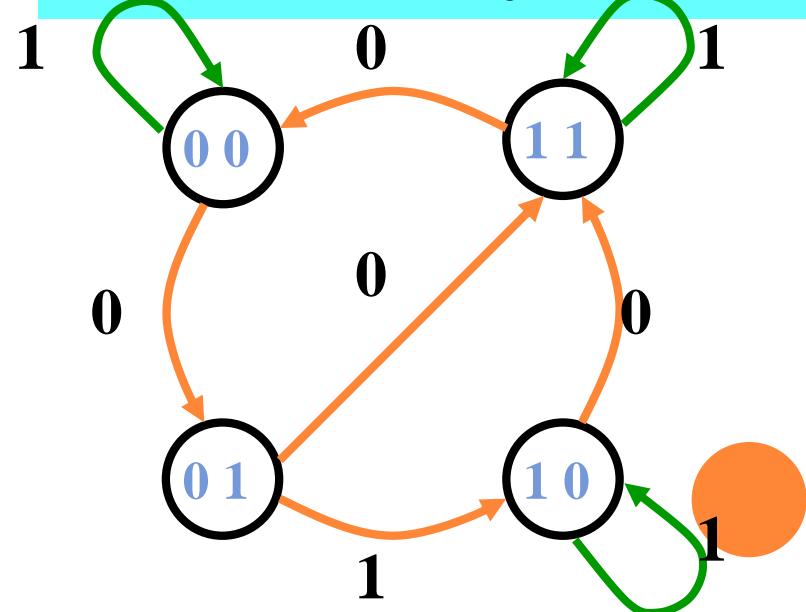
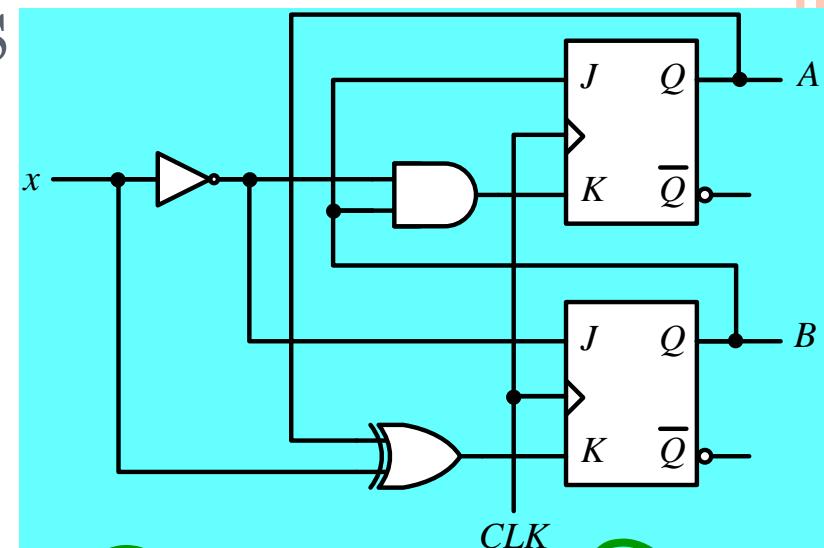
$$\begin{aligned} A(t+1) &= J_A Q'_A + K'_A Q_A \\ &= A'B + AB' + Ax \end{aligned}$$

$$\begin{aligned} B(t+1) &= J_B Q'_B + K'_B Q_B \\ &= B'x' + ABx + A'Bx' \end{aligned}$$

ANALYSIS OF CLOCKED SEQUENTIAL CIRCUITS: JK FLIP-FLOPS

Example:

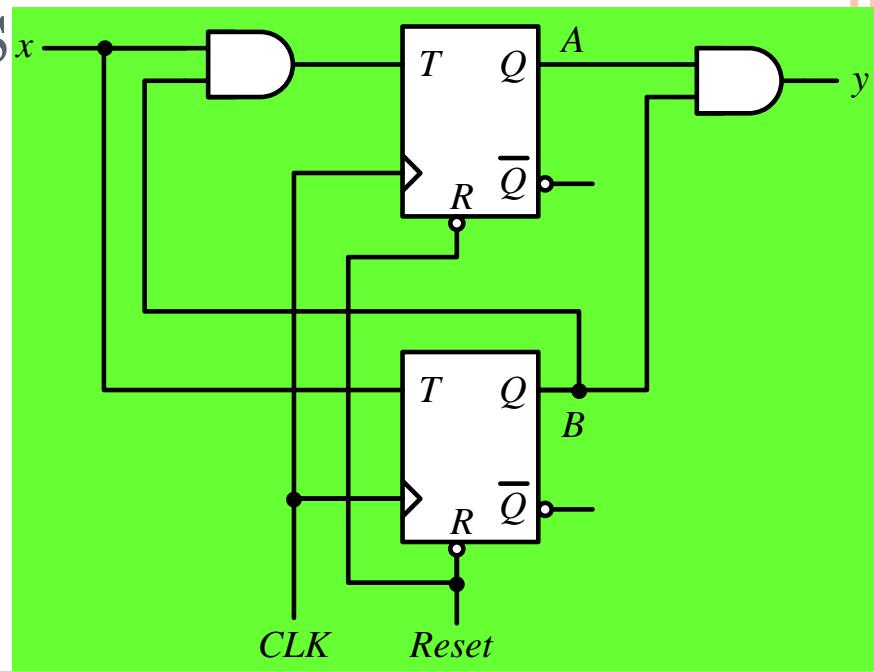
Present State		I/P	Next State		Flip-Flop Inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0



ANALYSIS OF CLOCKED SEQUENTIAL CIRCUITS: T FLIP-FLOPS

Example:

Present State		Next State		F.F Inputs	
A B	x	A B	T_A	T_B	y
0 0	0	0 0	0	0	0
0 0	1	0 1	0	1	0
0 1	0	0 1	0	0	0
0 1	1	1 0	1	1	0
1 0	0	1 0	0	0	0
1 0	1	1 1	0	1	0
1 1	0	1 1	0	0	1
1 1	1	0 0	1	1	1



$$\begin{aligned} T_A &= Bx \\ y &= AB \end{aligned}$$

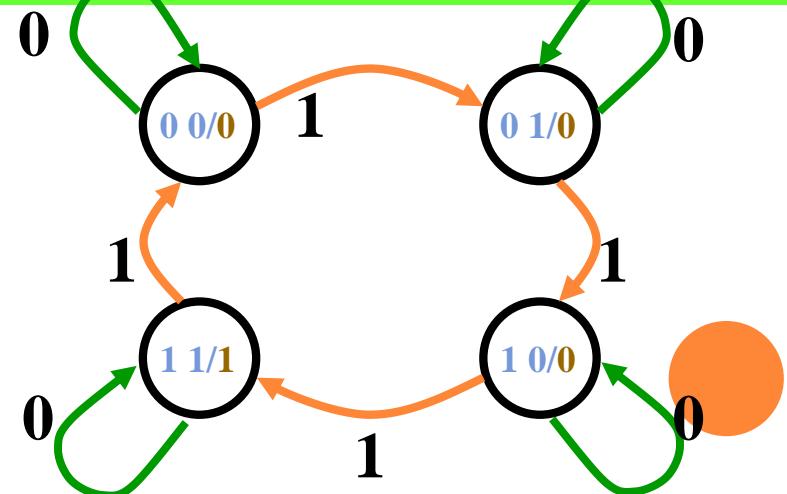
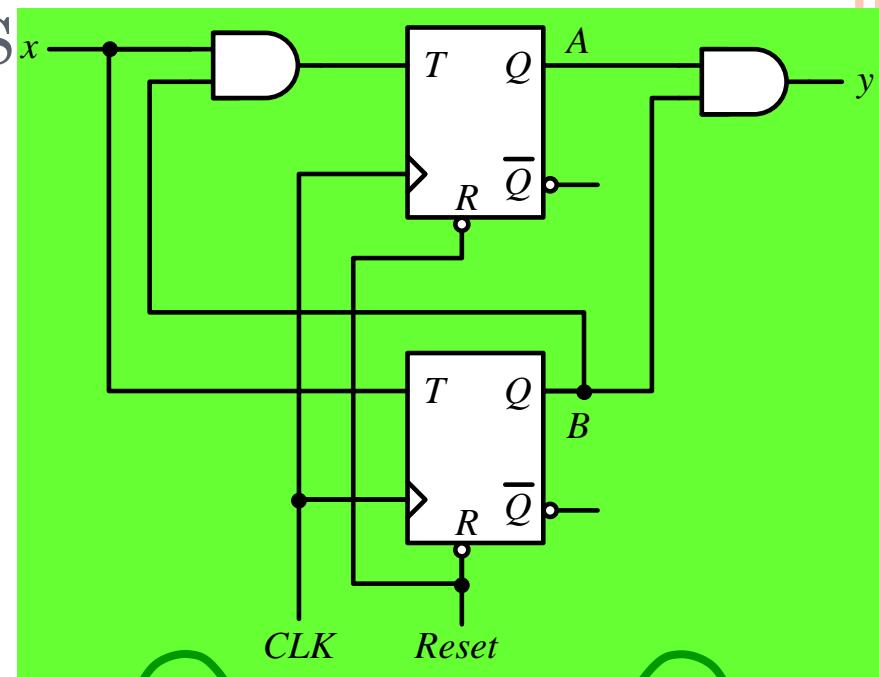
$$\begin{aligned} A(t+1) &= T_A Q'_A + T'_A Q_A \\ &= AB' + Ax' + A'Bx \end{aligned}$$

$$\begin{aligned} B(t+1) &= T_B Q'_B + T'_B Q_B \\ &= x \oplus B \end{aligned}$$

ANALYSIS OF CLOCKED SEQUENTIAL CIRCUITS: T FLIP-FLOPS

Example:

Present State		Next State		F.F Inputs	
A B	x	A B	T_A	T_B	y
0 0	0	0 0	0	0	0
0 0	1	0 1	0	1	0
0 1	0	0 1	0	0	0
0 1	1	1 0	1	1	0
1 0	0	1 0	0	0	0
1 0	1	1 1	0	1	0
1 1	0	1 1	0	0	1
1 1	1	0 0	1	1	1

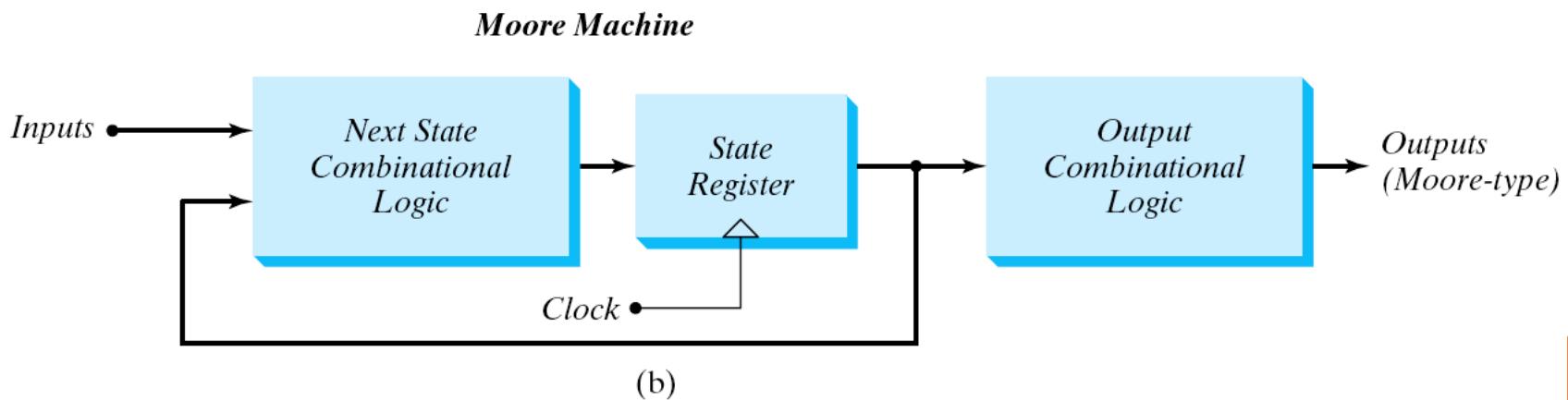
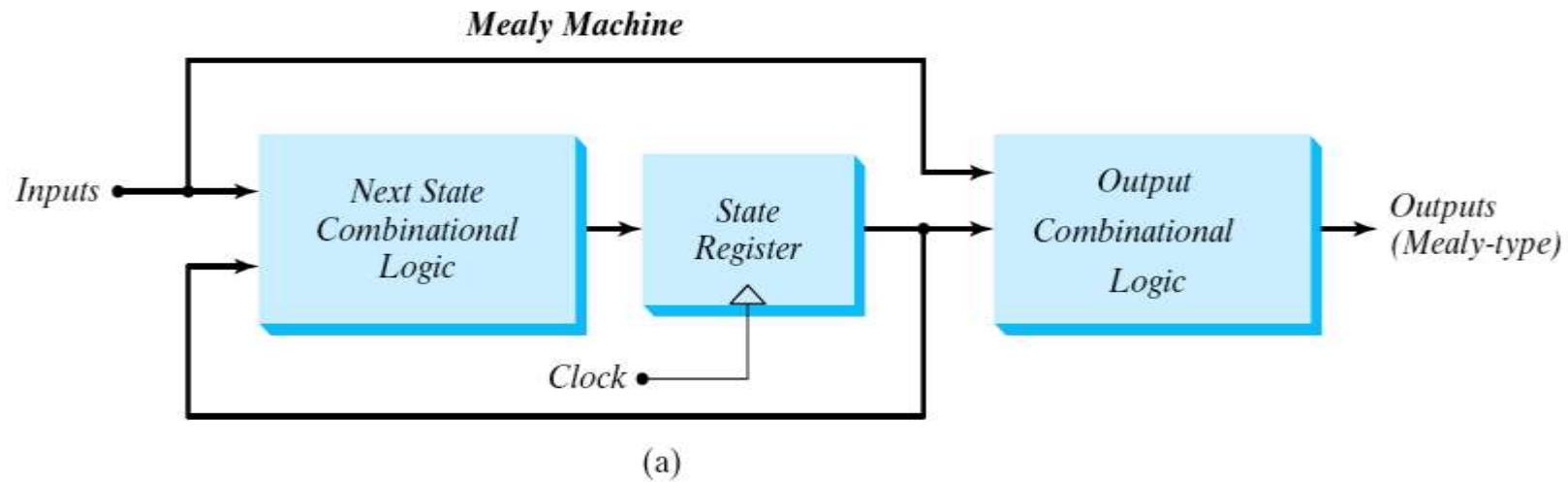


MEALY AND MOORE MODELS

- **The Mealy model:** the outputs are functions of both the present state and inputs
 - The outputs may change if the inputs change during the clock pulse period.
- **The Moore model:** the outputs are functions of the present state only
 - The outputs are synchronous with the clocks.



MEALY AND MOORE MODELS



Block diagram of Mealy and Moore state machine

MEALY AND MOORE MODELS

Mealy

Present State	I/P	Next State	O/P
A B	x	A B	y
0 0	0	0 0	0
0 0	1	0 1	0
0 1	0	0 0	1
0 1	1	1 1	0
1 0	0	0 0	1
1 0	1	1 0	0
1 1	0	0 0	1
1 1	1	1 0	0

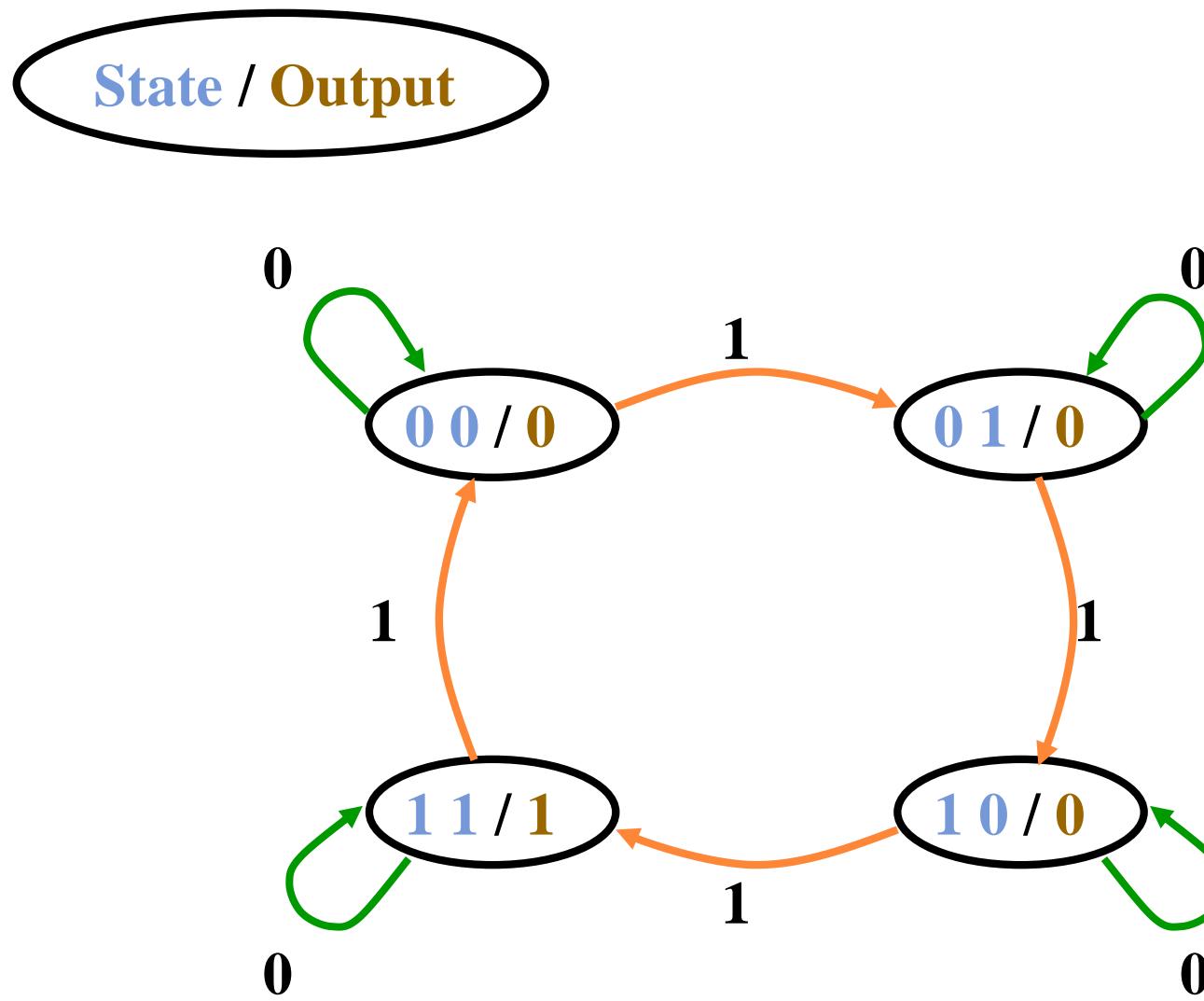
Moore

Present State	I/P	Next State	O/P
A B	x	A B	y
0 0	0	0 0	0
0 0	1	0 1	0
0 1	0	0 1	0
0 1	1	1 0	0
1 0	0	1 0	0
1 0	1	1 1	0
1 1	0	1 1	1
1 1	1	0 0	1

For the same state,
the output changes with the input

For the same state,
the output does not change with the input

MOORE STATE DIAGRAM



STATE REDUCTION

- Sequential circuit analysis

Circuit diagram \longrightarrow state table (or state diagram)

- Sequential circuit design

State diagram (state table) \longrightarrow circuit diagram

- Redundant state may exist in a state diagram (or table)

- By eliminating them \longrightarrow may reduce the # of flip-flops



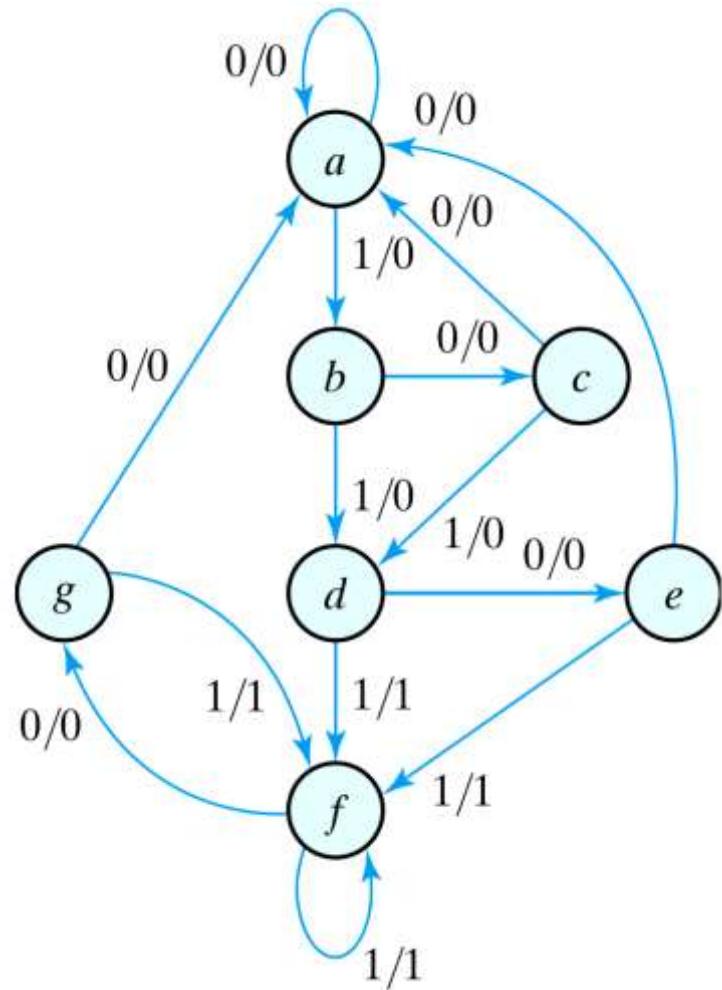
STATE REDUCTION

State: a a b c d e f f g f g a

Input: 0 1 0 1 0 1 1 0 1 0 0

Output: 0 0 0 0 0 1 1 0 1 0 0

- Only the input-output sequences are important.
- Two circuits are **equivalent**
 - Have identical outputs for all input sequences;
 - The number of states is not important.



State diagram

STATE REDUCTION

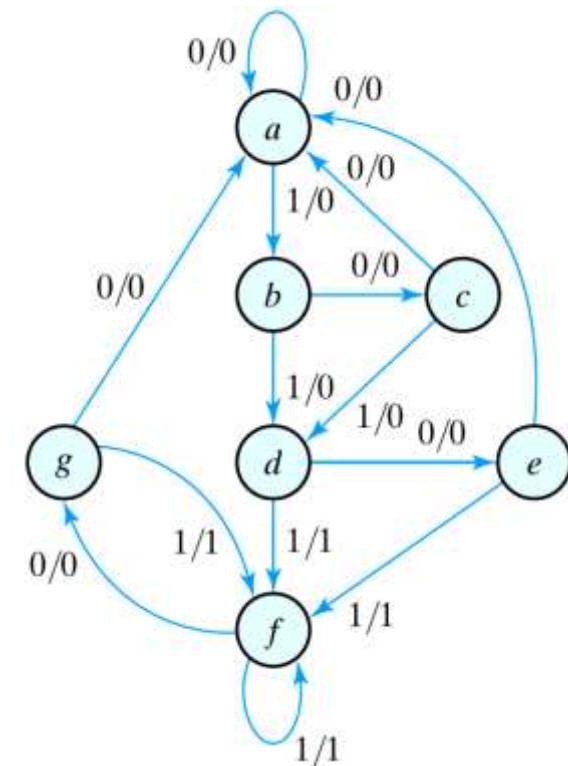
- Equivalent states
 - Two states are said to be equivalent
 - For each member of the set of inputs, they give exactly the same output and send the circuit to the same state or to an equivalent state.
 - One of them can be removed.



STATE REDUCTION

Table 5.6
State Table

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1



STATE REDUCTION

- Reducing the state table
 - $e = g$ (remove g);
 - $d = f$ (remove f);

Table 5.7
Reducing the State Table

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	e	f	0	1



STATE REDUCTION

- The reduced finite state machine

Table 5.8

Reduced State Table

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
<i>a</i>	<i>a</i>	<i>b</i>	0	0
<i>b</i>	<i>c</i>	<i>d</i>	0	0
<i>c</i>	<i>a</i>	<i>d</i>	0	0
<i>d</i>	<i>e</i>	<i>d</i>	0	1
<i>e</i>	<i>a</i>	<i>d</i>	0	1

State: a a b c d e d d e d e a

Input: 0 1 0 1 0 1 1 0 1 0 0

Output: 0 0 0 0 0 1 1 0 1 0 0



STATE REDUCTION: IMPLICATION TABLE

- The state-reduction procedure for completely specified state tables is based on the algorithm that two states in a state table can be combined into one if they can be shown to be equivalent.
- There are occasions when a pair of states do not have the same next states, but, nonetheless, go to equivalent next states
- The checking of each pair of states for possible equivalence in a table with a large number of states can be done systematically by means of an *implication table*.



STATE REDUCTION: IMPLICATION TABLE

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	c	b	0	1
b	d	a	0	1
c	a	d	1	0
d	b	d	1	0

- (a, b) imply (c, d) and (c, d) imply (a, b) . Both pairs of states are equivalent; i.e., a and b are equivalent as well as c and d .

STATE REDUCTION:IMPLICATION TABLE

<i>b</i>	<i>d , e ✓</i>		
<i>c</i>	✗		
<i>d</i>	✗		
<i>e</i>	✗	✗	✗
<i>f</i>	<i>c , d</i> ✗ <i>a , b</i>	✗	✗
<i>g</i>	✗	✗	✗
<i>a</i>			
<i>b</i>			
<i>c</i>			
<i>d</i>			
<i>e</i>			
<i>f</i>			

Present State	Next State		Output	
	x = 0	x = 1	x = 0	x = 1
<i>a</i>	<i>d</i>	6	0	0
<i>b</i>	<i>e</i>	<i>a</i>	0	0
<i>c</i>	<i>g</i>	<i>f</i>	0	1
<i>d</i>	<i>a</i>	<i>d</i>	1	0
<i>e</i>	<i>a</i>	<i>d</i>	1	0
<i>f</i>	<i>c</i>	<i>b</i>	0	0
<i>g</i>	<i>a</i>	<i>e</i>	1	0

STATE REDUCTION: IMPLICATION TABLE

- Finally, all the squares that have no crosses are recorded with check marks. The equivalent states are: (a, b) , (d, e) , (d, g) , (e, g) .
- We now combine pairs of states into larger groups of equivalent states. The last three pairs can be combined into a set of three equivalent states (d, e, g) because each one of the states in the group is equivalent to the other two.



STATE REDUCTION: IMPLICATION TABLE

- The final partition of these states consists of the equivalent states found from the implication table, together with all the remaining states in the state table that are not equivalent to any other state: (a, b) (c) (d, e, g) (f)

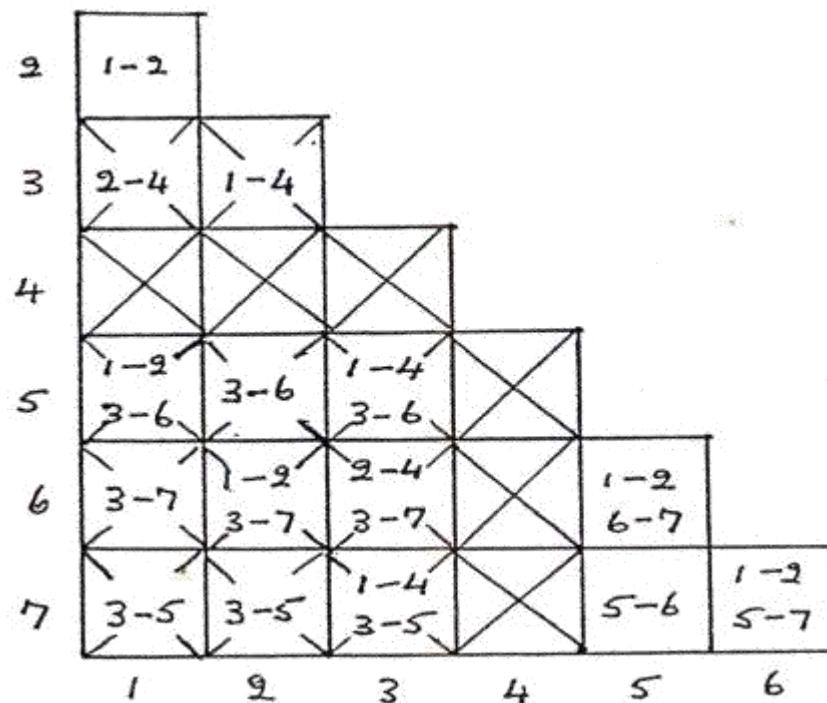
Table 9.5
Reduced State Table

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	d	a	0	0
c	d	f	0	1
d	a	d	1	0
f	c	a	0	0



IMPLIED EQUIVALENCES EXTENDING OVER A NUMBER OF STATES

PS	NS		Z
	x = 0	x = 1	
①	2	3	0
②	1	3	0
③	4	3	0
④	4	5	1
⑤	1	6	0
⑥	2	7	0
⑦	1	5	0



- **5 = 6** if $6 = 7$, **5 = 7** if $5 = 6$, **6 = 7** if $5 = 7$
- **1 = 2** and **5 = 6**, **5 = 7**, **6 = 7** i.e. **5 = 6 = 7**

IMPLIED EQUIVALENCES EXTENDING OVER A NUMBER OF STATES

PS	NS		Z
	x = 0	x = 1	
①	2	3	0
②	1	3	0
③	4	3	0
④	4	5	1
⑤	1	6	0
⑥	2	7	0
⑦	1	5	0

PS	NS		Z
	x = 0	x = 1	
①	1	3	0
③	4	3	0
④	4	5	1
⑤	1	5	0

- **5 = 6** if **6 = 7**, **5 = 7** if **5 = 6**, **6 = 7** if **5 = 7**
- **1 = 2** and **5 = 6**, **5 = 7**, **6 = 7** i.e. **5 = 6 = 7**



IMPLIED EQUIVALENCES EXTENDING OVER A NUMBER OF STATES

Alternative definition of equivalence:

- Two circuit states with the same output conditions can be made equivalent, unless the equivalence depends upon a known non-equivalence.



STATE ASSIGNMENT

- Assign coded binary values to the states for physical implementation
- For a circuit with m states, the codes must contain n bits where $2^n \geq m$
- Unused states are treated as don't care conditions during the design
 - Don't cares can help to obtain a simpler circuit
- There are many possible state assignments
 - Have large impacts on the final circuit size



POPULAR STATE ASSIGNMENT

Table 5.9
Three Possible Binary State Assignments

State	Assignment 1, Binary	Assignment 2, Gray Code	Assignment 3, One-Hot
<i>a</i>	000	000	00001
<i>b</i>	001	001	00010
<i>c</i>	010	011	00100
<i>d</i>	011	010	01000
<i>e</i>	100	110	10000



STATE ASSIGNMENT

- Any binary number assignment is satisfactory as long as each state is assigned a unique number
- Use binary assignment 1

Table 5.10

Reduced State Table with Binary Assignment 1

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
000	000	001	0	0
001	010	011	0	0
010	000	011	0	0
011	100	011	0	1
100	000	011	0	1



DESIGN PROCEDURE

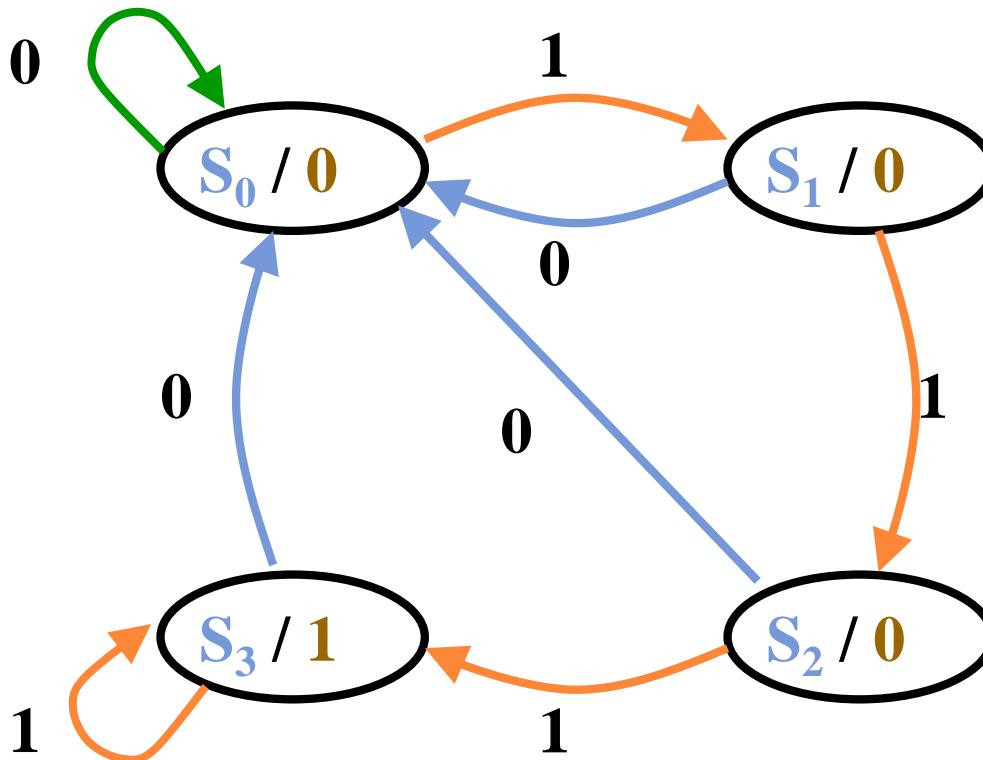
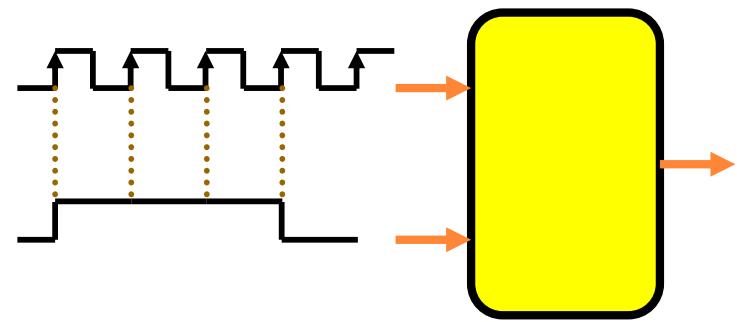
- Derive a state diagram for the circuit from specifications
- Reduce the number of states if necessary
- Assign binary values to the states
- Obtain the binary-coded state table
- Choose the type of flip-flop to be used
- Derive the simplified flip-flop input equations and output equations
- Draw the logic diagram



DESIGN OF CLOCKED SEQUENTIAL CIRCUITS

- Example:

Detect 3 or more consecutive 1's



State	A	B
S_0	0	0
S_1	0	1
S_2	1	0
S_3	1	1

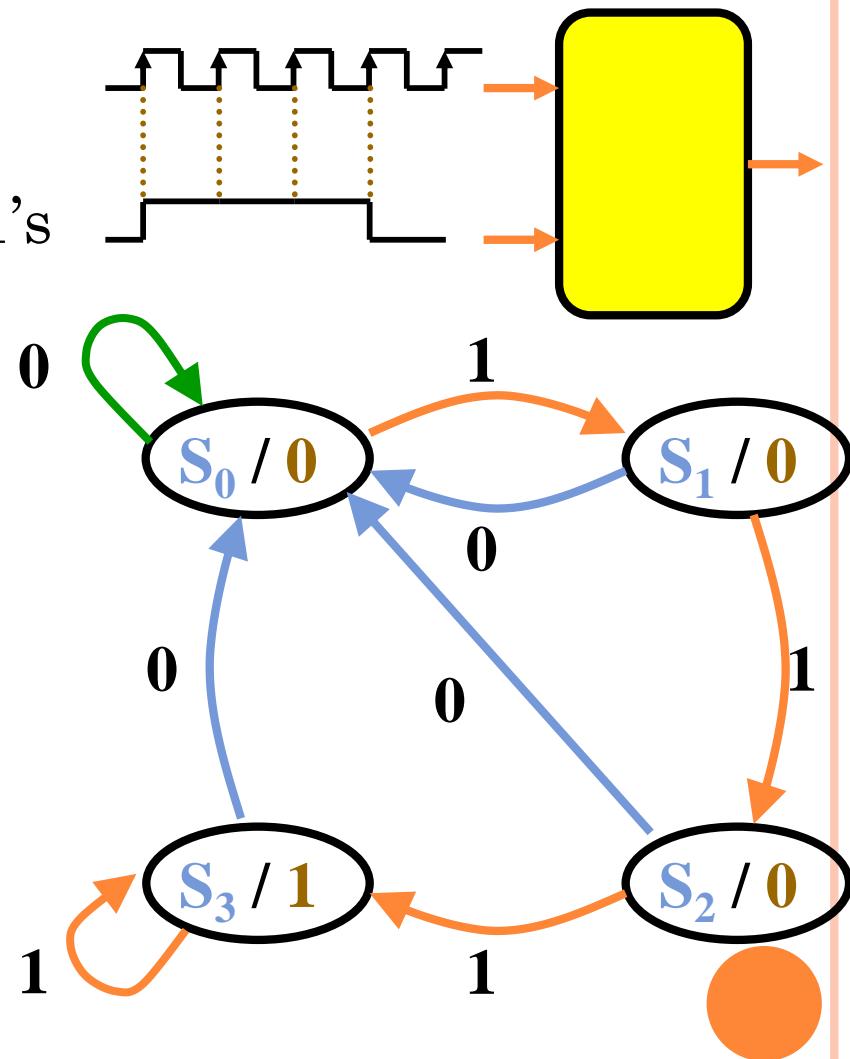


DESIGN OF CLOCKED SEQUENTIAL CIRCUITS

- Example:

Detect 3 or more consecutive 1's

Present State	Input	Next State	Output
A B	x	A B	y
0 0	0	0 0	0
0 0	1	0 1	0
0 1	0	0 0	0
0 1	1	1 0	0
1 0	0	0 0	0
1 0	1	1 1	0
1 1	0	0 0	1
1 1	1	1 1	1

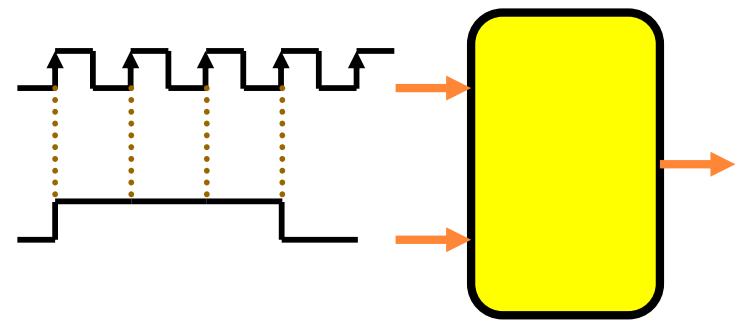


DESIGN OF CLOCKED SEQUENTIAL CIRCUITS

- Example:

Detect 3 or more consecutive 1's

Present State		Input	Next State		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	1



Synthesis using D Flip-Flops

$$\begin{aligned} A(t+1) &= D_A(A, B, x) \\ &= \sum (3, 5, 7) \end{aligned}$$

$$\begin{aligned} B(t+1) &= D_B(A, B, x) \\ &= \sum (1, 5, 7) \end{aligned}$$

$$y(A, B, x) = \sum (6, 7)$$



DESIGN OF CLOCKED SEQUENTIAL CIRCUITS WITH D F.F.

- Example:

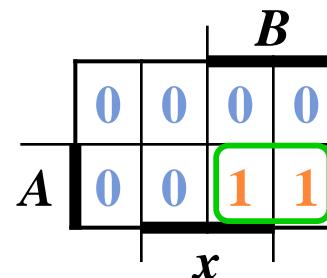
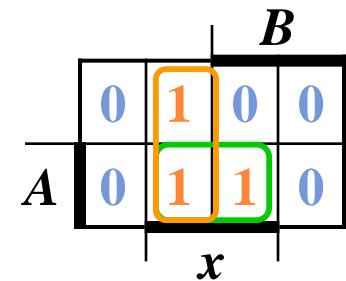
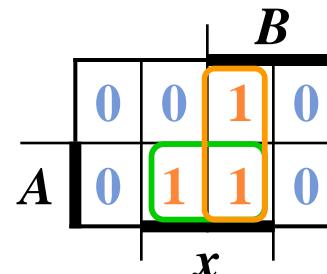
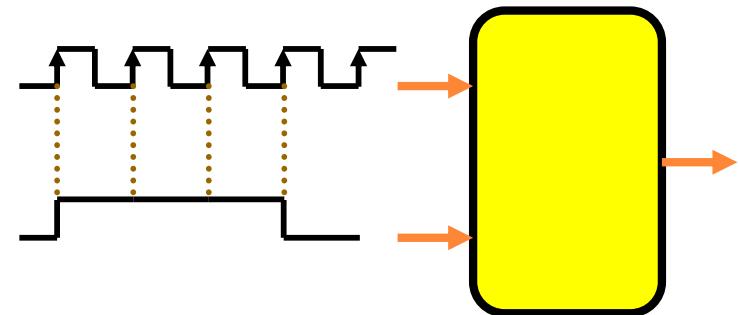
Detect 3 or more consecutive 1's

Synthesis using D Flip-Flops

$$D_A(A, B, x) = \sum (3, 5, 7) \\ = A'x + Bx$$

$$D_B(A, B, x) = \sum (1, 5, 7) \\ = Ax + B'x$$

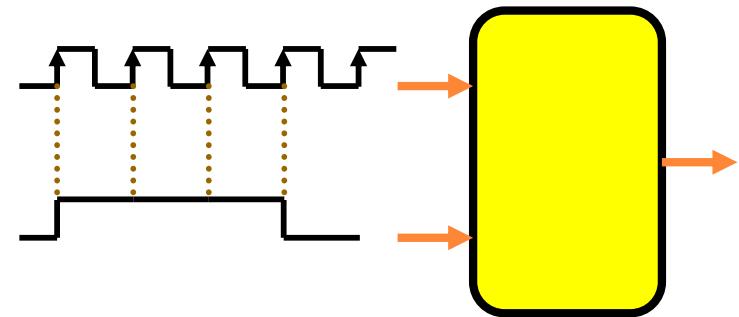
$$y(A, B, x) = \sum (6, 7) \\ = AB$$



DESIGN OF CLOCKED SEQUENTIAL CIRCUITS WITH D F.F.

- Example:

Detect 3 or more consecutive 1's

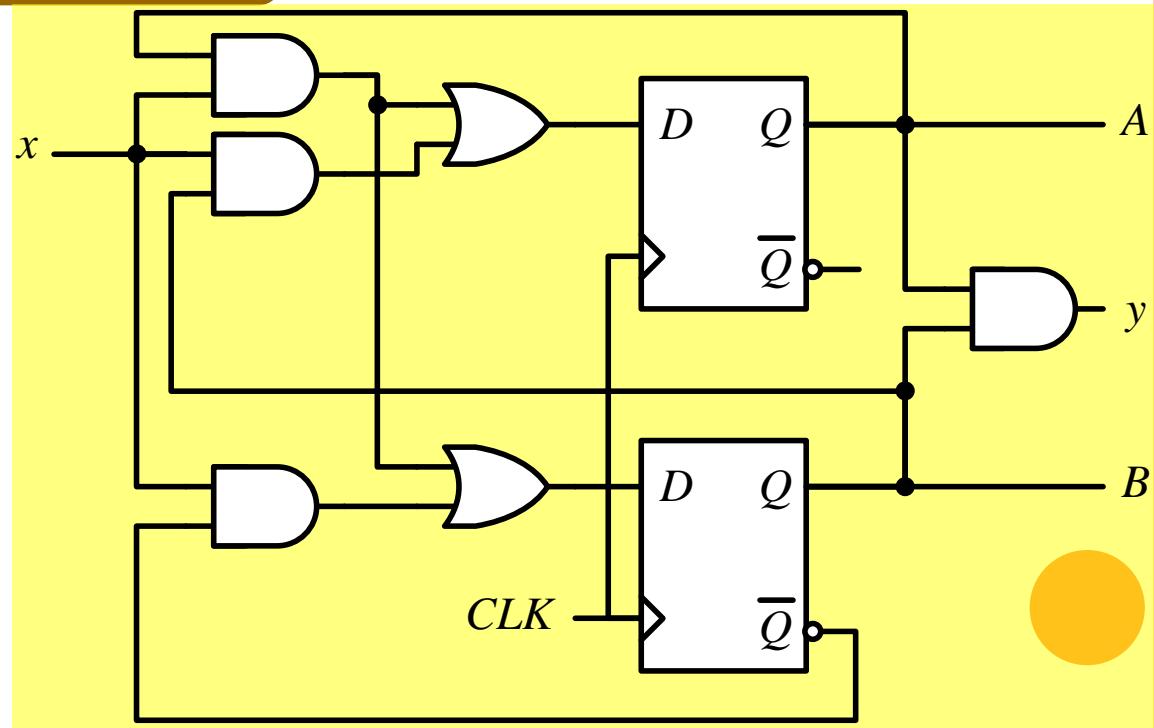


Synthesis using D Flip-Flops

$$D_A = A'x + Bx$$

$$D_B = A'x + B'x$$

$$y = AB$$



FLIP-FLOP EXCITATION TABLES

Present State	Next State	F.F. Input
$Q(t)$	$Q(t+1)$	D
0	0	0
0	1	1
1	0	0
1	1	1

Present State	Next State	F.F. Input
$Q(t)$	$Q(t+1)$	J K
0	0	0 x
0	1	1 x
1	0	x 1
1	1	x 0

- 0 0 (No change)
- 0 1 (Reset)
- 1 0 (Set)
- 1 1 (Toggle)
- 0 1 (Reset)
- 1 1 (Toggle)
- 0 0 (No change)
- 1 0 (Set)

$Q(t)$	$Q(t+1)$	T
0	0	0
0	1	1
1	0	1
1	1	0

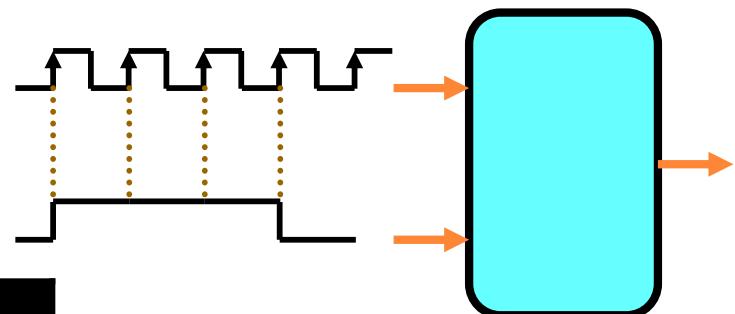


DESIGN OF CLOCKED SEQUENTIAL CIRCUITS WITH *JK* F.F.

- Example:

Detect 3 or more consecutive 1's

Present State	Input	Next State		Flip-Flop Inputs			
A B	x	A	B	J_A	K_A	J_B	K_B
0 0	0	0	0	0	x	0	x
0 0	1	0	1	0	x	1	x
0 1	0	0	0	0	x	x	1
0 1	1	1	0	1	x	x	1
1 0	0	0	0	x	1	0	x
1 0	1	1	1	x	0	1	x
1 1	0	0	0	x	1	x	1
1 1	1	1	1	x	0	x	0



Synthesis using *JK* F.F.

$$\begin{aligned}
 J_A(A, B, x) &= \sum(3) \\
 d_{JA}(A, B, x) &= \sum(4, 5, 6, 7) \\
 K_A(A, B, x) &= \sum(4, 6) \\
 d_{KA}(A, B, x) &= \sum(0, 1, 2, 3) \\
 J_B(A, B, x) &= \sum(1, 5) \\
 d_{JB}(A, B, x) &= \sum(2, 3, 6, 7) \\
 K_B(A, B, x) &= \sum(2, 3, 6) \\
 d_{KB}(A, B, x) &= \sum(0, 1, 4, 5)
 \end{aligned}$$

DESIGN OF CLOCKED SEQUENTIAL CIRCUITS WITH *JK* F.F.

- Example:

Detect 3 or more consecutive 1's

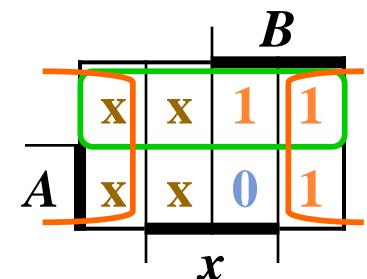
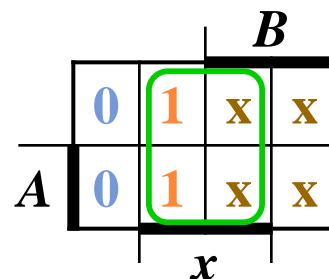
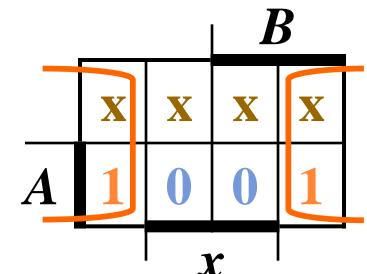
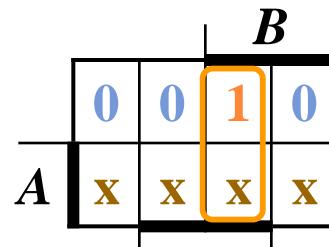
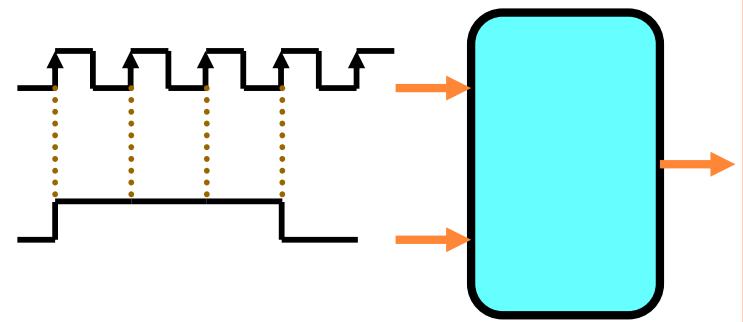
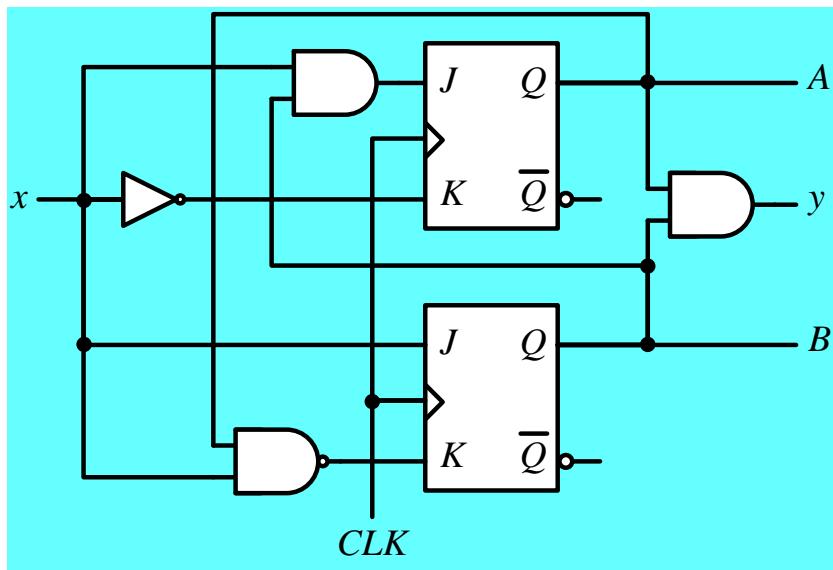
Synthesis using *JK* Flip-Flops

$$J_A = B \cdot x$$

$$K_A = x'$$

$$J_B = x$$

$$K_B = A' + x'$$

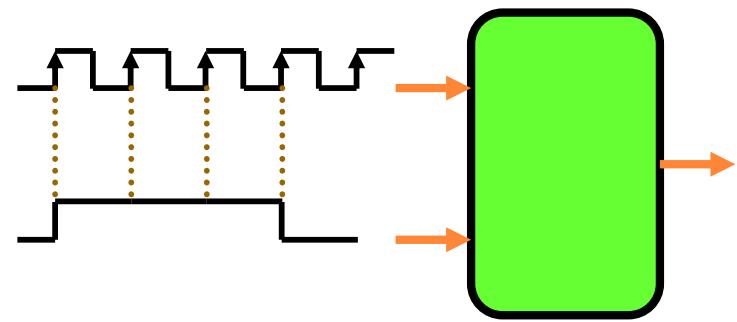


DESIGN OF CLOCKED SEQUENTIAL CIRCUITS WITH T F.F.

- Example:

Detect 3 or more consecutive 1's

Present State		Input	Next State		F.F. Input	
A	B	x	A	B	T_A	T_B
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	0	0	0	0	1
0	1	1	1	0	1	1
1	0	0	0	0	1	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	1	1	1	0	0



Synthesis using T Flip-Flops

$$T_A(A, B, x) = \sum (3, 4, 6)$$

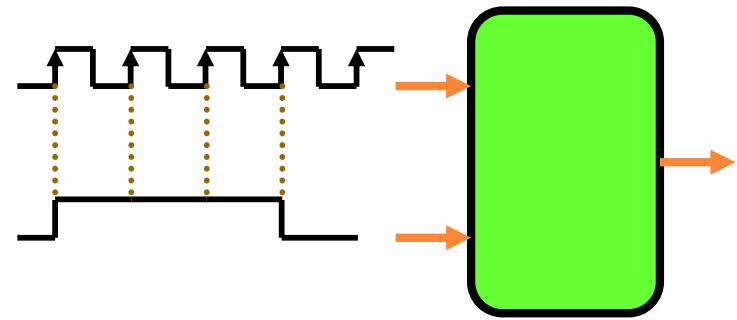
$$T_B(A, B, x) = \sum (1, 2, 3, 5, 6)$$



DESIGN OF CLOCKED SEQUENTIAL CIRCUITS WITH T F.F.

- Example:

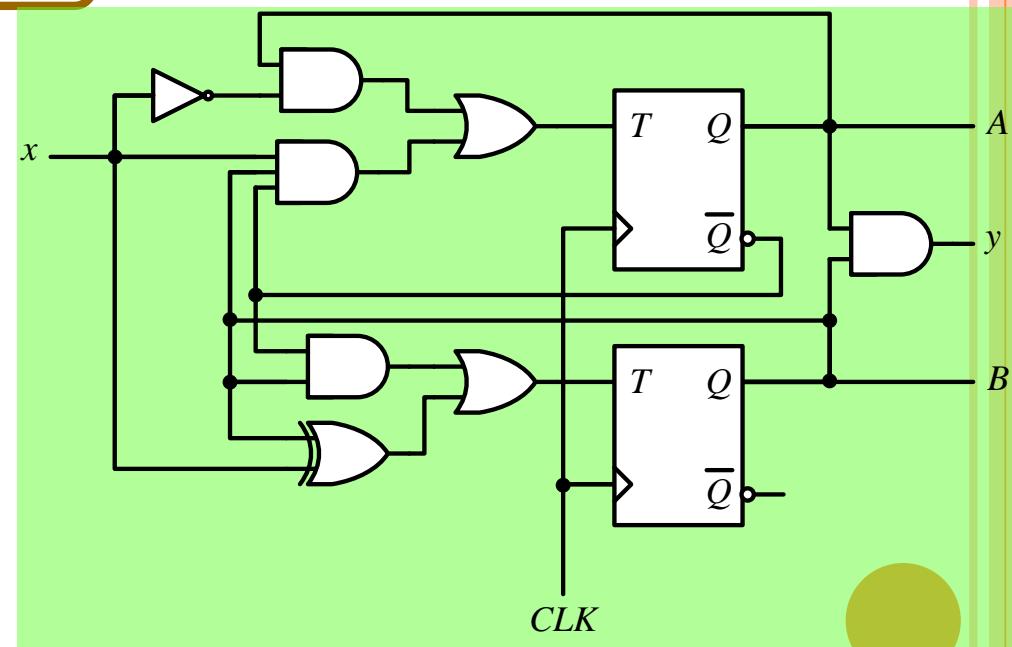
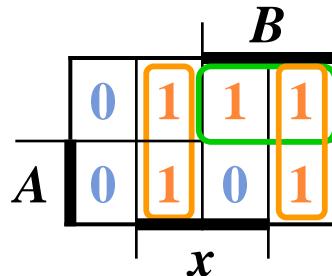
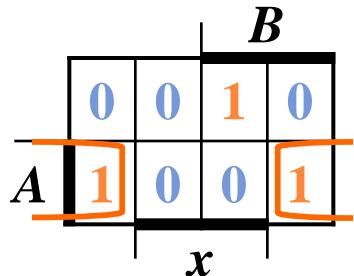
Detect 3 or more consecutive 1's



Synthesis using T Flip-Flops

$$T_A = A x' + A' B x$$

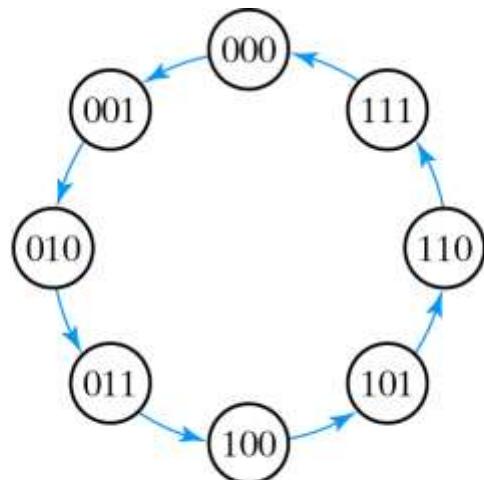
$$T_B = A' B + B \oplus x$$



DESIGN OF CLOCKED SEQUENTIAL CIRCUITS WITH T F.F.

- Example:

3-bit binary counter



Present State			Next State			Flip-Flop Inputs		
A2	A1	A0	A2	A1	A0	T_{A2}	T_{A1}	T_{A0}
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

Fig. 5-29 State Diagram of 3-Bit Binary Counter

DESIGN OF CLOCKED SEQUENTIAL CIRCUITS WITH T F.F.

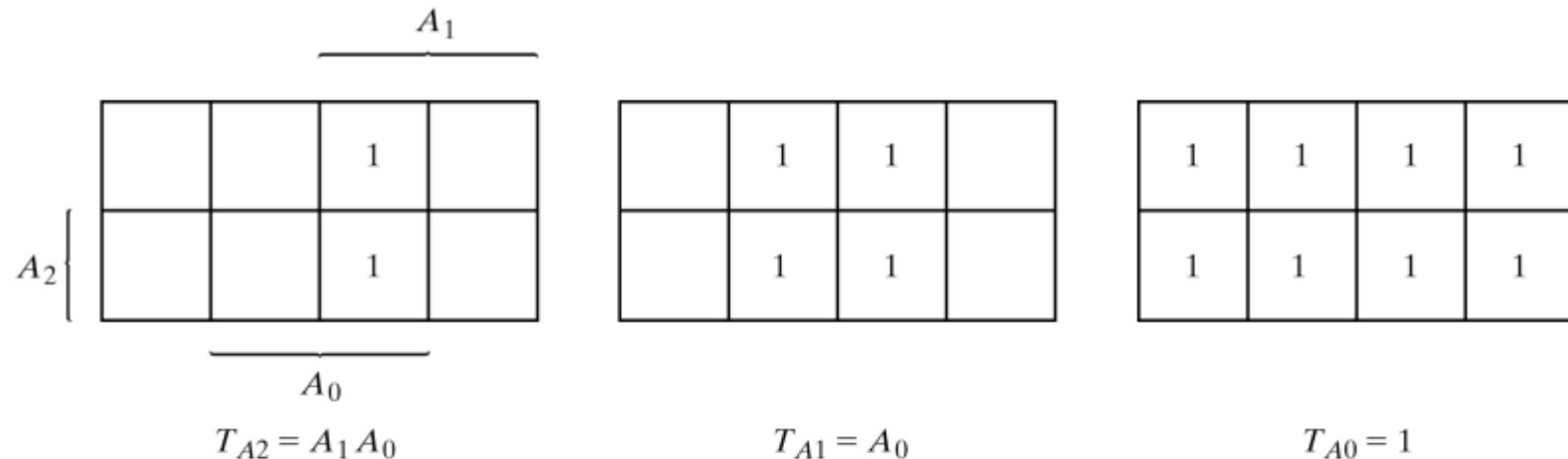


Fig. 5-30 Maps for 3-Bit Binary Counter

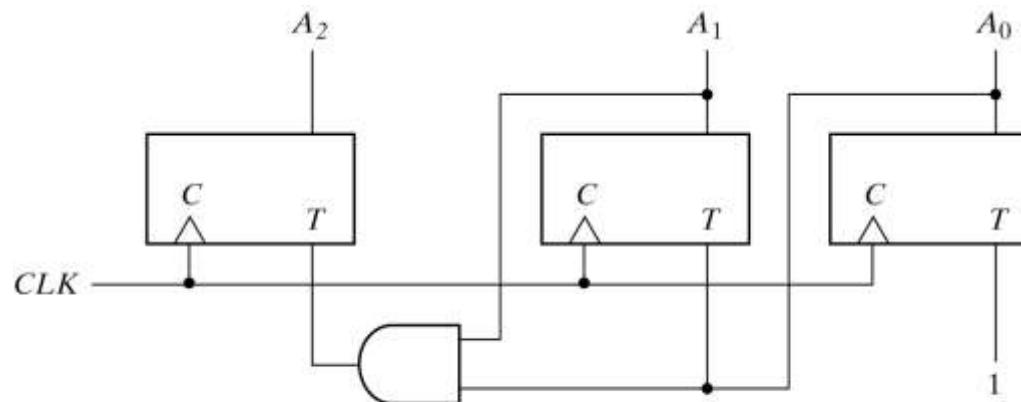


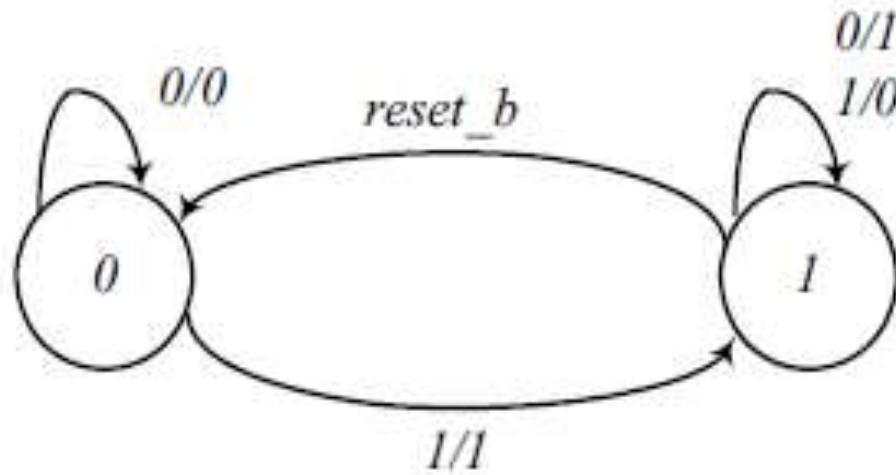
Fig. 5-31 Logic Diagram of 3-Bit Binary Counter

DESIGN OF CLOCKED SEQUENTIAL CIRCUITS WITH D F.F.

- Design a one-input, one-output serial 2's complementer. The circuit accepts a string of bits from the input and generates the 2's complement at the output. The circuit can be reset asynchronously to start and end the operation.



DESIGN OF CLOCKED SEQUENTIAL CIRCUITS WITH D F.F.

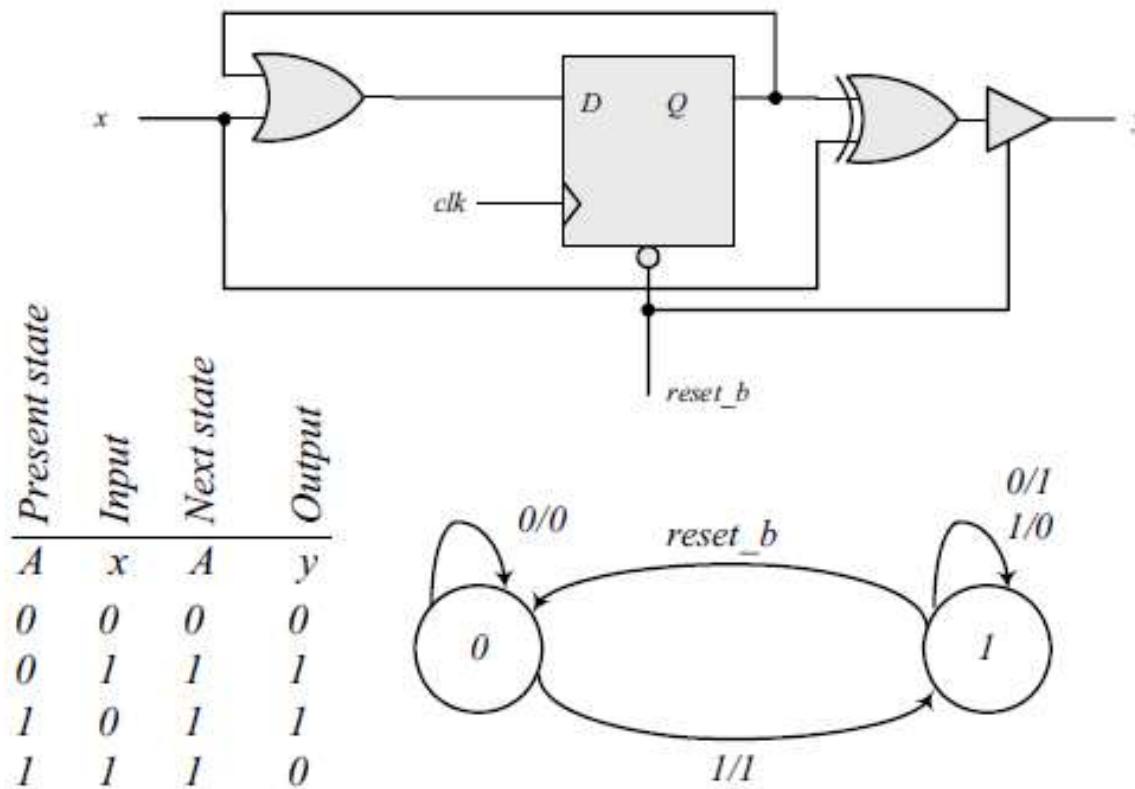


Present state	Input	Next state	Output
A	x	A	y
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	0

$$D_A = A + x$$
$$y = Ax' + A'x$$



DESIGN OF CLOCKED SEQUENTIAL CIRCUITS WITH D F.F.



$$D_A = A + x$$

$$y = Ax' + A'x$$

SYLLABUS

- Chapter 5 (Excluding Section 5.6)

