



## Description of Course CSE 205

### PART A: General Information

- |                                  |                        |
|----------------------------------|------------------------|
| <b>1 Course Title</b>            | : DIGITAL LOGIC DESIGN |
| <b>2 Type of Course</b>          | : THEORY               |
| <b>3 Offered to</b>              | : DEPARTMENT OF CSE    |
| <b>4 Pre-requisite Course(s)</b> | : NONE                 |

### PART B: Course Details

#### 1. Course Content (As approved by the Academic Council)

Digital logic: Boolean algebra, De Morgan's Theorems, logic gates and their truth tables, canonical forms, combinational logic circuits, minimization techniques; Arithmetic and data handling logic circuits, decoders and encoders, multiplexers and demultiplexers; Combinational circuit design; Flip-flops; race around problems; Counters: asynchronous and synchronous counters and their applications; Asynchronous and synchronous logic design: State diagram, Mealy and Moore machines; State minimizations and assignments; Pulse mode logic; Fundamental mode design; PLA design; Design using MSI and LSI components.

#### 2. Course Objectives

The students are expected to:

- i. Understand and formulate different number systems, binary logic, and circuits.
- ii. Design combinational and sequential circuits.
- iii. Develop state-machines circuits with flip-flops.

#### 3. Knowledge required

##### Technical

- N/A

##### Analytical

- N/A

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### COURSE OUTLINE

Course No: CSE 205, Level 2/ Term 1, Credit (Contact) Hours: 3 Credits (3hrs/wk)



### 4. Course Outcomes (COs)

| CO No. | CO Statement<br>After undergoing this course, students should be able to:             | Corresponding PO(s)* | Domains and Taxonomy level(s)** | Delivery Method(s) and Activity(-ies) | Assessment Tool(s)                                     |
|--------|---|----------------------|---------------------------------|---------------------------------------|--|
| CO1    | <b>Understand and formulate</b> different number systems, binary logic, and circuits. | PO1 and PO2          | C4                              | Lecture and Demonstration             | Class Tests or Assignments or Projects, and Final Exam |
| CO2    | <b>Design</b> combinational and sequential circuits.                                  | PO3 and PO4          | A4                              | Lecture and Demonstration             | Class Tests or Assignments or Projects, and Final Exam |
| CO3    | <b>Develop</b> state-machines circuits with flip-flops.                               | PO2 and PO3          | C6                              | Lecture and Demonstration             | Class Tests or Assignments or Projects, and Final Exam |

#### \*Program Outcomes (POs)

PO1: Engineering knowledge; PO2: Problem analysis; PO3: Design/development of solutions; PO4: Investigation; PO5: Modern tool usage; PO6: The engineer and society; PO7: Environment and sustainability; PO8: Ethics; PO9: Individual work and teamwork; PO10: Communication; PO11: Project management and finance; PO12: Life-long learning.

#### \*\*Domains

**C-Cognitive:** C1: Knowledge; C2: Comprehension; C3: Application; C4: Analysis; C5: Synthesis; C6: Evaluation

**A-Affective:** A1: Receiving; A2: Responding; A3: Valuing; A4: Organizing; A5: Characterizing

**P-Psychomotor:** P1: Perception; P2: Set; P3: Guided Response; P4: Mechanism; P5: Complex Overt Response; P6: Adaptation; P7: Organization

### 5. Mapping of Knowledge Profile, Complex Engineering Problem Solving and Complex Engineering Activities

| COs | K1 | K2 | K3 | K4 | K5 | K6 | K7 | K8 | P1 | P2 | P3 | P4 | P5 | P6 | P7 | A1 | A2 | A3 | A4 | A5 |
|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| CO1 |    | √  | √  |    |    |    |    |    | √  | √  |    |    |    |    |    | √  |    |    |    |    |
| CO2 |    | √  | √  |    |    |    |    |    | √  | √  |    |    |    |    |    | √  |    | √  |    |    |
| CO3 |    | √  | √  |    | √  | √  |    |    | √  | √  | √  |    |    |    |    |    | √  |    | √  |    |



## K-Knowledge Profile:

**K1:** A systematic, theory-based understanding of the natural sciences applicable to the discipline; **K2:** Conceptually based mathematics, numerical analysis, statistics and the formal aspects of computer and information science to support analysis and modeling applicable to the discipline; **K3:** A systematic, theory-based formulation of engineering fundamentals required in the engineering discipline; **K4:** Engineering specialist knowledge that provides theoretical frameworks and bodies of knowledge for the accepted practice areas in the engineering discipline; much is at the forefront of the discipline; **K5:** Knowledge that supports engineering design in a practice area; **K6:** Knowledge of engineering practice (technology) in the practice areas in the engineering discipline; **K7:** Comprehension of the role of engineering in society and identified issues in engineering practice in the discipline: ethics and the engineer's professional responsibility to public safety; the impacts of engineering activity; economic, social, cultural, environmental and sustainability; **K8:** Engagement with selected knowledge in the research literature of the discipline

## P-Range of Complex Engineering Problem Solving:

**P1:** Cannot be resolved without in-depth engineering knowledge at the level of one or more of K3, K4, K5, K6 or K8 which allows a fundamentals-based, first principles analytical approach; **P2:** Involve wide-ranging or conflicting technical, engineering and other issues; **P3:** Have no obvious solution and require abstract thinking, originality in analysis to formulate suitable models; **P4:** Involve infrequently encountered issues; **P5:** Are outside problems encompassed by standards and codes of practice for professional engineering; **P6:** Involve diverse groups of stakeholders with widely varying needs; **P7:** Are high level problems including many component parts or sub-problems

## A-Range of Complex Engineering Activities:

**A1:** Involve the use of diverse resources (and for this purpose resources include people, money, equipment, materials, information and technologies); **A2:** Require resolution of significant problems arising from interactions between wide-ranging or conflicting technical, engineering or other issues; **A3:** Involve creative use of engineering principles and research-based knowledge in novel ways; **A4:** Have significant consequences in a range of contexts, characterized by difficulty of prediction and mitigation; **A5:** Can extend beyond previous experiences by applying principles-based approaches

## 6. Lecture/ Activity Plan

| Week   | Lecture Topics  | Corresponding CO(s) |
|--------|---|---------------------|
| Week 1 | Introduction to Digital Logic Design<br>Boolean Algebra<br>De Morgan's Theorems<br>Logic gates and their truth tables | CO1                 |
| Week 2 | Canonical forms   | CO1                 |



| Week    | Lecture Topics   | Corresponding CO(s) |
|---------|--|---------------------|
|         | Number Systems   |                     |
| Week 3  | Minimization techniques  | CO1 and CO2         |
| Week 4  | Minimization techniques  | CO1 and CO2         |
| Week 5  | Combinational Logic<br>Arithmetic and data handling logic circuits | CO1 and CO2         |
| Week 6  | Decoders and Encoders  | CO1 and CO2         |
| Week 7  | Multiplexers and Demultiplexers, PLA Design                        | CO1 and CO2         |
| Week 8  | Flip-flops and their construction                                  | CO2                 |
| Week 9  | Synchronous Sequential Logic                                       | CO2 and CO3         |
| Week 10 | Registers and Counters   | CO2 and CO3         |
| Week 11 | Circuit Design with Flip-flops, Registers and Counters             | CO2 and CO3         |
| Week 12 | State minimization and state machines                              | CO2 and CO3         |
| Week 13 | Asynchronous Sequential Logic                                      | CO2 and CO3         |
| Week 14 | Asynchronous Sequential Logic                                      | CO2 and CO3         |

### 7. Assessment Strategy

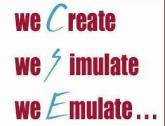
- Class Attendance: Class attendance will be recorded in every class.
- Class Tests/Assignments/Projects: There will be a minimum of 4 (four) Class Tests/Assignments/Projects, out of which the best 3 (three) will be considered in final evaluation.
- Final exam: A comprehensive Final exam will be held at the end of the semester as per the institutional ordinance.

### 8. Distribution of Marks

|                                   |      |
|-----------------------------------|------|
| Attendance:                       | 10 % |
| Class Tests/Assignments/Projects: | 20%  |
| Final Exam:                       | 70%  |
| Total:                            | 100% |

### 9. Textbook/ Reference

- a. Digital Design (5th edition), M. Morris Mano, Michael D. Ciletti
- b. Digital Design: A Pragmatic Approach, Everett L. Johnson, Mohammad A. Karim
- c. Digital Logic Circuit Analysis and Design, Nelson, Victor, Nagle, H., Carroll, Bill, Irwin, David



- d. Switching and Finite Automata Theory, Zvi Kohavi.

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