

Quad Two-Input NAND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7400	9ns	8mA
74LS00	9.5ns	1.6mA
74S00	3ns	15mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7400N • N74LS00N N74S00N	
Plastic SO	N74LS00D N74S00D	
Ceramic DIP		S5400F • S54LS00F S54S00F
Flatpack		S5400W • S54LS00W S54S00W
LLCC		S54LS00G

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

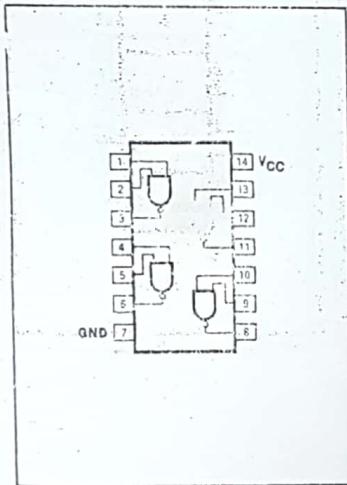
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

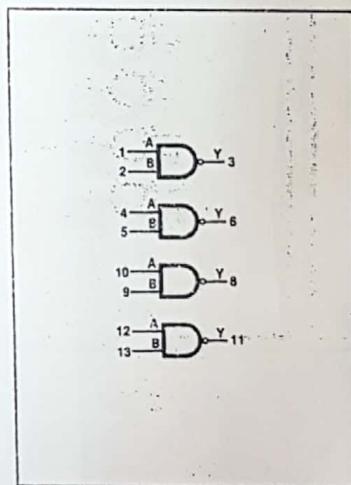
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1 <ul style="list-style-type: none">	1 <ul style="list-style-type: none">	1 <ul style="list-style-type: none">
Y	Output	10 <ul style="list-style-type: none">	10 <ul style="list-style-type: none">	10 <ul style="list-style-type: none">

NOTE
Where a 54/74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, a 54/74S unit load (Sul) is $50\mu A I_{IH}$ and $-2.0mA I_{IL}$, and 54/74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

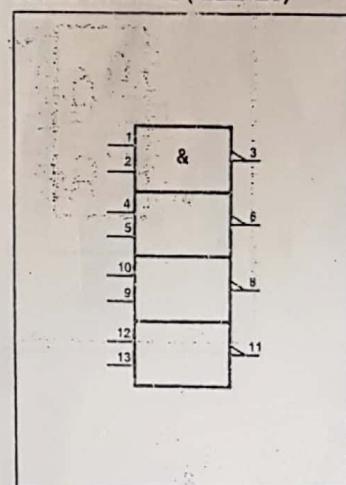
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



INVERTERS**54/7404, LS04, S04****Hex Inverter**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7404	10ns	12mA
74LS04	9.5ns	2.4mA
74S04	3ns	22mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7404N • N74LS04N N74S04N	
Plastic SO	N74LS04D • N74S04D	
Ceramic DIP		S5404F • S54LS04F S54S04F
Flatpack		S5404W • S54LS04W S54S04W
LLCC		S54LS04G

FUNCTION TABLE

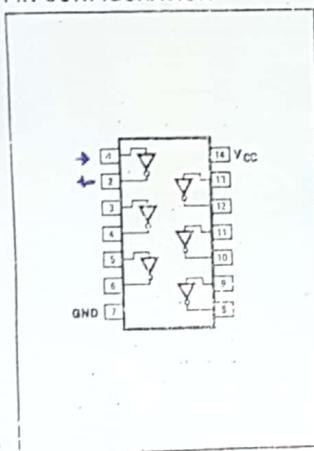
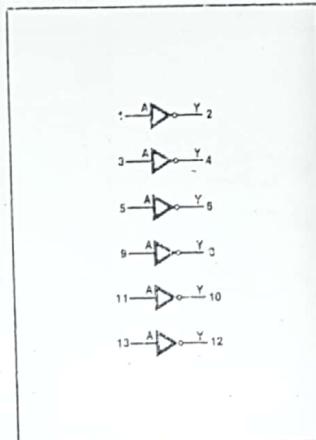
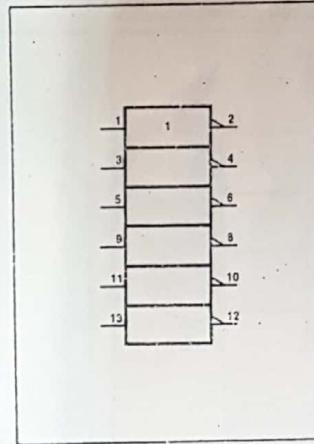
INPUT	OUTPUT
A	Y
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
A	Input	1 <ul style="list-style-type: none">	1 <ul style="list-style-type: none">	1 <ul style="list-style-type: none">
Y	Output	10 <ul style="list-style-type: none">	10 <ul style="list-style-type: none">	10 <ul style="list-style-type: none">

NOTE
Where a 54/74 unit load (ul) is understood to be 40 μA I_{IH} and $-1.5mA$ I_{IL} , a 54/74S unit load (Sul) is 50 μA I_{IH} and $-2.0mA$ I_{IL} , and 54/74LS unit load (LSul) is 20 μA I_{IH} and $-0.4mA$ I_{IL} .

PIN CONFIGURATION**LOGIC SYMBOL****LOGIC SYMBOL (IEEE/IEC)**

GATES

54/7408, LS08, S08

Quad Two-Input AND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7408	15ns	16mA
74LS08	9ns	3.4mA
74S08	5ns	25mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7408N • N74LS08N N74S08N	
Plastic SO	N74LS08N • N74S08N	
Ceramic DIP		S54S08F • S54LS08F
Flatpack		S54S08W • S54LS08W
LLCC		S54LS08G

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

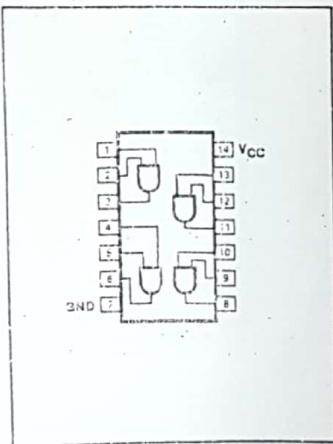
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

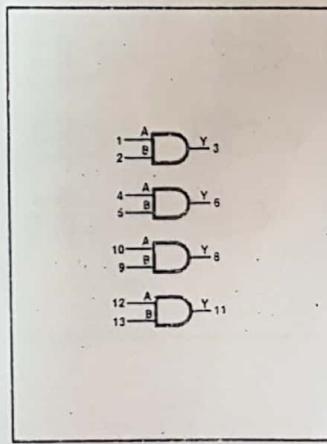
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1 <ul style="list-style-type: none">	1 <ul style="list-style-type: none">	1 <ul style="list-style-type: none">
Y	Output	10 <ul style="list-style-type: none">	10 <ul style="list-style-type: none">	10 <ul style="list-style-type: none">

NOTE
Where a 54/74 unit load (u_l) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, a 54/74S unit load (Su_l) is $50\mu A I_{IH}$ and $-2.0mA I_{IL}$, and 54/74LS unit load (LSu_l) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

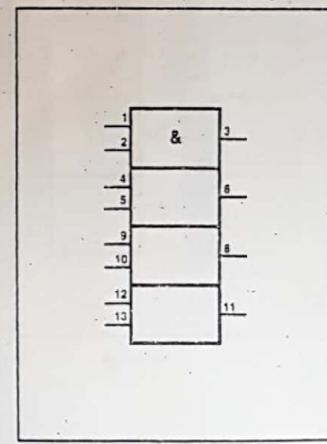
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Triple Three-Input NAND ('10), AND ('11) Gates

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7410	9ns	6mA
74LS10	10ns	1.2mA
74S10	3ns	12mA
7411	10ns	11mA
74LS11	9ns	2.6mA
74S11	5ns	19mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP '10	N7410N • N74LS10N • N74S10N	
'11	N7411N • N74LS11N • N74S11N	
Plastic SO '10	N74LS10D • N74S10D	
Plastic SO '11	N74LS11D • N74S11D	
Ceramic DIP '10		S54S10F • S54LS10F
'11		S5411F • S54S11F
Flatpack '10		S54S10W • S54LS10W
'11		S5411W • S54S11W
LLCC '10		S54LS10G

FUNCTION TABLE

INPUTS			OUTPUTS	
A	B	C	$Y(^1C)$	$Y(^11)$
L	L	L	H	L
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	L	H

H = HIGH voltage level

L = LOW voltage level

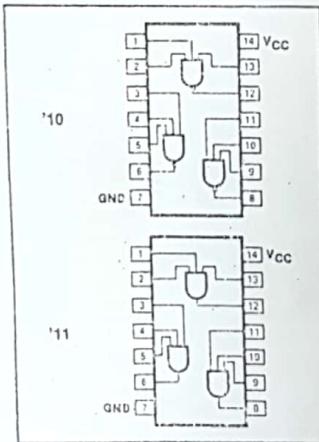
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
A-C	Inputs	1 <ul style="list-style-type: none">	1 <ul style="list-style-type: none">	1 <ul style="list-style-type: none">
Y	Output	10 <ul style="list-style-type: none">	10 <ul style="list-style-type: none">	10 <ul style="list-style-type: none">

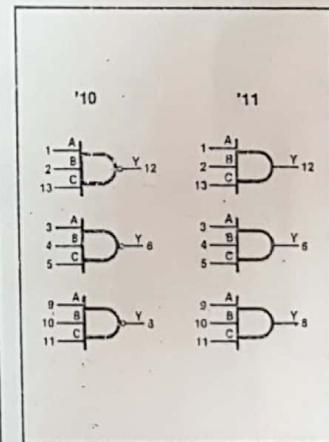
NOTE

Where a 54/74 unit load (l_U) is understood to be $40\mu A l_{IH}$ and $-1.6mA l_{IL}$, a 54/74S unit load (SUL) is $50\mu A l_{IH}$ and $-2.0mA l_{IL}$, and 54/74LS unit load ($LsUL$) is $20\mu A l_{IH}$ and $-0.4mA l_{IL}$.

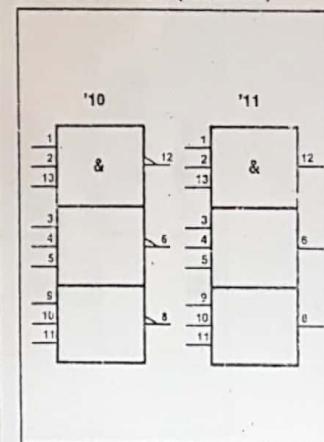
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Dual Four-Input NAND ('20), AND ('21) Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7420	10ns	8mA
74LS20	10ns	0.8mA
74S20	3ns	8mA
7421	12ns	8mA
74LS21	9ns	1.7mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP '20	N7420N • N74LS20N N74S20N	
'21	N7421N • N74LS21N	
Plastic SO	N74LS20D • N74S20D N74LS21D	
Ceramic DIP '20		S5420F • S54LS20F S54S20F
Flatpack '20		S5420W • S54LS20W S54S20W
LLCC		S54LS20G

FUNCTION TABLE

INPUTS				OUTPUTS	
A	B	C	D	$Y('20)$	$Y('21)$
L	X	X	X	H	L
X	L	X	X	H	L
X	X	L	X	H	L
X	X	X	L	H	L
H	H	H	H	L	H

H = HIGH voltage level

L = LOW voltage level

X = Don't care

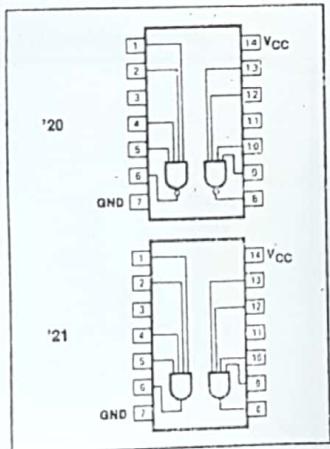
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
A-D	Inputs	1 <ul style="list-style-type: none">	1 <ul style="list-style-type: none">	1 <ul style="list-style-type: none">
Y	Output	10 <ul style="list-style-type: none">	10 <ul style="list-style-type: none">	10 <ul style="list-style-type: none">

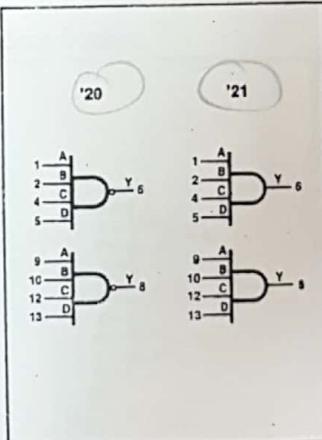
NOTE

Where a 54/74 unit load (U_L) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, a 54/74S unit load (SUL) is $50\mu A I_{IH}$ and $-2.0mA I_{IL}$, and 54/74LS unit load ($LSUL$) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

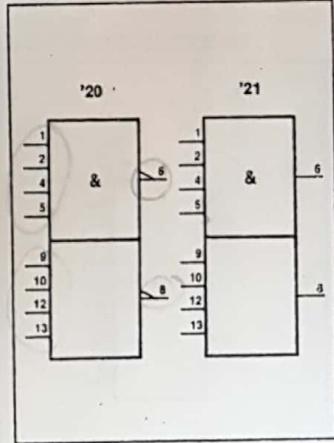
PIN CONFIGURATION



LOGIC SYMBOL



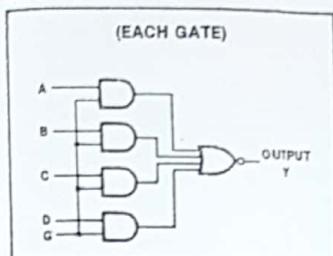
LOGIC SYMBOL (IEEE/IEC)



Dual Four-Input NOR Gate With Strobe

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7425	9ns	9mA

LOGIC DIAGRAM



ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7425N	
Ceramic DIP		S5425F
Flatpack		S5425W

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	G	Y
X	X	X	X	L	H
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	H	H	L
X	X	X	H	H	L
L	L	L	L	H	H

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74
A-D	Inputs	1 <ul style="list-style-type: none">i
G	Input	4 <ul style="list-style-type: none">i
Y	Output	10 <ul style="list-style-type: none">i

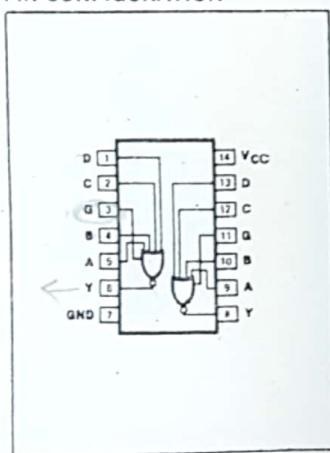
H = HIGH voltage level

L = LOW voltage level

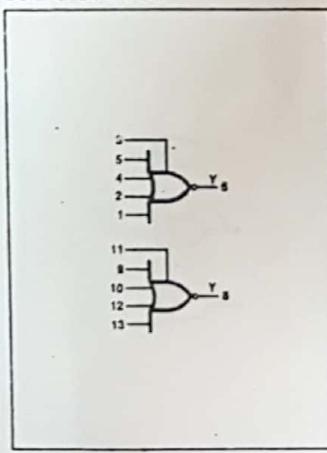
X = Don't care

NOTE
Where a 54/74 unit load (μ) is understood to be $40\mu A$ I_{OH} and $-1.6mA$ I_{OL} .

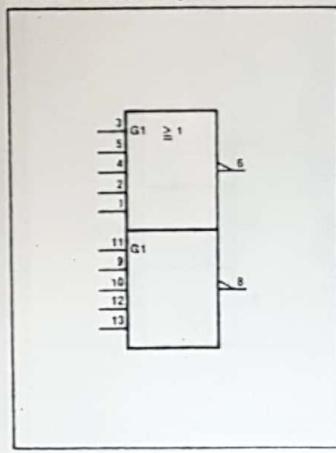
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



GATES**54/7427, LS27****Triple Three-Input NOR Gate**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7427	9ns	13mA
74LS27	10ns	2.7mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7427N • N74LS27N	
Plastic SO	N74LS27D	

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

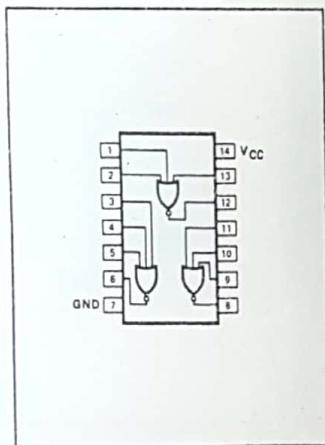
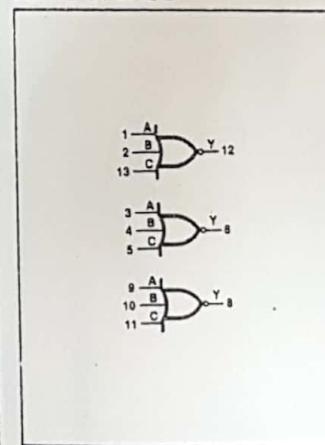
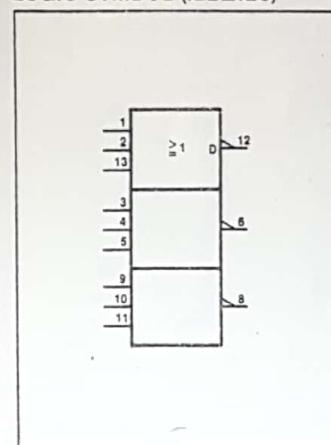
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
A-C	Inputs	1 <ul style="list-style-type: none">I	1 <ul style="list-style-type: none">LS
Y	Output	10 <ul style="list-style-type: none">I	10 <ul style="list-style-type: none">LS

NOTE
Where a 54/74 unit load (

I
) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} , a 54/74LS unit load (

LS
) is 20 μ A I_{IH} and -0.4mA I_{IL} .

PIN CONFIGURATION**LOGIC SYMBOL****LOGIC SYMBOL (IEEE/IEC)**

GATES

54/7430, LS30

Eight-Input NAND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7430	11ns	2mA
74LS30	11ns	0.5mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7430N • N74LS30N	
Plastic SO	N74LS30D	
Ceramic DIP		S54LS30F
Flatpack		S54LS30W

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
H	H	H	H	H	H	H	H	L

H = HIGH voltage level

L = LOW voltage level

X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

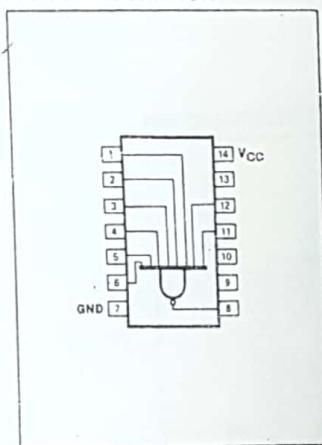
PINS	DESCRIPTION	54/74	54/74LS
A-H	Inputs	1 <ul style="list-style-type: none">	1LS <ul style="list-style-type: none">
Y	Output	10 <ul style="list-style-type: none">	10LS <ul style="list-style-type: none">

NOTE

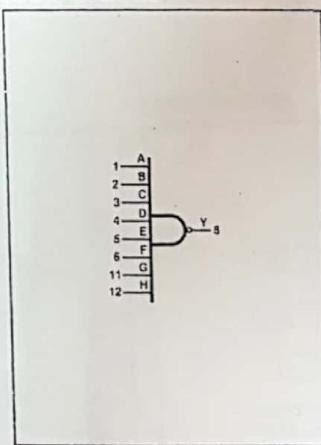
Where a 54/74 unit load (μ l) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and 54/74LS unit load (LS

) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

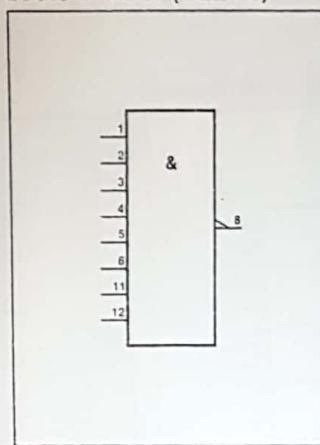
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC PRODUCTS

GATES**54/7432, LS32, S32****Quad Two-Input OR Gate**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7432	12ns	19mA
74LS32	14ns	4.0mA
74S32	4ns	28mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7432N • N74LS32N N74S32N	
Plastic SO	N74LS32D • N74S32D	
Ceramic DIP		S5432F • S54LS32F
Flatpack		S5432W • S54LS32W
LLCC		S54LS32G

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

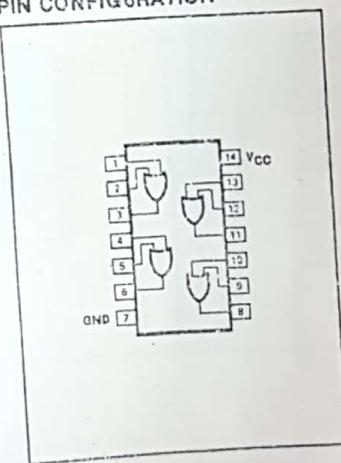
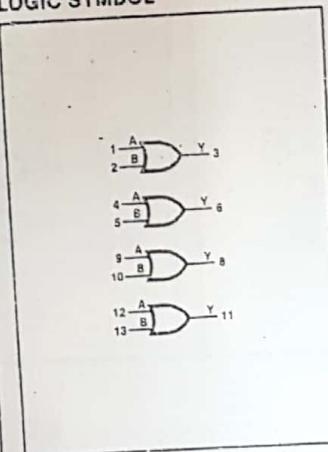
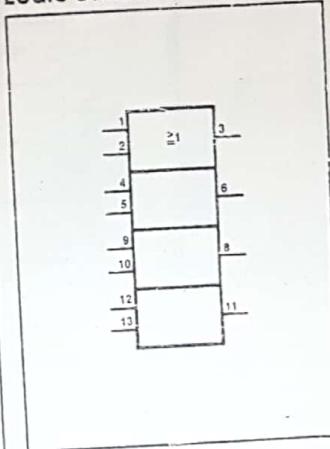
H = HIGH voltage level

L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1 <ul style="list-style-type: none">	1 <ul style="list-style-type: none">	1 <ul style="list-style-type: none">
Y	Output	10 <ul style="list-style-type: none">	10 <ul style="list-style-type: none">	10 <ul style="list-style-type: none">

NOTE
 Where a 54/74 unit load (u_l) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, a 54/74S unit load (Su_l) is $50\mu A I_{IH}$ and $-2.0mA I_{IL}$, and a 54/74LS unit load (LSu_l) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

PIN CONFIGURATION**LOGIC SYMBOL****LOGIC SYMBOL (IEEE/IEC)**

Quad Two-Input NAND Buffers (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7438	13ns	28mA
74LS38	19ns	3.5mA
74S38	6.5ns	33mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7438N • N74LS38N N74S38N	
Plastic SO	N74S38D • N74LS38D	

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

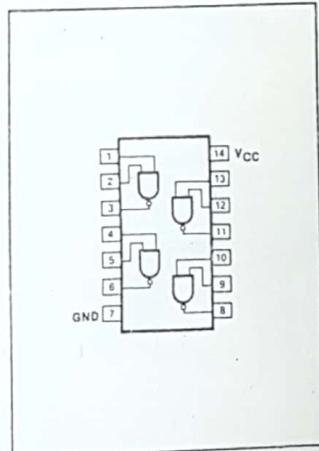
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

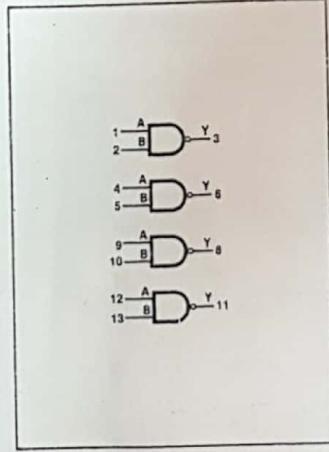
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1 <ul style="list-style-type: none">	2 <ul style="list-style-type: none">	1 <ul style="list-style-type: none"> Sul
Y	Output	30 <ul style="list-style-type: none">	30 <ul style="list-style-type: none"> Sul	30 <ul style="list-style-type: none"> Sul

NOTE
Where a 54/74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, a 54/74S unit load (Sul) is $50\mu A I_{IH}$ and $-2.0mA I_{IL}$, and 54/74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

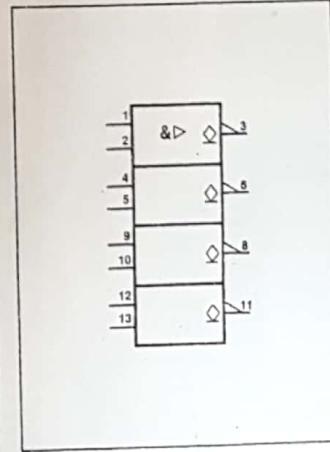
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOPS

54/7473, LS73

DESCRIPTION

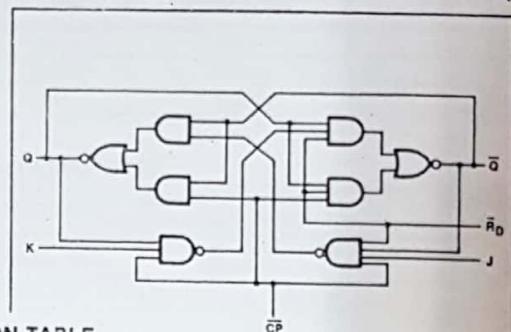
The '73 is a dual flip-flop with individual J, K, Clock and direct Reset inputs. The 7473 is positive pulse-triggered, JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW transition. For the 7473, the J and K inputs should be stable while the Clock is HIGH for conventional operation.

The 74LS73 is a negative edge-triggered flip-flop. The J and K inputs must be stable one setup time prior to the HIGH-to-LOW Clock transition for predictable operation.

The Reset (\bar{R}_D) is an asynchronous active LOW input. When LOW, it overrides the Clock and Data inputs, forcing the Q output LOW and the \bar{Q} output HIGH.

LOGIC DIAGRAM

Dual J-K Flip-Flop



FUNCTION TABLE

OPERATING MODE	INPUTS		OUTPUTS			
	\bar{R}_D	$\bar{C}P(b)$	J	K	Q	\bar{Q}
Asynchronous Reset (Clear)	L	X	X	X	L	H
Toggle	H	—	h	h	\bar{q}	q
Load "0" (Reset)	H	—	l	h	L	H
Load "1" (Set)	H	—	h	l	H	L
Hold "no change"	H	—	l	l	q	\bar{q}

H = HIGH voltage level steady state.

h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.^(a)

l = LOW voltage level steady state.

— = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.^(a)

q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.

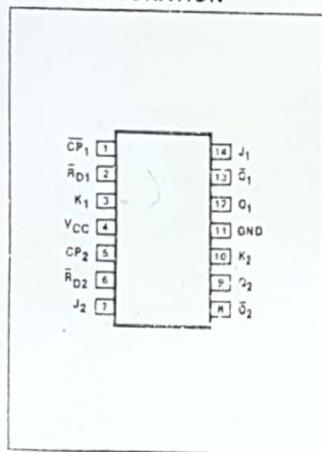
X = Don't care.

— = Positive Clock pulse.

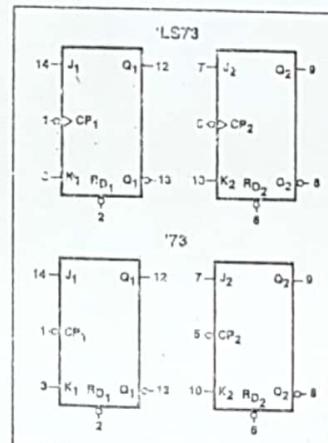
NOTES

- a. The J and K inputs of the 7473 must be stable while the Clock is HIGH for conventional operation.
- b. The 74LS73 is edge triggered. Data must be stable one setup time prior to the negative edge of the Clock for predictable operation.

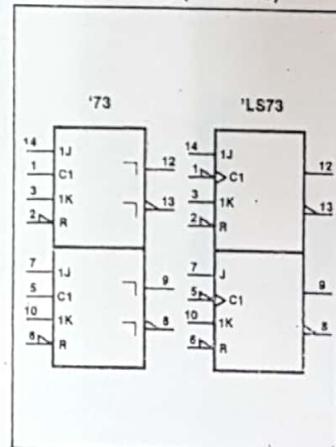
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



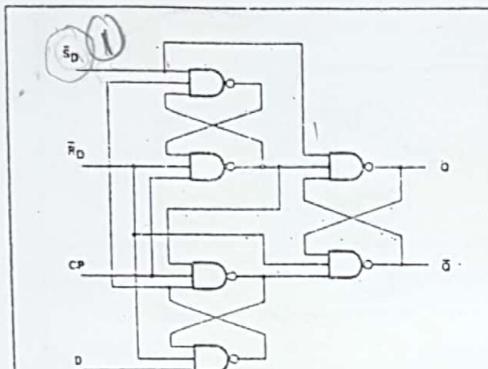
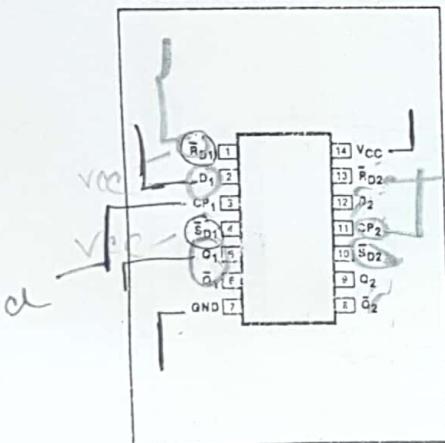
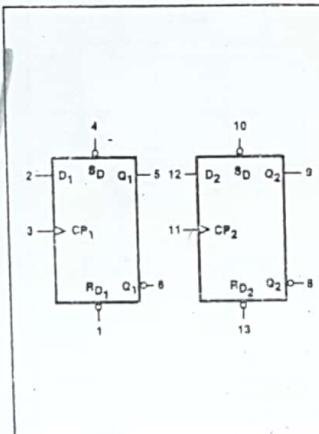
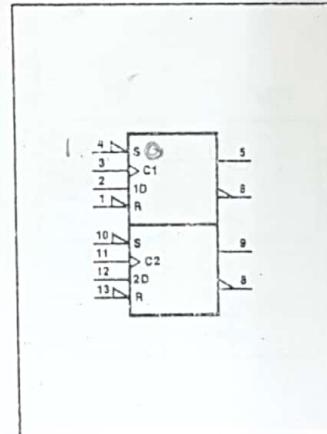
FLIP-FLOPS

54/7474, LS74A, 574

Dual D-Type Flip-Flop**DESCRIPTION**

The '74 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock and Set and Reset inputs; also complementary Q and \bar{Q} outputs.

Set (S_D) and Reset (R_D) are asynchronous active-LOW inputs and operate independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one setup time prior to the LOW-to-HIGH clock transition for predictable operation. Although the Clock input is level-sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock-to-output delay time for reliable operation.

LOGIC DIAGRAM**PIN CONFIGURATION****LOGIC SYMBOL****LOGIC SYMBOL (IEEE/IEC)**

FLIP-FLOPS

54/7476, LS76

Dual J-K Flip-Flop

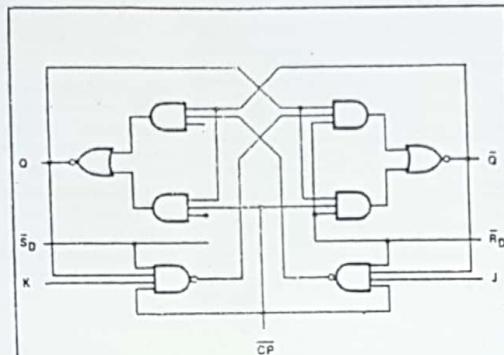
DESCRIPTION

The '76 is a dual J-K flip-flop with individual J, K, Clock, Set and Reset inputs. The 7476 is positive pulse-triggered. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW Clock transition. The J and K inputs must be stable while the Clock is HIGH for conventional operation.

The 74LS76 is a negative edge-triggered flip-flop. The J and K inputs must be stable only one setup time prior to the HIGH-to-LOW Clock transition.

The Set (\bar{S}_D) and Reset (\bar{R}_D) are asynchronous active LOW inputs. When LOW, they override the Clock and Data inputs, forcing the outputs to the steady state levels as shown in the Function Table.

LOGIC DIAGRAM



ORDERING CODE

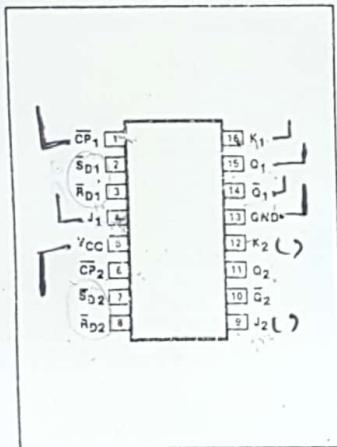
PACKAGES	COMMERCIAL RANGES		MILITARY RANGES	
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7476N	N74LS76N	S5476F	S54LS76F
Ceramic DIP			S5476W	S54LS76W
Flatpack				

FUNCTION TABLE

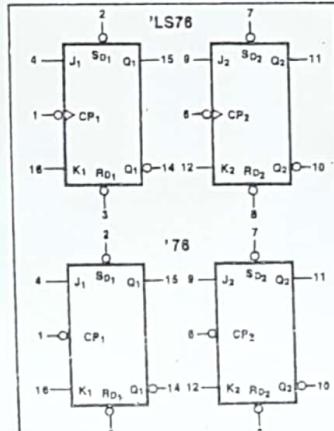
OPERATING MODE	INPUTS		OUTPUTS				
	\bar{S}_D	\bar{R}_D	CP	J	K	Q	\bar{Q}
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined ^[a]	L	L	X	X	X	H	H
Toggle	H	H	—	h	h	—	q
Load "0" (Reset)	H	H	—	I	I	L	H
Load "1" (Set)	H	H	—	h	I	H	L
Hold "no change"	H	H	—	I	I	q	—

- = HIGH voltage level steady state.
- = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.^[c]
- = LOW voltage level steady state.
- = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.^[c]
- = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.

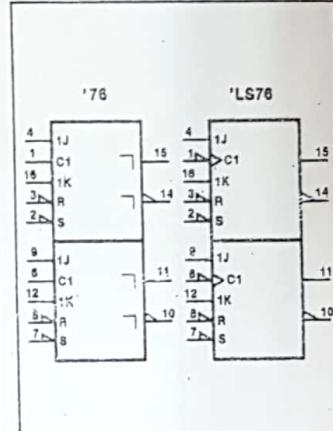
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ADDERS

54/7483, LS83A

4-Bit Full Adder

- High speed 4-bit binary addition
- Cascadeable in 4-bit increments
- LS83A has fast internal carry lookahead
- See '283 for corner power pin version

DESCRIPTION

The '83 adds two 4-bit binary words (A_1 , plus B_1) plus the incoming carry. The binary sum appears on the Sum outputs (Σ_1 - Σ_4) and the outgoing carry (C_{out}) according to the equation:

$$\begin{aligned} C_{\text{in}} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) \\ + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 \\ + 16C_{\text{out}} \end{aligned}$$

Where (+) = plus.

Due to the symmetry of the binary add function, the '83 can be used with either all active-HIGH operands (positive logic) or with all active-LOW operands (negative logic). See Function Table. With active-HIGH inputs, C_{in} cannot be left open; it must be held LOW when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus C_{in} , A_1 , B_1 , can arbitrarily be assigned to pins 10, 11, 13, etc.

TYPE	TYPICAL ADD TIMES (Two 8-bit Words)	TYPICAL SUPPLY CURRENT (Total)
7483	23ns	66mA
74LS83A	25ns	19mA

ORDERING CODE

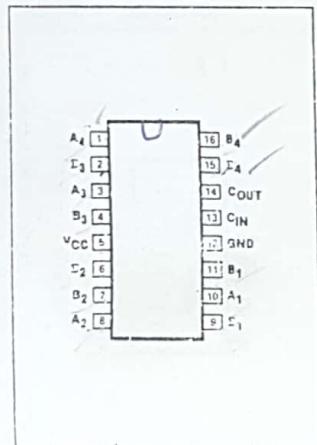
PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$
Plastic DIP	N7483N • N74LS83AN	
Plastic SO	N74LS83AD	
Ceramic DIP		S5483F • S54LS83AF
Flatpack		S5483W • S54LS83AW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

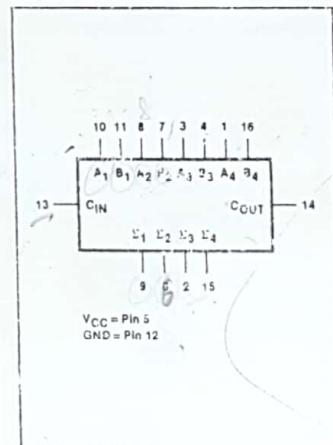
PINS	DESCRIPTION	54/74	54/74LS
$A_1, B_1, A_3, B_3, C_{\text{IN}}$	Inputs	2 <u>l</u>	
A_2, B_2, A_4, B_4	Inputs	1 <u>l</u>	
A, B	Inputs		2LS <u>l</u>
C_{IN}	Input		1LS <u>l</u>
Sum	Outputs	10 <u>l</u>	10LS <u>l</u>
Carry	Output	5 <u>l</u>	10LS <u>l</u>

NOTE
Where a 54/74 unit load (l) is understood to be $40\mu\text{A } I_{IH}$ and $-1.6\text{mA } I_{IL}$ and a 54/74LS unit load (LSl) is $20\mu\text{A } I_{IH}$ and $-0.4\text{mA } I_{IL}$.

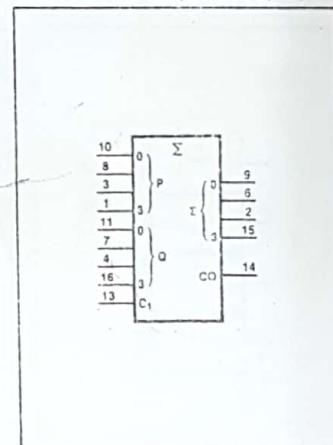
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



GATES

54/7486, LS86, S86

Quad Two-Input Exclusive-OR Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7486	14ns	30mA
74LS86	10ns	6.1mA
74S86	7ns	50nA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7486N • N74LS86N N74S86N	
Plastic SO	N74LS86D • N74S86D	
Ceramic DIP		S5486F • S54LS86F S54S86F
Flatpack		S5486W • S54LS86W S54S86W
LLCC		S54LS86G

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH voltage level

L = LOW voltage level

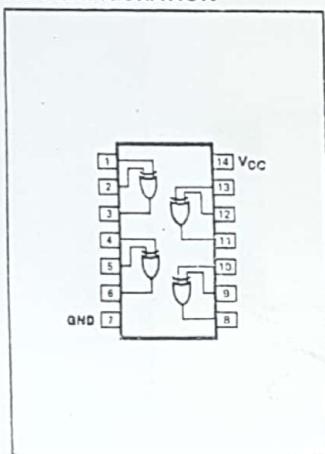
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1 <ul style="list-style-type: none">	1 <ul style="list-style-type: none">	1 <ul style="list-style-type: none">
Y	Output	10 <ul style="list-style-type: none">	10 <ul style="list-style-type: none">	10 <ul style="list-style-type: none">

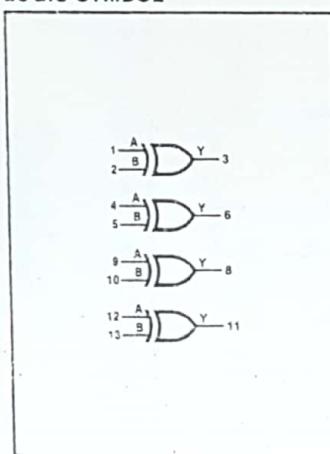
NOTE

Where a 54/74 unit load (u_l) is understood to be $40\mu A$ I_{IH} and $-1.8mA$ I_{IL} , a 54/74S unit load (Su_l) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and a 54/74LS unit load (LSu_l) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

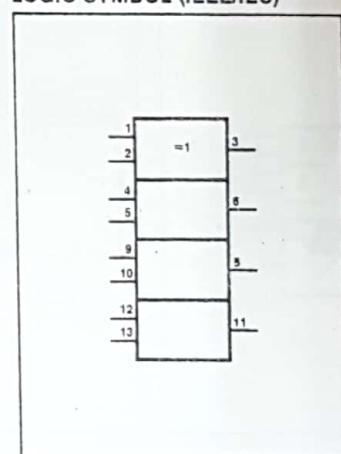
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



COUNTERS

54/7490, LS90

DESCRIPTION

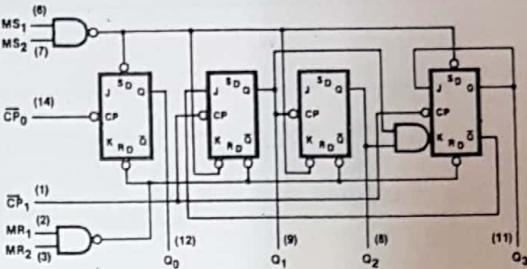
The '90 is a 4-bit, ripple-type Decade Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-five section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset (MR₁, MR₂) is provided which overrides both clocks and resets (clears) all the flip-flops. Also provided is a gated AND asynchronous Master Set (MS₁, MS₂) which overrides the clocks and the MR inputs, setting the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a BCD (8421) counter the \overline{CP}_1 input must be externally connected to the Q_0 output. The \overline{CP}_0 input receives the incoming count producing a BCD count sequence. In a symmetrical Bi-quinary divide-by-ten counter the Q_3 output must be connected externally to the \overline{CP}_0 input. The input count is then applied to the CP₁ input and a divide-by-ten square wave is obtained at

LOGIC DIAGRAM

Decade Counter

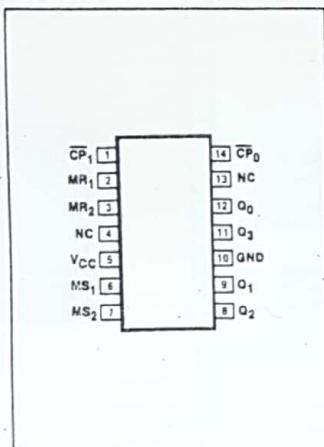
MODE SELECTION—
FUNCTION TABLE

RESET/SET INPUTS				OUTPUTS			
MR ₁	MR ₂	MS ₁	MS ₂	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	X	Count		
X	L	X	L	L	Count		
L	X	X	L	L	Count		
H	L	L	X	X	Count		

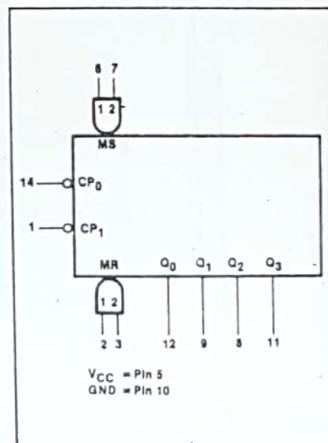
output Q_0 . To operate as a divide-by-two and a divide-by-five counter no external interconnections are required. The first flip-flop is used as a binary element for the

divide-by-two function (\overline{CP}_0 as the input and Q_0 as the output). The \overline{CP}_1 input is used to obtain a divide-by-five operation at the Q_3 output.

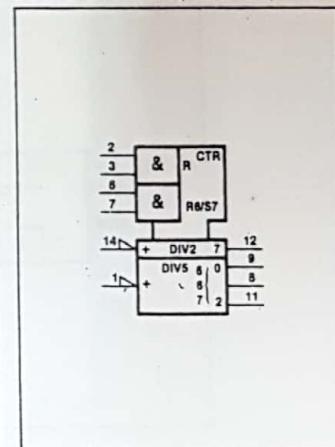
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



REGISTER

54/7491A

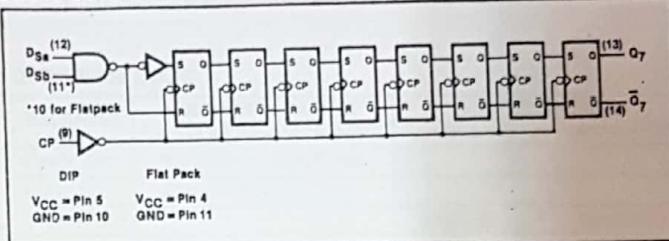
8-Bit Shift Register

- 8-bit serial-in-serial-out shift register
- Common buffered clock
- 2-input gate for serial data entry
- True and Complement outputs

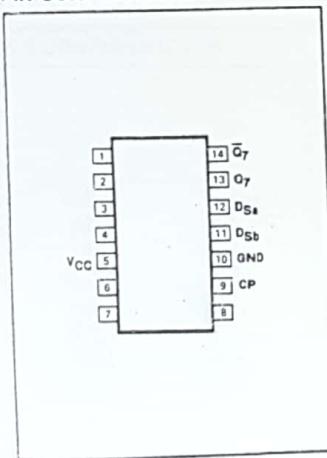
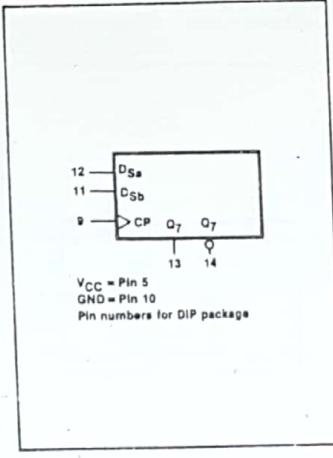
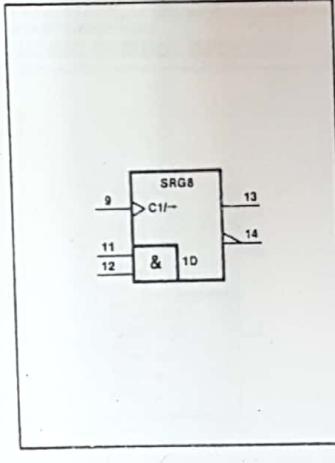
DESCRIPTION

The '91A is an 8-bit serial-in-serial-out shift register. The serial data is entered through a 2-input AND gate (D_{Sa} and D_{Sb}). HIGH data is entered when both D_{Sa} and D_{Sb} are HIGH. LOW data is entered when either Serial Data Input is LOW. The Data Inputs are edge-triggered and must be stable just one setup time prior to the LOW-to-HIGH transition of the Clock input (CP) for predictable operation. The data is shifted one bit to the right ($Q_0 - Q_1 - \dots - Q_7$) synchronous with each LLOW-to-HIGH clock transition. The '91A has no reset capacity, so initialization requires the shifting in of at least 8 bits of known data. Once the register is fully loaded, the Q output follows the Serial Inputs delayed by eight clock pulses. The Complement (\bar{Q}) output from the last stage is also available for simpler decoding applications.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
7491A	18MHz	35mA

LOGIC DIAGRAM**MODE SELECT—FUNCTION TABLE**

OPERATING MODE	INPUTS			FIRST STAGE		OUTPUTS	
	CP	D_{Sa}	D_{Sb}	Q_0	\bar{Q}_0	Q_7	\bar{Q}_7
Shift, reset first stage	I	I	X	L	H	Q_8	\bar{Q}_8
Shift, set first stage	I	X	I	L	H	Q_8	\bar{Q}_8

PIN CONFIGURATION**LOGIC SYMBOL****LOGIC SYMBOL (IEEE/IEC)**

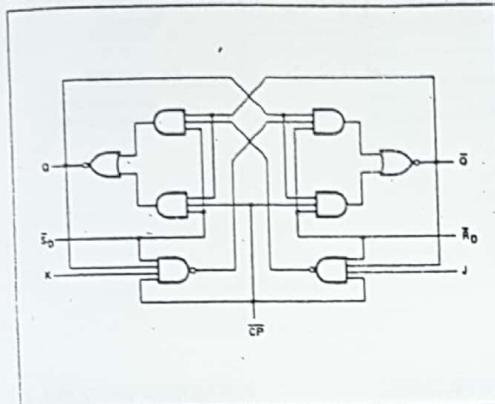
Dual J-K Edge-Triggered Flip-Flop

DESCRIPTION

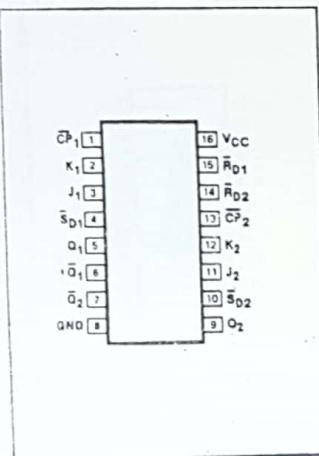
The '112 is a dual J-K negative edge-triggered flip-flop featuring individual J, K, Clock, Set and Reset inputs. The Set (S_D) and Reset (R_D) inputs, when LOW, set or reset the outputs as shown in the Function Table regardless of the levels at the other inputs.

A HIGH level on the Clock (\bar{CP}) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the \bar{CP} is HIGH and the flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of \bar{CP} .

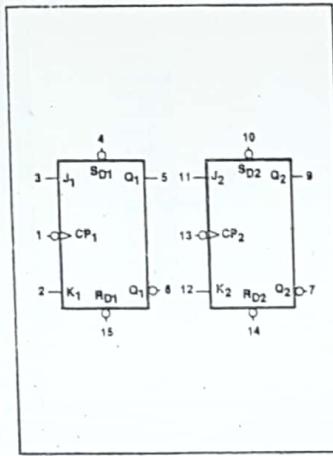
LOGIC DIAGRAM



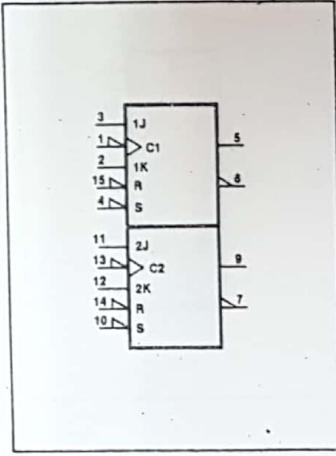
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



DECODERS/DEMULTIPLEXERS

54/74LS138, S138

1-Of-8 Decoder/Demultiplexer

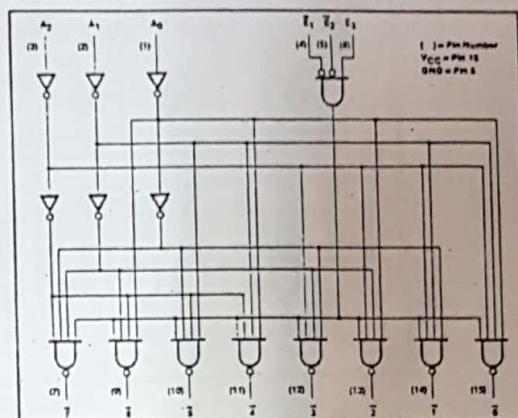
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Direct replacement for Intel 3205

DESCRIPTION

The '138 decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled, provides eight mutually exclusive, active LOW outputs ($\bar{O}-\bar{7}$). The device features three Enable inputs: two active LOW (\bar{E}_1, \bar{E}_2) and one active HIGH (E_3). Every output will be HIGH unless \bar{E}_1 and \bar{E}_2 are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four '138s and one inverter.

The device can be used as an eight output demultiplexer by using one of the active LOW Enable inputs as the Data input and the remaining Enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active HIGH or active LOW state.

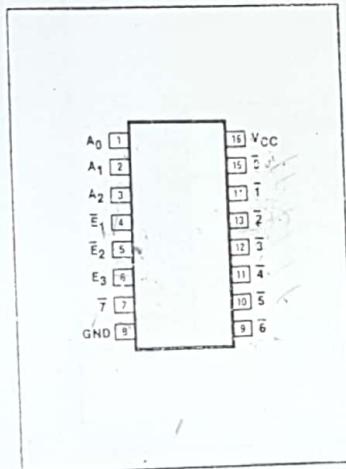
LOGIC DIAGRAM



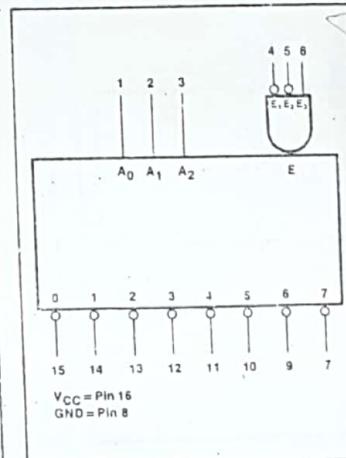
FUNCTION TABLE

INPUTS						OUTPUTS							
\bar{E}_1	\bar{E}_2	E_3	A_3	A_1	A_2	0	1	2	3	4	5	6	7
H	X	X	X	X	X	X	H	H	H	H	H	H	H
X	H	X	X	X	X	X	H	H	H	H	H	H	H
X	X	L	X	X	X	X	H	H	H	H	H	H	H
L	L	H	L	L	L	L	L	H	H	H	H	H	H
L	L	H	H	L	L	L	H	L	H	H	H	H	H
L	L	H	H	H	L	L	H	H	L	H	H	H	H
L	L	H	H	L	H	L	H	H	H	L	H	H	H
L	L	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

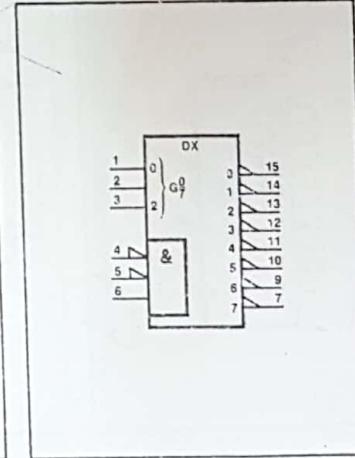
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



DECODER/DRIVER

BCD-To-Decimal Decoder/Driver (Open Collector)

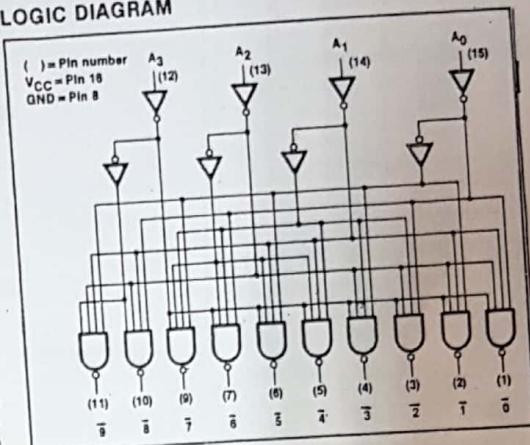
LOGIC DIAGRAM

- 80mA output drive capability
- 15V output breakdown voltage
- See '45 for 30V output voltage
- See '42 for standard TTL outputs

DESCRIPTION

The '145 is a 1-of-10 decoder with Open Collector outputs. This decoder accepts BCD inputs on the A₀ to A₃ address lines and generates 10 mutually exclusive active LOW outputs. When an input code greater than "9" is applied, all outputs are HIGH. This device can therefore be used as a 1-of-8 decoder with A₃ used as an active LOW enable.

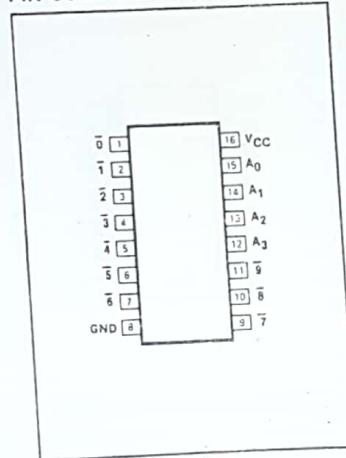
The '145 features an output breakdown voltage of 15V. This device is ideal as a lamp or solenoid driver.



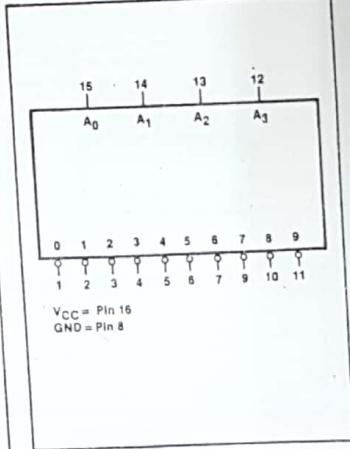
FUNCTION TABLE

A ₃	A ₂	A ₁	A ₀	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	H	L
H	L	L	H	H	H	H	H	H	H	H	H	H	H
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

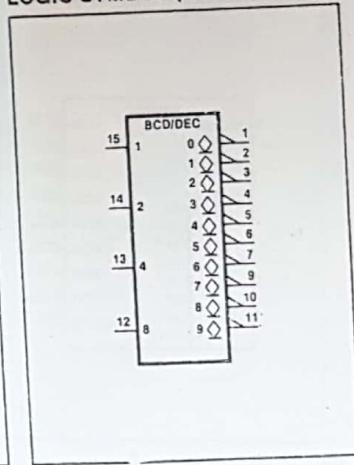
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ENCODER

54/74148

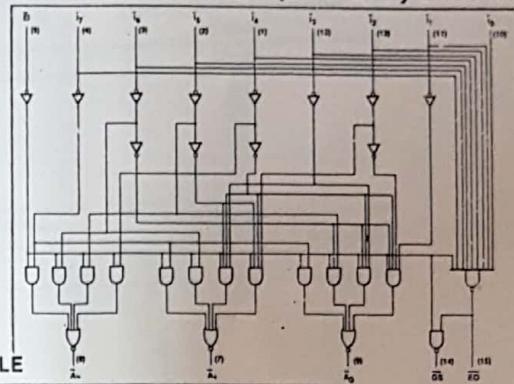
- Code conversions
- Multi-channel D/A converter
- Decimal-to-BCD converter
- Cascading for priority encoding of "N" bits
- Input Enable capability
- Priority encoding—automatic selection of highest priority input line
- Output Enable—active LOW when all inputs HIGH
- Group Signal output—active when any input is LOW

DESCRIPTION

The '148 8-Input priority encoder accepts data from eight active-LOW inputs and provides a binary representation on the three active-LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line \bar{I}_7 having the highest priority.

A HIGH on the Enable Input ($\bar{E}I$) will force all outputs to the inactive (HIGH) state and

LOGIC DIAGRAM 8-Input Priority Encoder



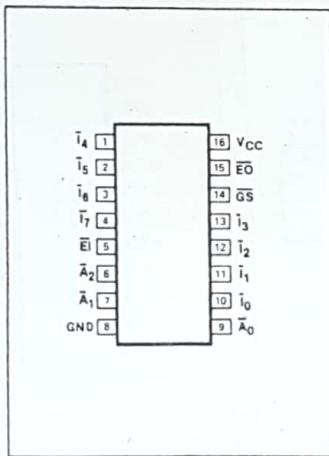
FUNCTION TABLE

$\bar{E}I$	INPUTS								OUTPUTS				
	\bar{I}_0	\bar{I}_1	\bar{I}_2	\bar{I}_3	\bar{I}_4	\bar{I}_5	\bar{I}_6	\bar{I}_7	$\bar{G}S$	\bar{A}_0	\bar{A}_1	\bar{A}_2	$\bar{E}O$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	L	H	H
L	X	X	X	L	H	H	H	H	L	L	H	L	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

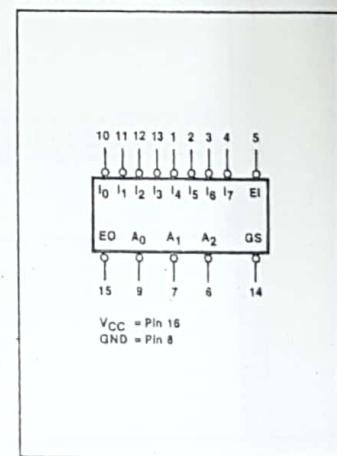
allow new data to settle without producing erroneous information at the outputs.

any input is LOW; this indicates when any input is active. The $\bar{E}O$ is active-LOW when all inputs are HIGH. Using the Enable Output along with the Enable Input allows priority encoding of N input signals. Both $\bar{E}O$ and $\bar{G}S$ are active-HIGH when the Enable Input is HIGH.

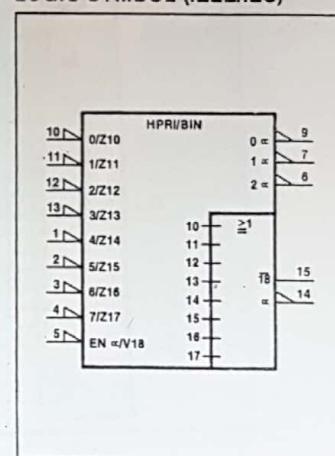
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



MULTIPLEXER

54/74150

16-Input Multiplexer

- Select data from 16 sources
- Demultiplexing capability
- Active-LOW enable or strobe
- Inverting data output

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74150	17ns	40mA

DESCRIPTION

The '150 is a logical implementation of a single-pole, 16-position switch with the switch position controlled by the state of four Select inputs, S_0 , S_1 , S_2 , S_3 . The Multiplexer output (\bar{Y}) inverts the selected data. The Enable input (E) is active-LOW. When \bar{E} is HIGH the \bar{Y} output is HIGH regardless of all other inputs. In one package the '150 provides the ability to select from 16 sources of data or control information.

ORDERING CODE

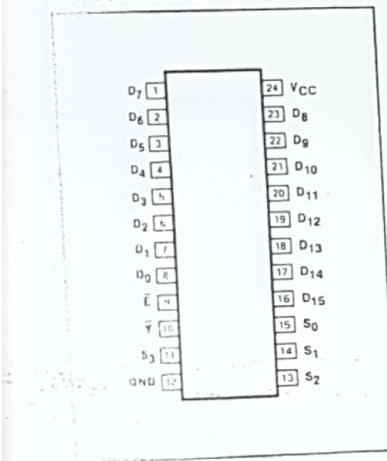
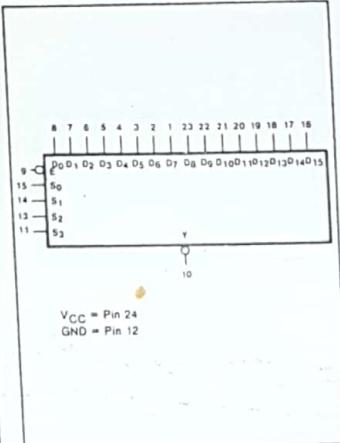
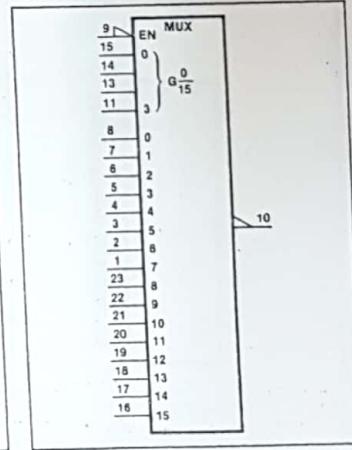
PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74150N	

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74
All	Inputs	1 <ul style="list-style-type: none">
\bar{Y}	Output	10 <ul style="list-style-type: none">

NOTE

A 54/74 unit load (u_l) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

PIN CONFIGURATION**LOGIC SYMBOL****LOGIC SYMBOL (IEEE/IEC)**

MULTIPLEXERS

54/74151, LS151, S151

8-Input Multiplexer

- Multifunction capability
- Complementary outputs
- See '251 for 3-state version

DESCRIPTION

The '151 is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0 , S_1 , S_2 . True (Y) and Complement (\bar{Y}) outputs are both provided. The Enable Input (E) is active LOW. When E is HIGH, the \bar{Y} output is HIGH and the Y output is LOW, regardless of all other inputs. The logic function provided at the output is:

$$\begin{aligned} Y = & \bar{E} \cdot (I_0 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_1 \cdot S_0 \cdot \bar{S}_1 \cdot \bar{S}_2 \\ & + I_2 \cdot \bar{S}_0 \cdot S_1 \cdot \bar{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \bar{S}_2 \\ & + I_4 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \bar{S}_1 \cdot S_2 \\ & + I_6 \cdot \bar{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2). \end{aligned}$$

In one package the '151 provides the ability to select from eight sources of data or control information. The device can provide any logic function of four variables and its negation with correct manipulation.

TYPE	TYPICAL PROPAGATION DELAY (Enable to \bar{Y})	TYPICAL SUPPLY CURRENT (Total)
74151	18ns	29mA
74LS151	12ns	6mA
74S151	9ns	45mA

ORDERING CODE

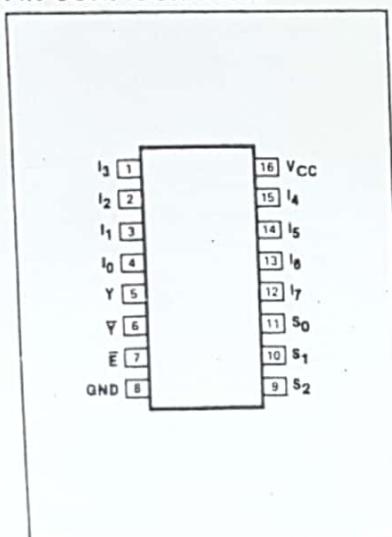
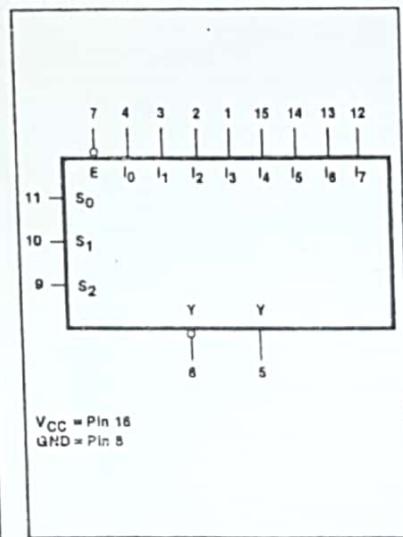
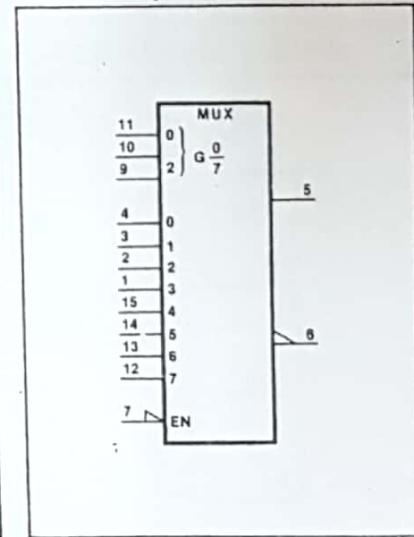
PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74151N • N74LS151N N74S151N	
Plastic SO	N74LS151D • N74S151D	
Ceramic DIP		S54151F • S54LS151F S54S151F
Flatpack		S54151W • S54LS151W S54S151W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
All	Inputs	1 <ul style="list-style-type: none">	1 <ul style="list-style-type: none">	1 <ul style="list-style-type: none">
All	Outputs	10 <ul style="list-style-type: none">	10 <ul style="list-style-type: none">	10 <ul style="list-style-type: none">

NOTE

Where a 54/74 unit load (u_l) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , and a 54/74S unit load (Su_l) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and a 54/74LS unit load (LSu_l) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

PIN CONFIGURATION**LOGIC SYMBOL****LOGIC SYMBOL (IEEE/IEC)**

MULTIPLEXERS

54/74153, LS153, S153

- Non-inverting outputs
- Separate Enable for each section
- Common Select inputs
- See '253 for 3-State version

DESCRIPTION

The '153 is a dual 4-input multiplexer that can select 2 bits of data from up to four sources under control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables (\bar{E}_a, \bar{E}_b) which can be used to strobe the outputs independently. Outputs (Y_a, Y_b) are forced LOW when the corresponding Enables (\bar{E}_a, \bar{E}_b) are HIGH.

The device is the logical implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

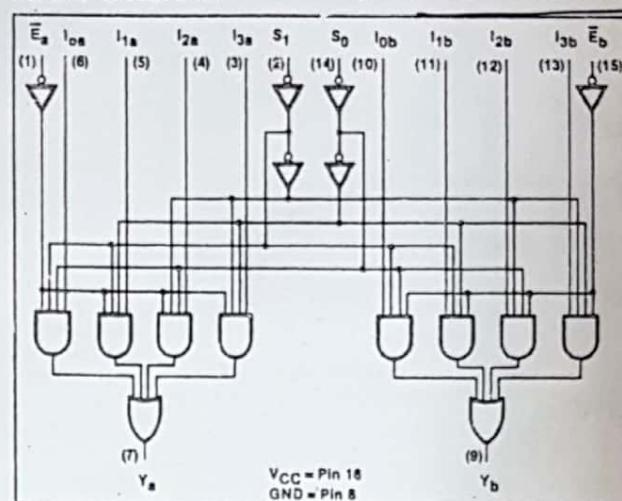
$$Y_a = \bar{E}_a \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Y_b = \bar{E}_b \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

The '153 can be used to move data to a common output bus from a group of registers. The state of the Select inputs would

LOGIC DIAGRAM

Dual 4-Line To 1-Line Multiplexer



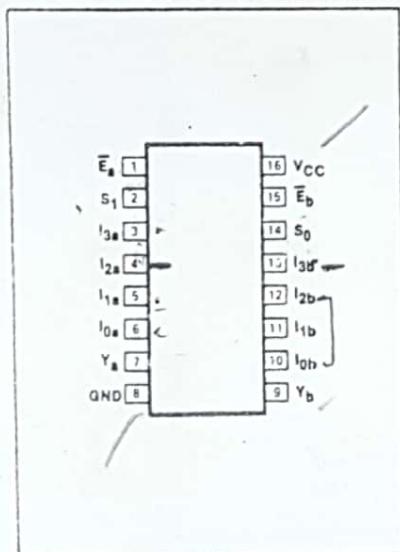
FUNCTION TABLE

SELECT INPUTS		INPUTS (a or b)				OUTPUT	
S_0	S_1	\bar{E}	I_0	I_1	I_2	I_3	Y
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

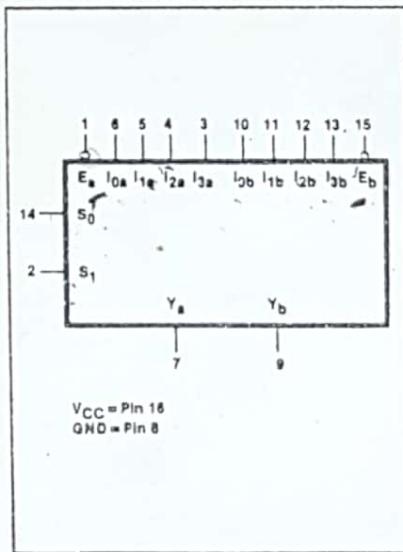
determine the particular register from which the data came. An alternative application is as a function generator. The de-

vice can generate two functions or three variables. This is useful for implementing highly irregular random logic.

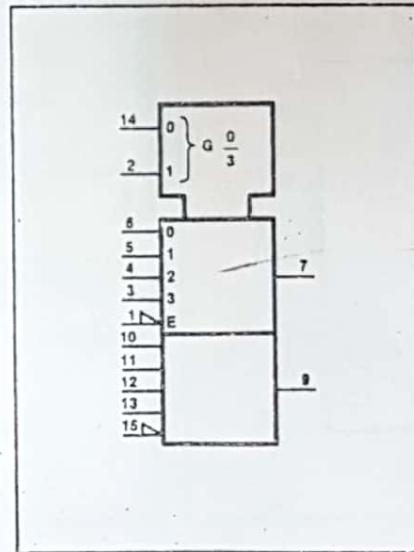
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC PRODUCTS

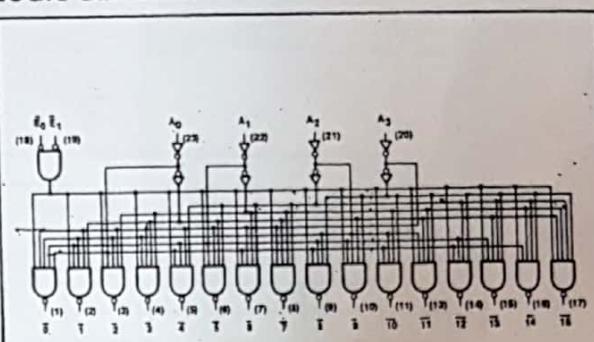
DECODER/DEMULTIPLEXERS**54/74154, LS154****LOGIC DIAGRAM****1-of-16 Decoder/Demultiplexer**

- 16-line demultiplexing capability
- Mutually exclusive outputs
- 2-input enable gate for strobing or expansion

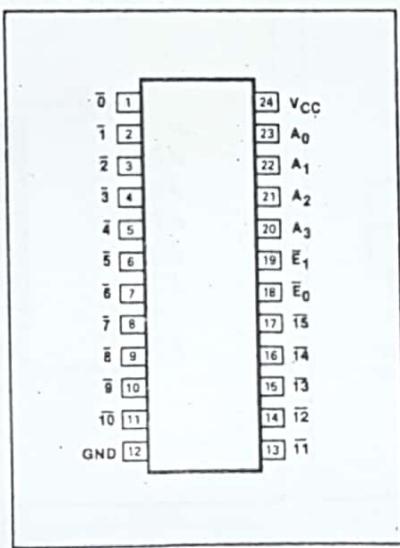
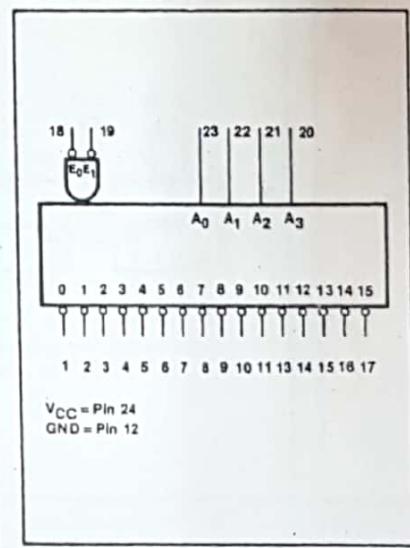
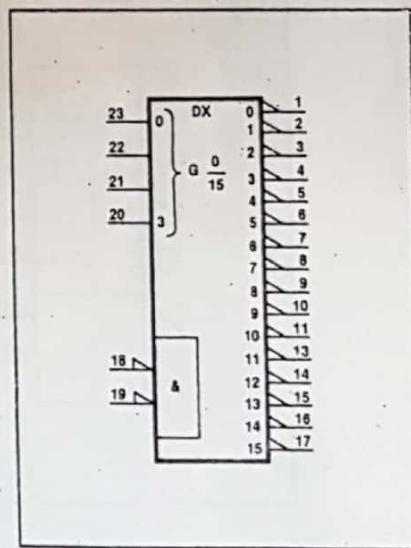
DESCRIPTION

The '154 decoder accepts four active HIGH binary address inputs and provides 16 mutually exclusive active LOW outputs. The 2-Input enable gate can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or it can be used for expansion of the decoder. The enable gate has two AND'ed inputs which must be LOW to enable the outputs.

The '154 can be used as a 1-of-16 demultiplexer by using one of the enable inputs as the multiplexed data input. When the other enable is LOW, the addressed output will follow the state of the applied data.

**FUNCTION TABLE**

INPUTS						OUTPUTS															
E ₀	E ₁	A ₃	A ₂	A ₁	A ₀	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	
L	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	
L	L	L	H	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	
L	L	L	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	
L	L	L	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	
L	L	L	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	
L	L	L	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	
L	L	L	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	
L	L	L	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	

PIN CONFIGURATION**LOGIC SYMBOL****LOGIC SYMBOL (IEEE/IEC)**

DECODERS/DEMULTIPLEXERS

54/74155, LS155

Dual 2-Line To 4-Line Decoder/Demultiplexer

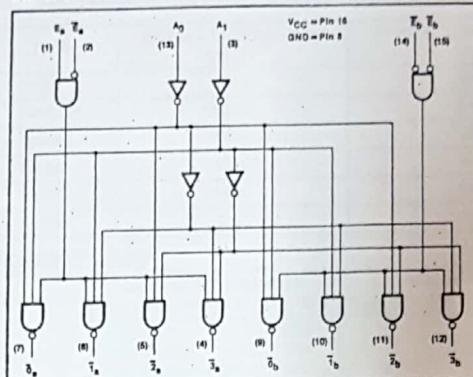
- Common Address inputs
- True or complement data demultiplexing
- Dual 1-of-4 or 1-of-8 decoding
- Function generator applications

DESCRIPTION

The '155 is a Dual 1-of-4 Decoder/Demultiplexer with common Address Inputs and separate gated Enable inputs. Each decoder section, when enabled, will accept the binary weighted Address input (A_0, A_1) and provide four mutually exclusive active-LOW outputs ($\bar{0}-\bar{3}$). When the enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

Both decoder sections have a 2-input enable gate. For decoder "a" the enable gate requires one active-HIGH input and one active-LOW input (E_a, \bar{E}_a). Decoder "a" can accept either true or complemented data in demultiplexing applications, by using the \bar{E}_a or E_a inputs respectively. The decoder "b" enable gate requires two active-LOW inputs (\bar{E}_b, \bar{E}_b). The device can be used as a 1-of-8 decoder/demultiplexer by tying E_a to \bar{E}_b and relabeling the common connection address as (A_2); forming the common enable by connecting the remaining \bar{E}_b and \bar{E}_a .

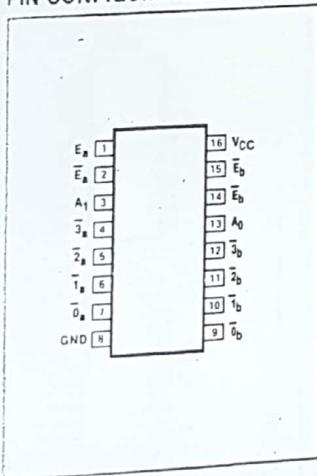
LOGIC DIAGRAM



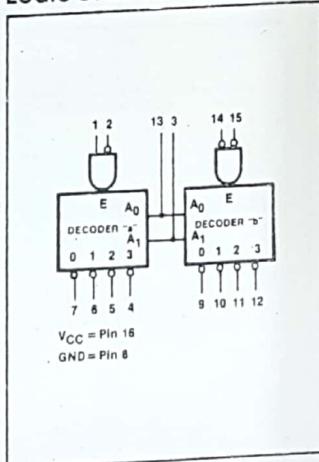
FUNCTION TABLE

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A_0	A_1	E_a	\bar{E}_a	0	1	2	3	\bar{E}_b	E_b	0	1	2	3
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	L	H
H	L	H	L	H	L	H	H	L	L	L	H	H	L
L	H	H	L	H	H	H	L	L	L	L	H	H	L
H	H	H	L	H	H	H	L	L	L	L	H	H	L

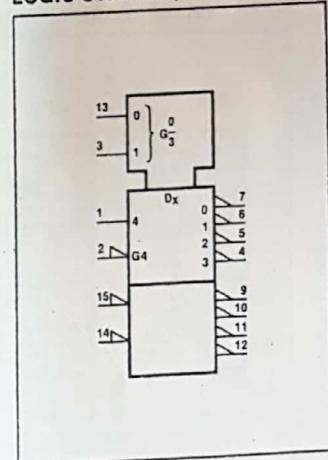
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



DATA SELECTORS/MULTIPLEXERS 54/74157, 54/74158, LS157, LS158, S157, S158

'157 Quad 2-Input Data Selector/Multiplexer (Non-Inverted)
 '158 Quad 2-Input Data Selector/Multiplexer (Inverted)

DESCRIPTION

The '157 is a quad 2-input multiplexer which selects four bits of data from two sources under the control of a common Select input (S). The Enable input (\bar{E}) is active LOW. When \bar{E} is HIGH, all of the outputs (Y) are forced LOW regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of the '157. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator. The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. Logic equations for the outputs are shown below:

$$\begin{aligned} Y_a &= \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S}) \\ Y_b &= \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S}) \\ Y_c &= \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S}) \\ Y_d &= \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S}) \end{aligned}$$

The '158 is similar but has inverting outputs:

$$\begin{aligned} \bar{Y}_a &= \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S}) \\ \bar{Y}_b &= \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S}) \\ \bar{Y}_c &= \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S}) \\ \bar{Y}_d &= \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S}) \end{aligned}$$

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74157	13ns	30mA
74LS157	13ns	9.7mA
74S157	7.4ns	50mA
74158	13ns	30mA
74LS158	13ns	4.8mA
74S158	6ns	40mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74157N • N74158N N74S157N • N74LS157N N74S158N • N74LS158N	
Plastic SO	N74LS157D N74LS158D	
Ceramic DIP		S54157F S54S157F • S54LS157F S54S158F • S54LS158F
Flatpack		S54157W S54S157W • S54LS157W S54S158W • S54LS158W
LLCC		

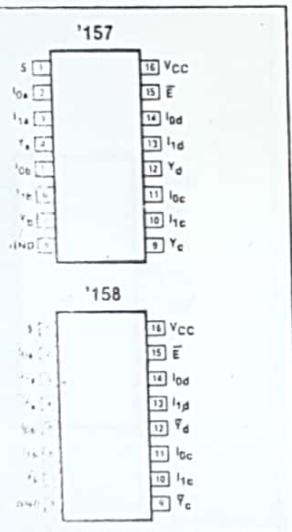
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
S, \bar{E}	Inputs	1 <ul style="list-style-type: none">	2 <ul style="list-style-type: none">	2 <ul style="list-style-type: none">
Data	Inputs	1 <ul style="list-style-type: none">	1 <ul style="list-style-type: none">	1 <ul style="list-style-type: none">
All	Outputs	10 <ul style="list-style-type: none">	10 <ul style="list-style-type: none">	10 <ul style="list-style-type: none">

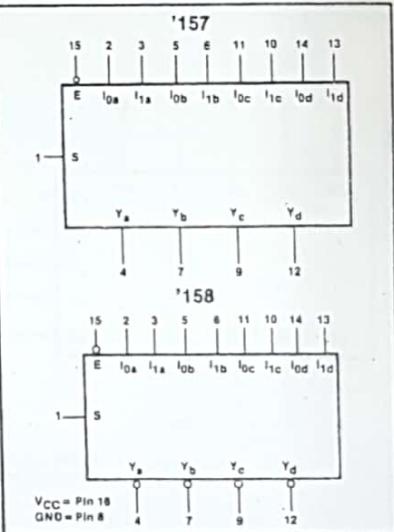
NOTE

Where a 54/74 unit load (ul) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , a 54/74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and a 54/74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

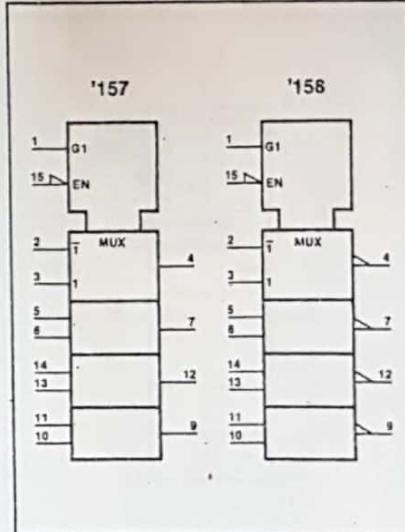
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



REGISTER FILES**54/74170, LS170****4 x 4 Register File (Open Collector)**

- Simultaneous and independent Read and Write operations
- Expandable to 1024 words by n-bits
- Open Collector outputs for wired-AND expansion
- See '670 for 3-State output version

DESCRIPTION

The '170 is a 16-bit register file organized as 4 words of 4 bits each, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four Data Inputs. The Write Address inputs (W_A and W_B) determine the location of the stored word. When the Write Enable (WE) input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the \overline{WE} is LOW. Data supplied at the inputs will be read out in true (non-inverting) form. Data and Write Address Inputs are inhibited when WE is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs (R_A and R_B). The addressed word appears at the four outputs when the Read Enable (RE) is

TYPE	TYPICAL PROPAGATION DELAY (RE to Q)	TYPICAL SUPPLY CURRENT (Total)
74170	10ns (t_{PLH}) 20ns (t_{PHL})	127mA
74LS170	20ns (t_{PLH}) 20ns (t_{PHL})	25mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\% ; T_A = 0^\circ C \text{ to } +70^\circ C$	$V_{CC} = 5V \pm 10\% ; T_A = -55^\circ C \text{ to } +125^\circ C$
Plastic DIP	N74170N • N74LS170N	

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

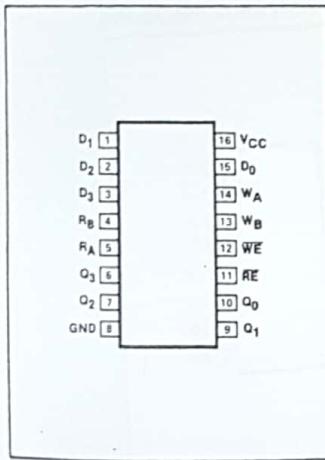
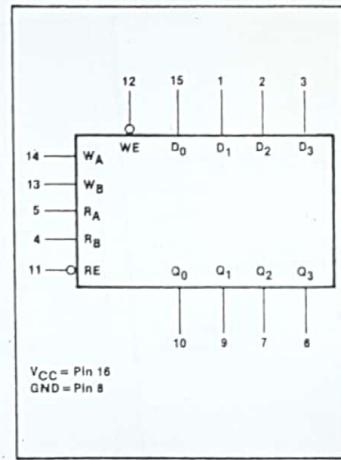
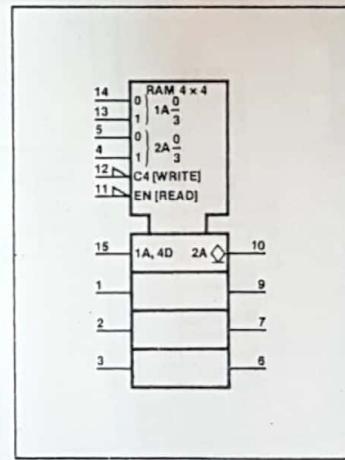
PINS	DESCRIPTION	54/74	54/74LS
D, W_A , W_B , R_A , R_B	Inputs	1 <ul style="list-style-type: none">l	1 <ul style="list-style-type: none">lS
\overline{WE} , RE	Inputs	1 <ul style="list-style-type: none">l	2 <ul style="list-style-type: none">lS
All	Outputs	10 <ul style="list-style-type: none">l	10 <ul style="list-style-type: none">lS

NOTE

Where a 54/74 unit load (l) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$ and a 54/74LS unit load (lS) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

LOW. Data outputs are inhibited and remain HIGH when the Read Enable input is HIGH. This permits simultaneous reading and writing, eliminates recovery times, and is limited in speed only by the read time and the write time.

Up to 256 devices can be stacked to increase the word size to 1024 locations by tying the Open Collector outputs together. Parallel expansion to generate n-bit words is accomplished by driving the Enable and Address inputs of each device in parallel.

PIN CONFIGURATION**LOGIC SYMBOL****LOGIC SYMBOL (IEEE/IEC)**

COUNTERS

- Synchronous, reversible counting
- BCD/decade — '190
- 4-bit binary — '191
- Synchronous, reversible counting
- Asynchronous parallel load capability
- Count enable control for synchronous expansion
- Single Up/Down control input

DESCRIPTION

The '190 is an asynchronously presettable up/down BCD decade counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation. The '191 is similar, but is a 4-bit binary counter.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel Data Inputs (D_0 - D_3) is loaded into the counter and appears on the outputs when the Parallel Load (PL) input is LOW. As indicated in the Mode Select Table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the Count Enable (\overline{CE}) input. When \overline{CE} is LOW, internal state changes are initiated

'190 Presettable BCD/Decade Up/Down Counter
'191 Presettable 4-Bit Binary Up/Down Counter

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74190	25MHz	65mA
74191	25MHz	65mA
74LS191	25MHz	20mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%; T_A = 0^\circ C \text{ to } +70^\circ C$	$V_{CC} = 5V \pm 10\%; T_A = -55^\circ C \text{ to } +125^\circ C$
Plastic DIP	N74190N N74191N • N74LS191N	
Plastic SO	N74LS191D	
Ceramic DIP		S54190F S54191F • S54LS191F
Flatpack		S54190W S54191W • S54LS191W

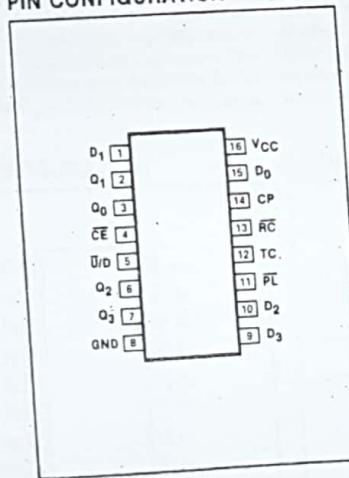
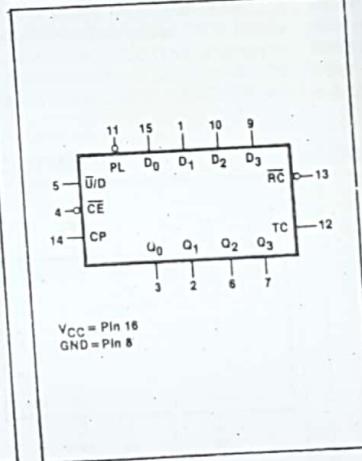
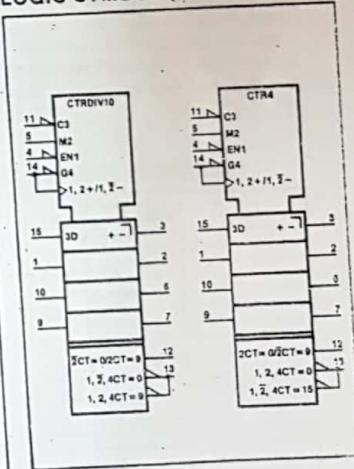
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
\overline{CE}	Input	3 <ul style="list-style-type: none">l	3 <ul style="list-style-type: none">l
Other	Inputs	1 <ul style="list-style-type: none">l	1 <ul style="list-style-type: none">l
All	Outputs	10 <ul style="list-style-type: none">l	10 <ul style="list-style-type: none">l

NOTE
Where a 54/74 unit load is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 54/74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

synchronously by the LOW-to-HIGH transition of the Clock Input. The Up/Down ($\overline{U/D}$) input signal determines the direction of counting as indicated in the Mode Select Table. The \overline{CE} input may go LOW

when the clock is in either state, however, the LOW-to-HIGH \overline{CE} transition must occur only when the clock is HIGH. Also, the $\overline{U/D}$ input should be changed only when either \overline{CE} or CP is HIGH.

PIN CONFIGURATION**LOGIC SYMBOL****LOGIC SYMBOL (IEEE/IEC)**

SHIFT REGISTERS

54/74194, LS194A, S194

P-32
LC
SI
M

4-Bit Bidirectional Universal Shift Register

- Buffered clock and control inputs
- Shift left and shift right capability
- Synchronous parallel and serial data transfers
- Easily expanded for both serial and parallel operation
- Asynchronous Master Reset
- Hold (do nothing) mode

DESCRIPTION

The functional characteristics of the '194 4-Bit Bidirectional Shift Register are indicated in the Logic Diagram and Function Table. The register is fully synchronous, with all operations taking place in less than 20ns (typical) for the 54/74 and 54LS/74LS, and 12ns (typical) for 54S/74S, making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

The '194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select Inputs, S_0 and S_1 . As shown in the Mode Select Table, data can be entered and shifted from left to right (shift right, Q_0-Q_1 , etc.) or, right to left (shift left, Q_3-Q_2 , etc.) or, parallel data can be entered, loading all 4 bits of the register simultaneously. When both S_0 and S_1 are LOW, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type Serial Data Inputs (D_{SR} , D_{SL}) to allow multistage

TYPE	TYPICAL I_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74194	36MHz	39mA
74LS194A	36MHz	15mA
74S194	105MHz	85mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74194N • N74LS194AN N74S194N	
Plastic SO	N74LS194AD • N745194D	
Ceramic DIP		S54194F • S54LS194AF S54S194F
Flatpack		S54194W • S54LS194AW S54S194W
LLCC		S54194G

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
All	Inputs	1uL	1Sul	1LSul
Q_0-Q_3	Outputs	10uL	10Sul	10LSul

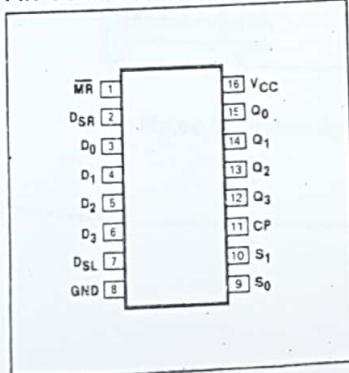
NOTE
Where a 54/74 unit load (uL) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, a 54/74S unit load (Sul) is $50\mu A I_{IH}$ and $-2.0mA I_{IL}$, and 54/74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

shift right or shift left data transfers without interfering with parallel load operation. gated with the clock and should be changed from HIGH-to-LOW only while the Clock Input is HIGH.

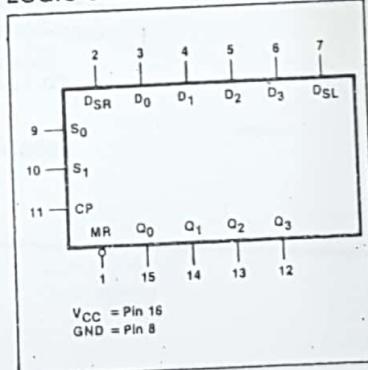
Mode Select and Data inputs on the 54S/74S194 and 54LS/74LS194A are edge-triggered, responding only to the LOW-to-HIGH transition of the Clock (CP). Therefore, the only timing restriction is that the Mode Control and selected Data inputs must be stable one setup time prior to the positive transition of the clock pulse. The Mode Select inputs of the 54/74194 are

The four parallel data inputs (D_0-D_3) are D-type inputs. Data appearing on D_0-D_3 inputs when S_0 and S_1 are HIGH is transferred to the Q_0-Q_3 outputs respectively, following the next LOW-to-HIGH transition of the clock. When LOW, the asynchronous Master Reset (MR) overrides all other input conditions and forces the Q outputs LOW.

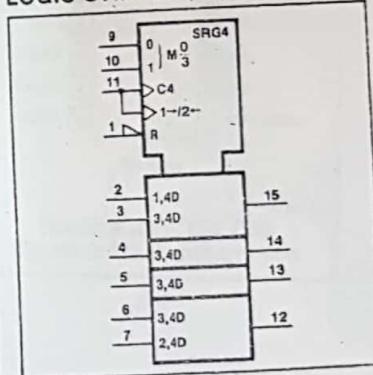
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ADC0804

μ P-Compatible Converters

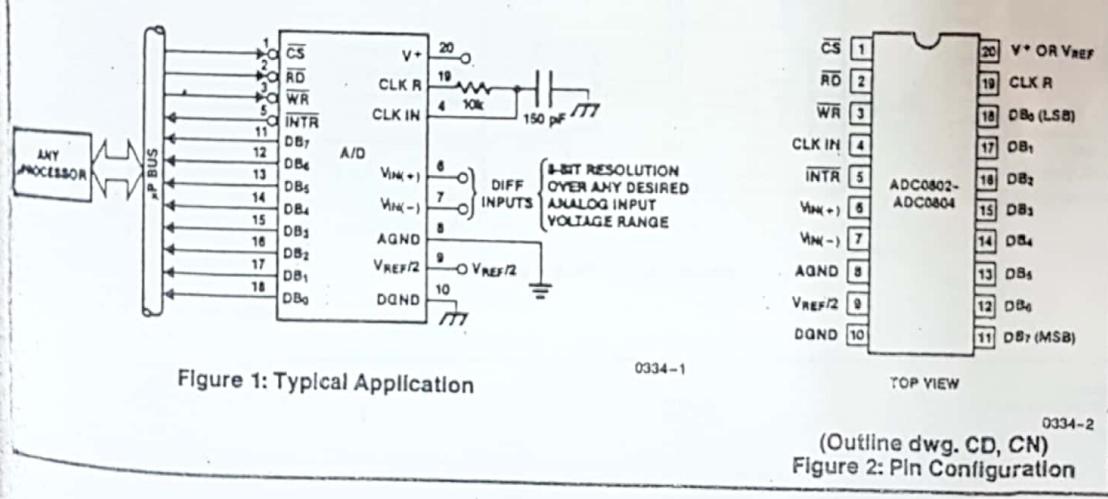
P-33
INTERSIL

0334-1 ADC0804

FEATURES

- 80C48 and 80C80/85 Bus Compatible — No Interfacing Logic Required
- Conversion Time < 100 μ s
- Easy Interface to Most Microprocessors
- Will Operate in a "Stand Alone" Mode
- Differential Analog Voltage Inputs
- Works With Bandgap Voltage References
- TTL Compatible Inputs and Outputs
- On-Chip Clock Generator
- 0V to 5V Analog Voltage Input Range (Single +5V Supply)
- No Zero-Adjust Required

Part Number	Error	Temperature Range	Package
ADC0802LCN	$\pm \frac{1}{2}$ bit no adjust	0°C to +70°C	20 pin Plastic DIP
ADC0802LCD	$\pm \frac{3}{4}$ bit no adjust	-40°C to +85°C	20 pin CERDIP
ADC0802LD	± 1 bit no adjust	-55°C to +125°C	20 pin CERDIP
ADC0803LCN	$\pm \frac{1}{2}$ bit adjusted full-scale	0°C to +70°C	20 pin Plastic DIP
ADC0803LCD	$\pm \frac{3}{4}$ bit adjusted full-scale	-40°C to +85°C	20 pin CERDIP
ADC0803LD	± 1 bit adjusted full-scale	-55°C to +125°C	20 pin CERDIP
ADC0804LCN	± 1 bit no adjust	0°C to +70°C	20 pin Plastic DIP
ADC0804LCD	± 1 bit no adjust	-40°C to +85°C	20 pin CERDIP





8255A/8255A-5 PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
 - 24 Programmable I/O Pins
 - Completely TTL Compatible
 - Fully Compatible with Intel Microprocessor Families
 - Improved Timing Characteristics
 - Direct Bit Set/Reset Capability Easing Control Application Interface
 - Reduces System Package Count
 - Improved DC Driving Capability
 - Available in EXPRESS
 - Standard Temperature Range
 - Extended Temperature Range
 - 40 Pin DIP Package or 44 Lead PLCC
- (See Intel Packaging Draw Number 231308)

The Intel 8255A is a general purpose programmable I/O device designed for use with Intel microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

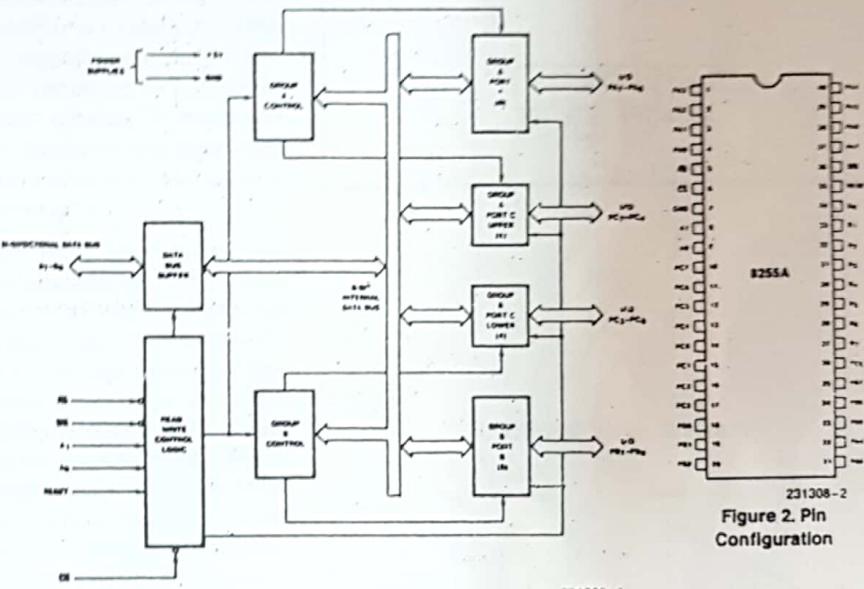


Figure 1. 8255A Block Diagram

231308-1

September 1987
Order Number: 231309-002

- Timing from Microseconds to Hours
- Astable or Monostable Operation
- Adjustable Duty Cycle
- TTL-Compatible Output Can Sink or Source up to 200 mA
- Designed to be Interchangeable with Signetics SE555/NE555

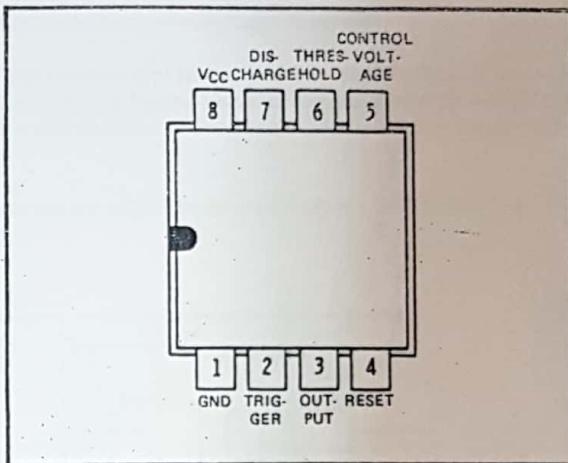
description

The SE555 and NE555 are monolithic timing circuits capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle may be independently controlled with two external resistors and a single external capacitor.

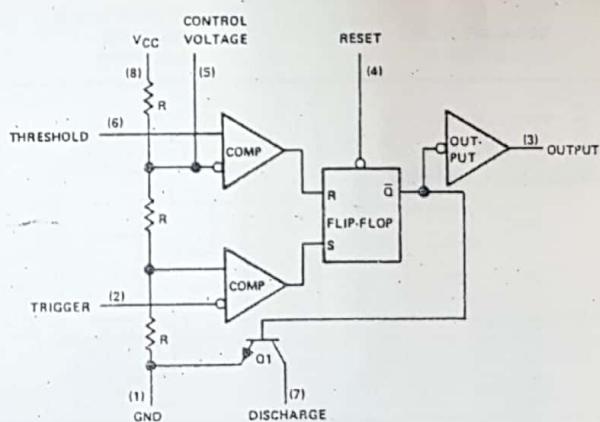
The threshold and trigger levels are normally two-thirds and one-third, respectively, of V_{CC}. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. When the threshold input rises above the threshold level, the flip-flop is reset and the output goes low. The reset input can override all other inputs and can be used to initiate a new timing cycle. When the reset input goes low, the flip-flop is reset and the output goes low. When the output is low, a low-impedance path is provided between the discharge terminal and ground.

The output circuit is capable of sinking or sourcing current up to 200 milliamperes. Operation is specified for supplies of 5 to 15 volts. With a 5-volt supply, output levels are compatible with TTL inputs.

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



functional block diagram



LINEAR
INTEGRATED
CIRCUITS

TYPES uA741M, uA741C
GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

BULLETIN NO. DL-S 11363, NOVEMBER 1970—REVISED OCTOBER 1970

- Short-Circuit Protection
- Offset-Voltage Null Capability
- Large Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-up

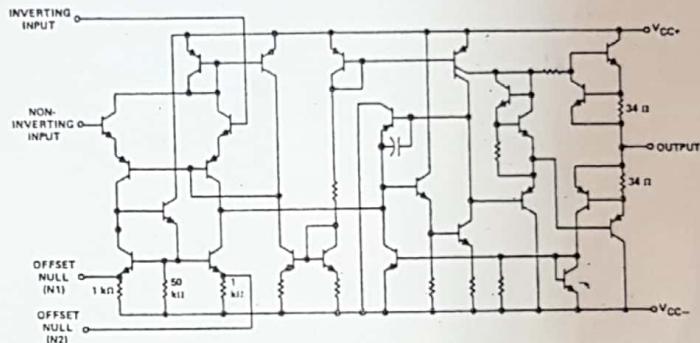
description

The uA741 is a general-purpose operational amplifier featuring offset-voltage null capability.

The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low-value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 2.

The uA741M is characterized for operation over the full military temperature range of -55°C to 125°C ; the uA741C is characterized for operation from 0°C to 70°C .

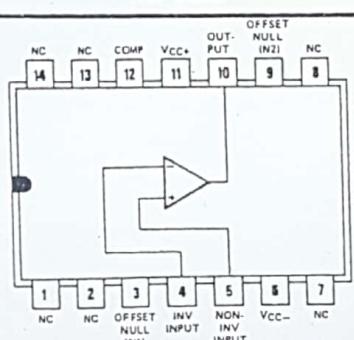
schematic



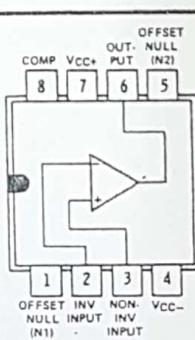
Resistor values shown are nominal

terminal assignments

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE
(TOP VIEW)



JG OR P DUAL-IN-LINE
PACKAGE
(TOP VIEW)



U
FLAT PACKAGE
(TOP VIEW)

