# Cadence 전자회로설계해석 PCB Artwork 실무 프로젝트

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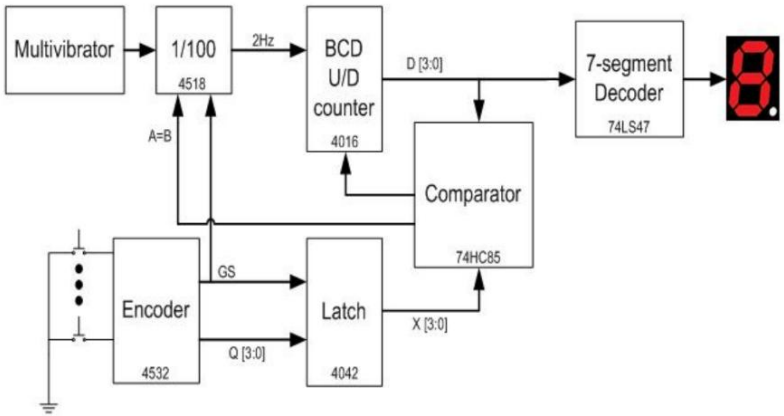
한정호

# INDEX

# Elevator Circuit BLOCK DIAGRAM




*Encoder & Switch
- Switch입력 받아 4bit Data “Q[3:0]” 생성
- Latch 동작 신호 “GS” 출력

*Latch - Q[3:0] -> X[3:0]으로 저장 후 유지

*Multivibrator – Pulse Signal 생성

*1/100분주기 – Pulse Signal Freq -> 2Hz 설정.

*Comparator – Latch의 X[3:0]과 Counter의 D[3:0]비교

*BCD U/D Counter
- Comparator의 지시에 따라 동작함.
- D[3:0] = 현재 엘리베이터의 층

*7-Segment Decoder – D[3:0]을 시각적으로 표현함.

# 동작 요구 사항[1]

가. VR1을 조정하여 TP1에서 100[Hz]의 주파수 나오게 하시오.

나. TP1과 TP2를 측정하여 파형을 답안지에 그리시오.

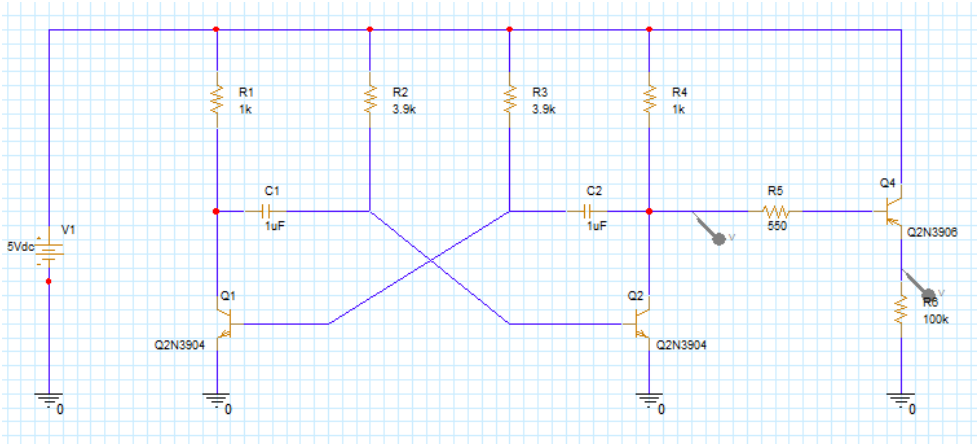
다. Reset SW를 누르면 FND에 “1”이 표시되게 하시오.

라. 1층~9층을 운행하는 엘리베이터로 현재 층은 LED와 FND에 표시되게 하시오.

마. 운행하고자 하는 층을 SW1~SW9로 선택하면 현재 층에서 0.5[s]의 속도로 선택한 층까지 이동하게 하시오.

사. FND에 표시된 층보다 선택한 층이 높을 경우 Up Counter을 하며, 선택한 층이 낮을 경우는 Down Counter를 하게 하시오.

# Multivibrator Circuit



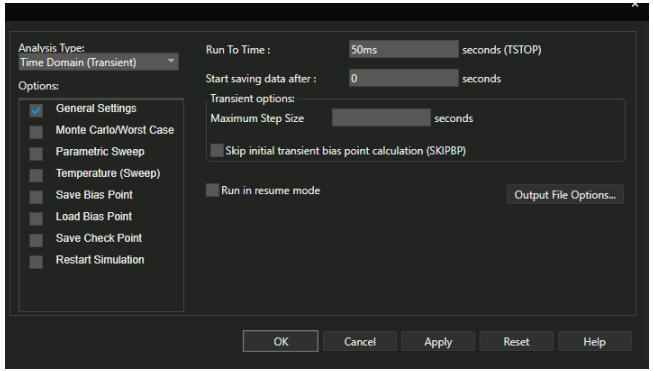

* Q1, Q2, R1~R4, C1, C2 : 주기적인 사각파 신호 생성

*Q4, R5, R6 : 입력 신호 받아 반전 후 출력.

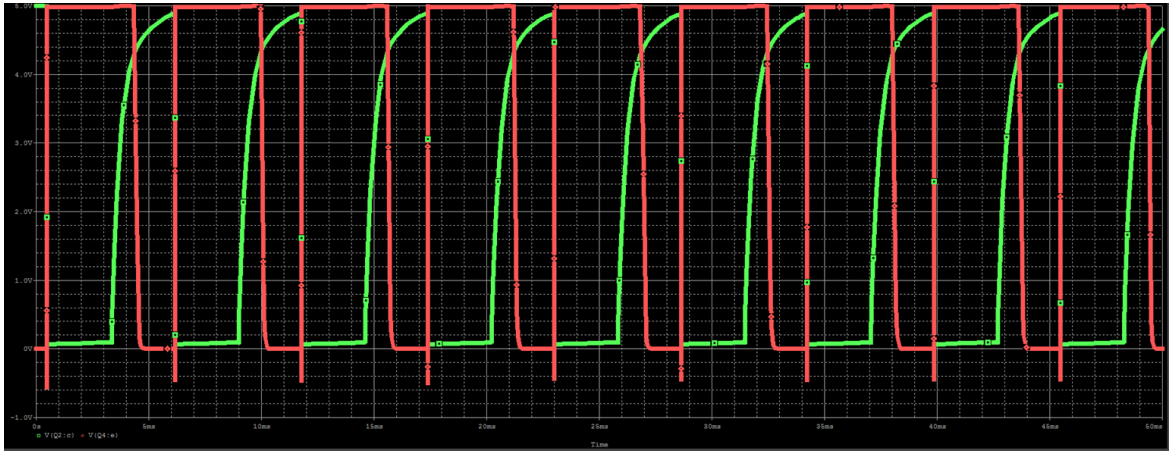
*예상 동작

1. Q1 On -> Vc1 = 0V
2. C1 전압강하 전달
3. Vb2 = 0v -> Q2 off
4. C1 충전
5. Vb2 > Vth -> Q2 On
6. Q2 On -> Vc2 = 2V
7. C2 전압강하 전달
8. Vb1 = 0v 0-> Q1 off
9. 1~8 반복.

# Multivibrator Simulation



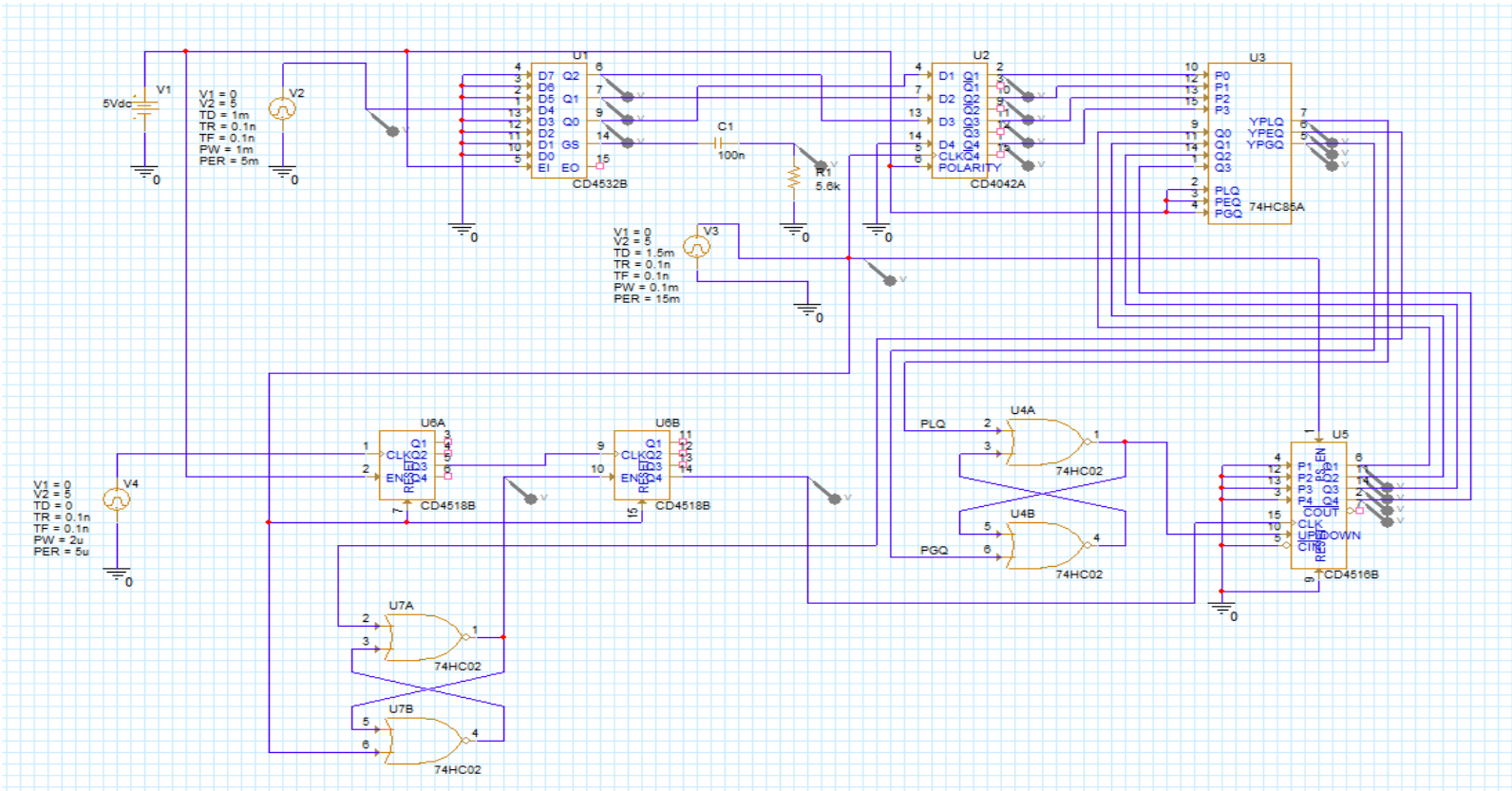

*Transient Analysis 진행
- Run To Time : 50ms



* V(Q2 :c) : 0V / 5V의 On/ Off 반복

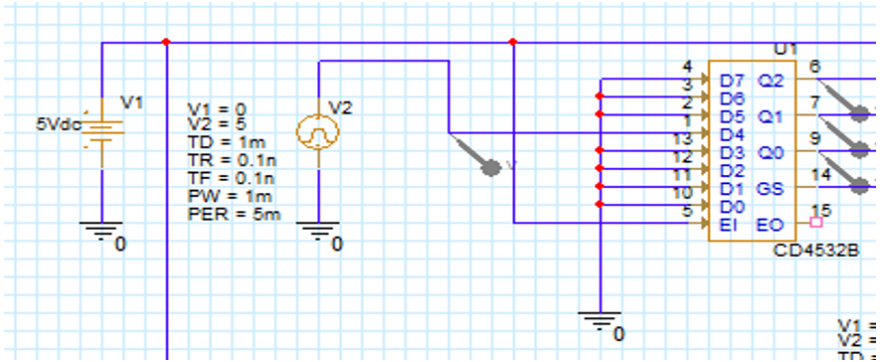
* V(Q4 :e) : 반전 출력, C2로 인해 충, 방전 파형 나타남

# Elevator Control System Circuit

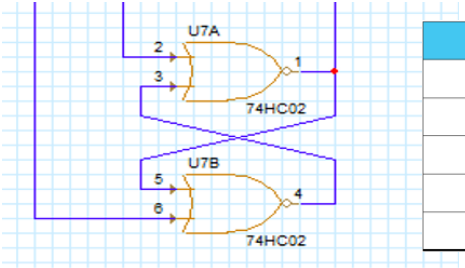


# Elevator Control System Circuit

## *Encoder



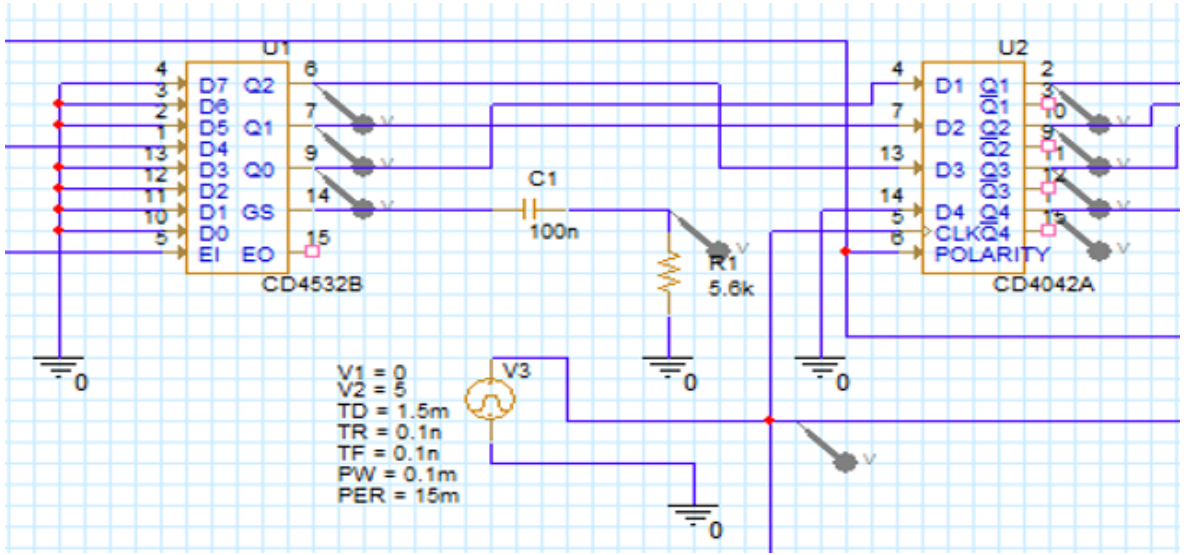

## *SR Latch




| 입력 | | 출력 |
|---|---|---|
| $S$ | $R$ | $Q(t+1)$ |
| 0 | 0 | $Q(t)$ 불변 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 부정 |

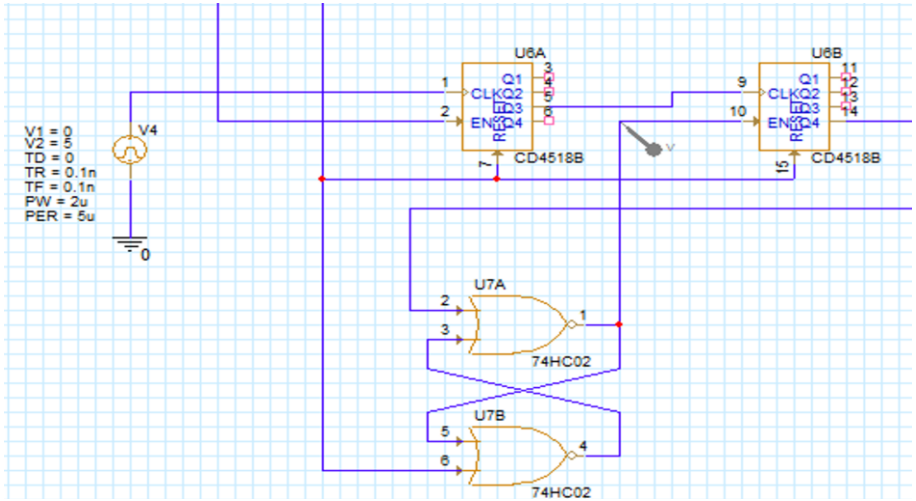
# Elevator Control System Circuit

*Encoder & Latch



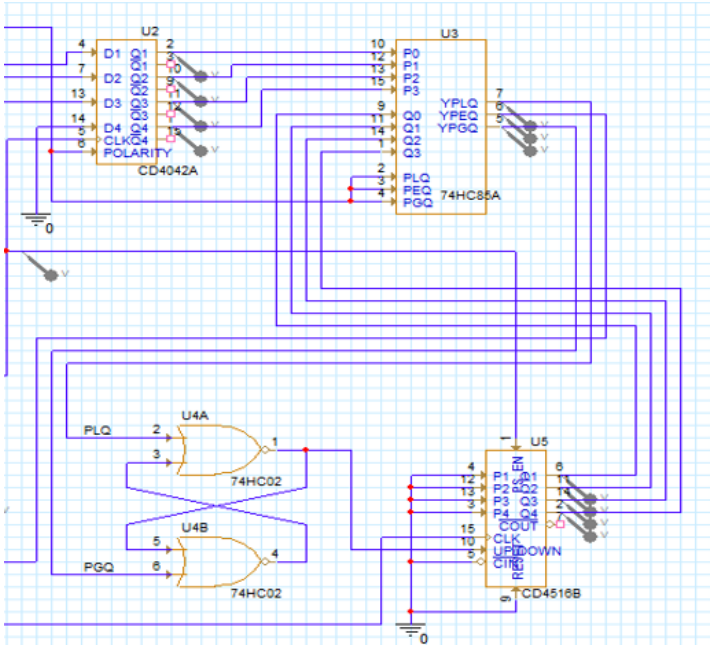
# Elevator Control System Circuit

*Multivibrator & 1/100분주기 – Pulse Signal 생성, Freq 조정

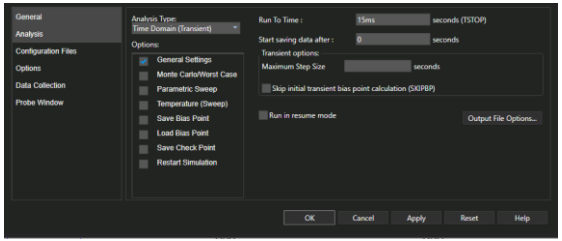


# Elevator Control System Circuit

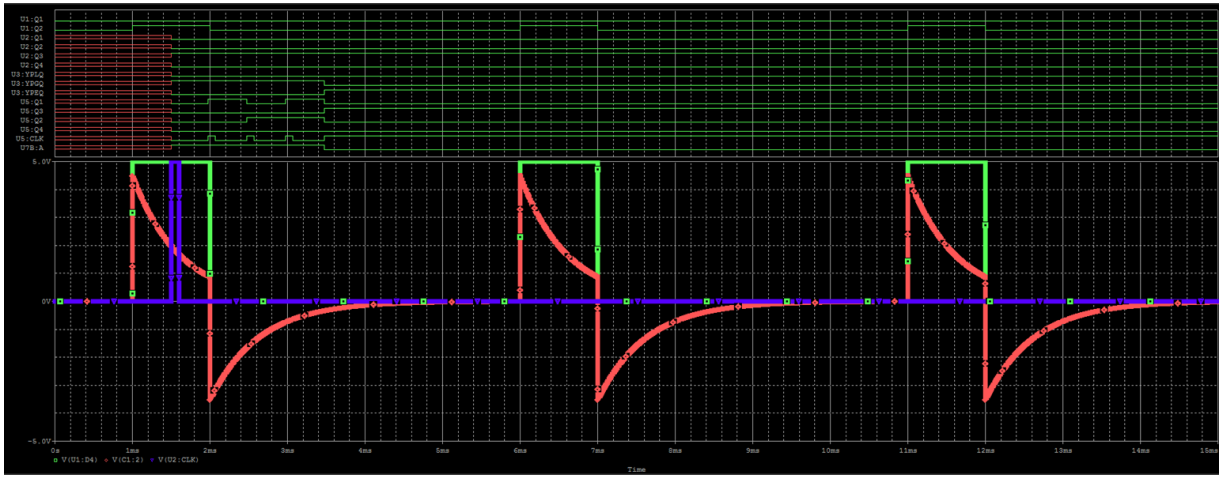
*Comparator & BCD U/D Counter



# Elevator Control System Circuit Simulation

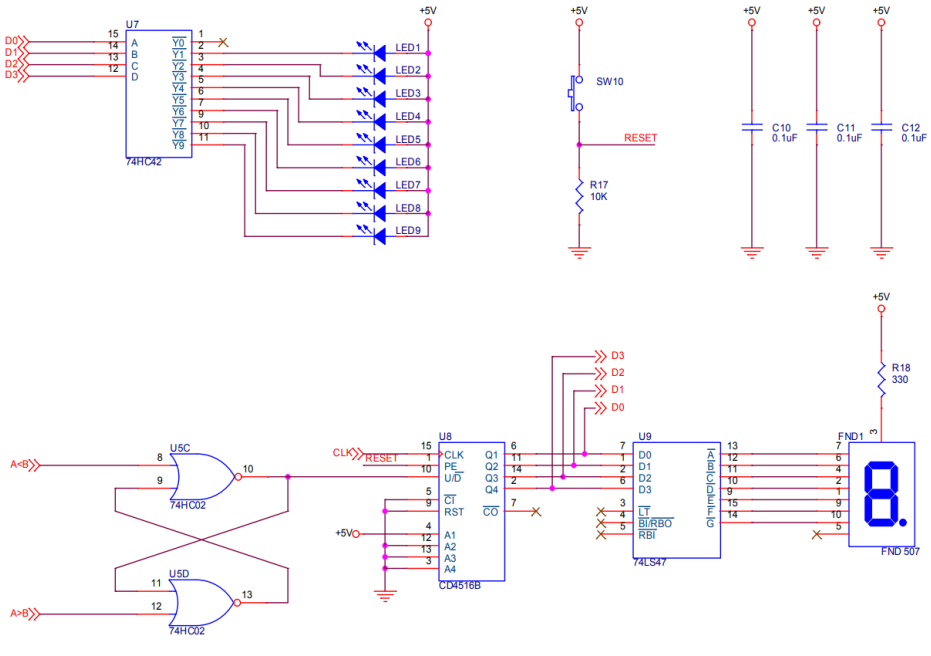



*Transient Analysis 진행
- Run To Time : 15ms




*Encoder, Comparator, U/P Counter의 동작을 잘 나타내고 있음

# Output and Display circuit



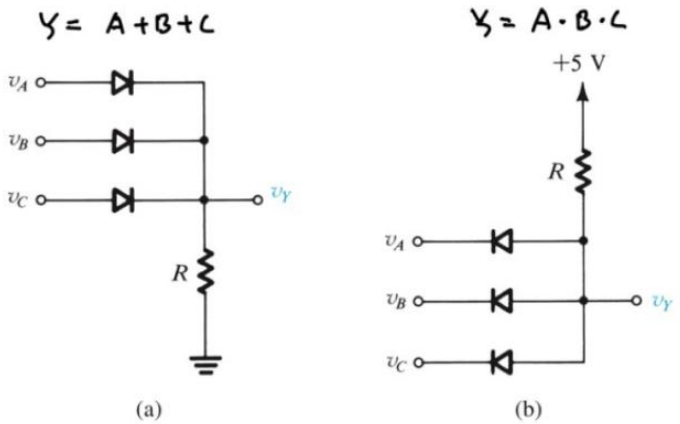

*LED 출력
- LED
- BCD to Decimal Decoder(74HC42)

*카운터 및 제어
- U/D Counter(CD4516B)
- NOR gate(74HC02)

*7 Segment 출력
- BCD to 7 Segment Decoder(74LS47)
- 7 Segment(FND1)

*Reset 회로
- SW10, R17

# Diode Logic Circuits




5 Diode logic gates: **(a)** OR gate; **(b)** AND gate (in a positive-logic system).

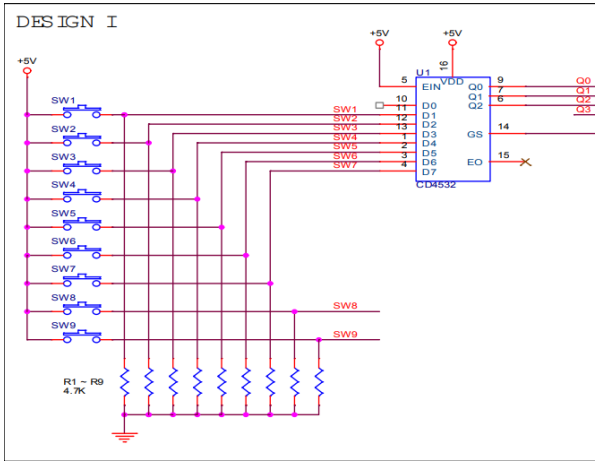
*Diode On/ Off에 따른 출력전압 Vy 관찰

*Diode를 활용하여 Logic Gate 구현 가능

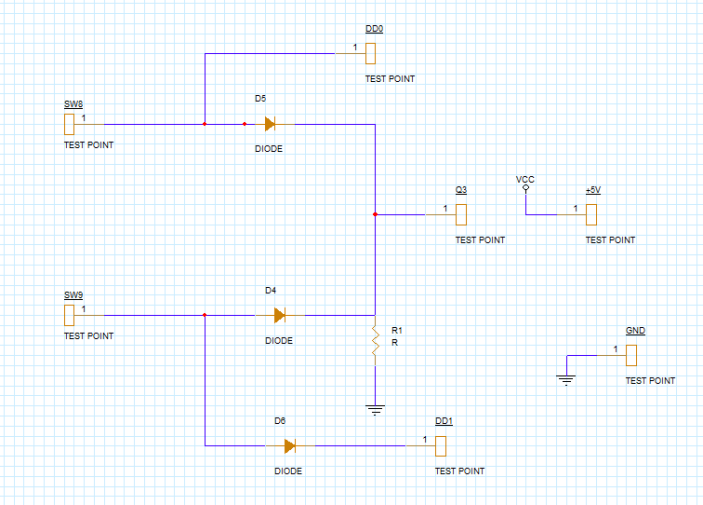
## 동작 요구 사항[2]

| 출력 / 입력 | Q0 | Q1 | Q2 | Q3 |
|---|---|---|---|---|
| SW1 ON | 1 | 0 | 0 | 0 |
| SW2 ON | 0 | 1 | 0 | 0 |
| SW3 ON | 1 | 1 | 0 | 0 |
| SW4 ON | 0 | 0 | 1 | 0 |
| SW5 ON | 1 | 0 | 1 | 0 |
| SW6 ON | 0 | 1 | 1 | 0 |
| SW7 ON | 1 | 1 | 1 | 0 |
| SW8 ON | 0 | 0 | 0 | 1 |
| SW9 ON | 1 | 0 | 0 | 1 |

# DIODE, TEST POINT Circuit

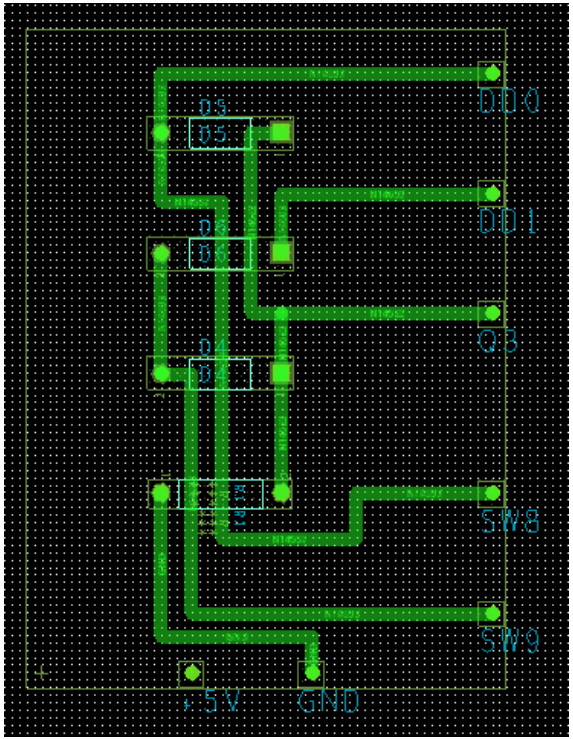



*주어진 회로

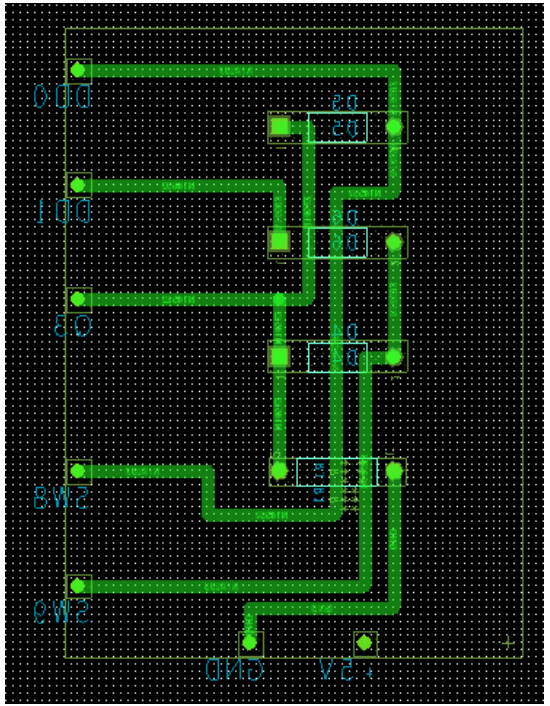



*실제 구현 회로

# PCB Layout & Final Product

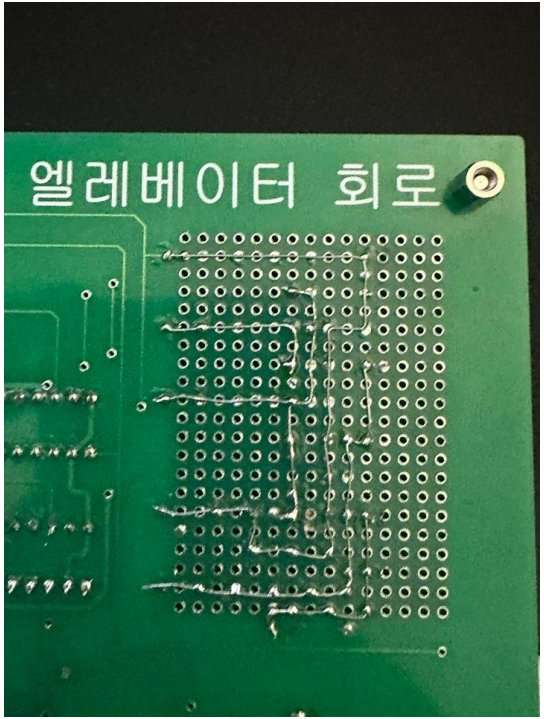



*PCB Editor



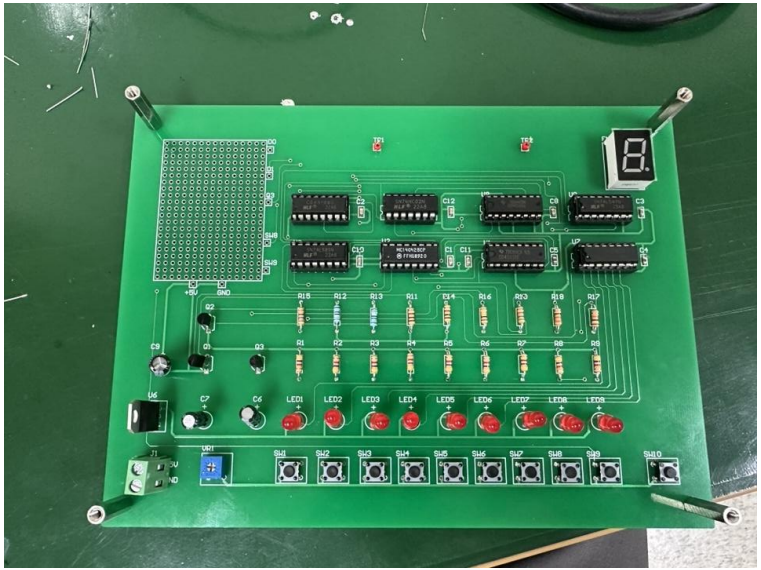

*실제 배선 위해 좌우 대칭 이미지 참고

# PCB Layout & Final Product

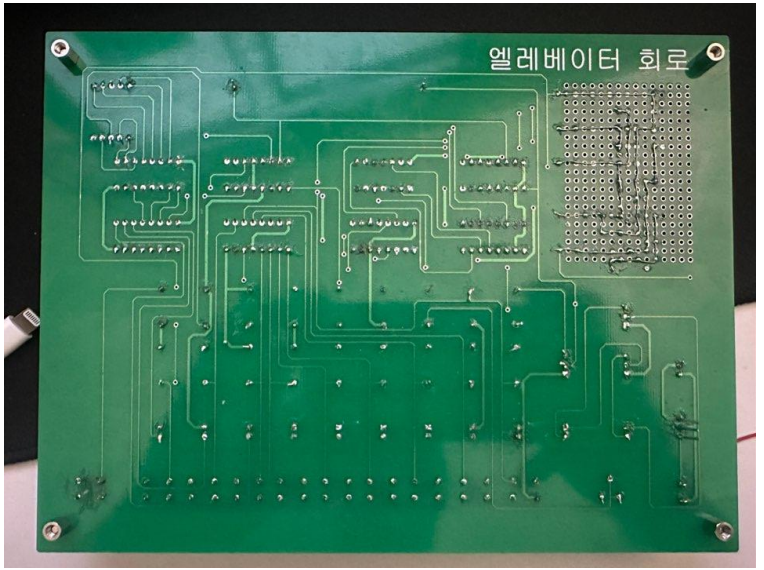



*Real Product

# Final Product

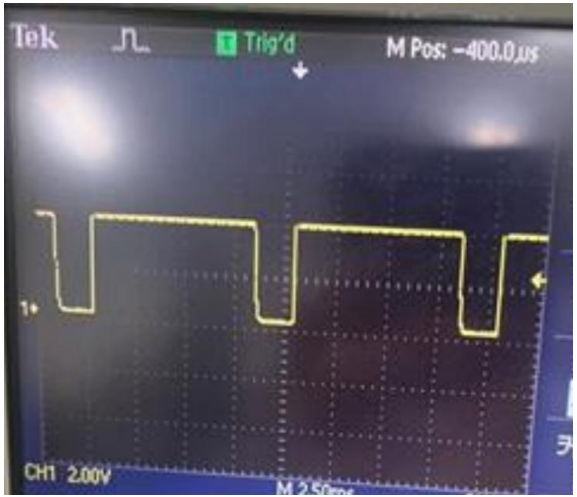


*전면부




*후면부

# TEST




*TP1


*TP2