自制操作系统 -准备篇

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1 课题硬件环境描述

1 硬件: TEC-8 实验电路

   1 74181ALU 等

   2 可编程逻辑芯片 EPM7128

2 软件: Quartus II 9.0

2 题目分析

2.1 实验目标

1 完成硬连线控制器基础设计

2 在原指令的基础上扩指至少三条

3 修改 PC 指针功能

4 完成流水硬连线控制器基础设计

5 在原指令的基础上扩指至少三条

6 修改 PC 指针功能

2.2 设计思路

1 画出硬连线控制器运行流程图

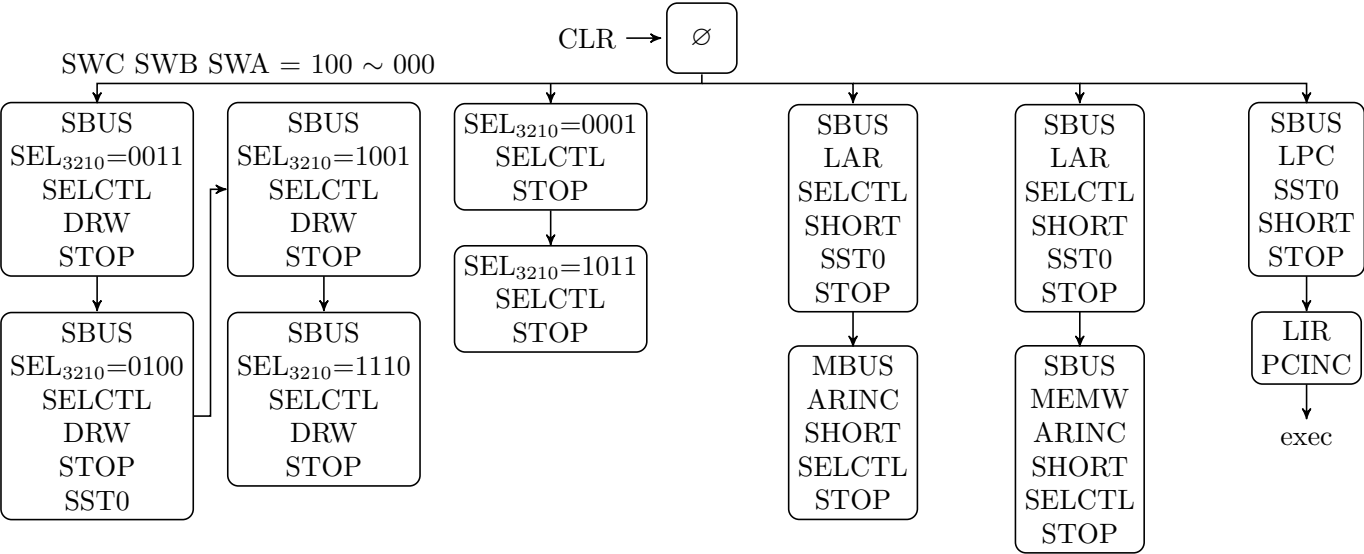2 将硬连线控制器运行流程图翻译成硬连线信号

3 将硬连线信号翻译成 VHDL 多分支程序

3   团队分工

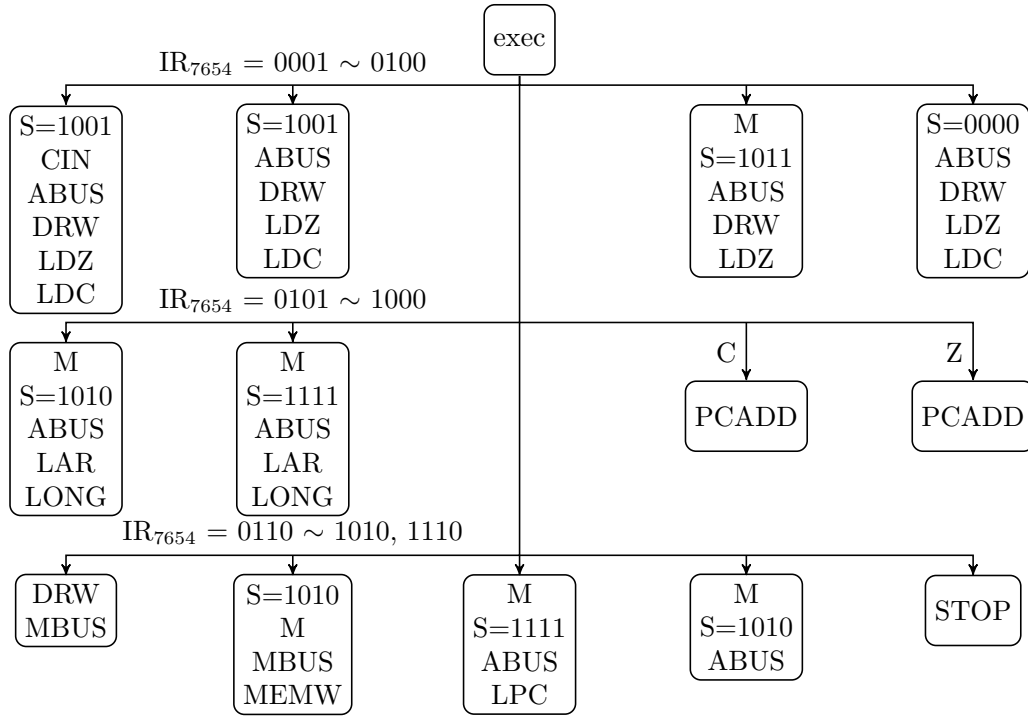向阳曦负责程序指令翻译, 张逸群负责控制台程序。

合并一起以后，两人一起完成控制器程序的测试。

4   设计详解

4.1   硬连线控制器

4.1.1   设计硬连线控制器运行流程图

CLR → ∅

SWC SWB SWA $= 100 \sim 000$

SBUS
$SEL_{3210}=0011$
SELCTL
DRW
STOP

SBUS
$SEL_{3210}=0100$
SELCTL
DRW
STOP
SST0

SBUS
$SEL_{3210}=1001$
SELCTL
DRW
STOP

SBUS
$SEL_{3210}=1110$
SELCTL
DRW
STOP

$SEL_{3210}=0001$
SELCTL
STOP

$SEL_{3210}=1011$
SELCTL
STOP

SBUS
LAR
SELCTL
SHORT
SST0
STOP

MBUS
ARINC
SHORT
SELCTL
STOP

SBUS
LAR
SELCTL
SHORT
SST0
STOP

SBUS
MEMW
ARINC
SHORT
SELCTL
STOP

SBUS
LPC
SST0
SHORT
STOP

LIR
PCINC

exec

其中 CLR 表示转移到 ∅. 任意没有出边的状态也都转移到 ∅, 任意时刻传入 CLR 信号也都转移到 ∅.

exec

$IR_{7654} = 0001 \sim 0100$

| S=1001 CIN ABUS DRW LDZ LDC | S=1001 ABUS DRW LDZ LDC | M S=1011 ABUS DRW LDZ | S=0000 ABUS DRW LDZ LDC |

$IR_{7654} = 0101 \sim 1000$

| M S=1010 ABUS LAR LONG | M S=1111 ABUS LAR LONG |

C

PCADD

Z

PCADD

$IR_{7654} = 0110 \sim 1010, 1110$

| DRW MBUS | S=1010 M MBUS MEMW | M S=1111 ABUS LPC | M S=1010 ABUS | STOP |

上图显示了从左到右, 从上到下依次为 ADD, SUB, AND, INC, LD, ST, JC, JZ, JMP, OUT, STP 的所有指令.

需要注意的是, 如果某条指令包含 SHORT, 那么它是一个单拍指令, 如果某条指令包含 LONG，那么它的下一拍还属于该指令, 计三拍.

4.1.2 翻译成硬连线信号

SBUS $\leftarrow$

$(\text{W1} + \text{W2}) \cdot \text{SWC} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} +$

$\text{W1} \cdot \overline{\text{SWC}} \cdot \text{SWB} \cdot \overline{\text{SWA}} \cdot \overline{\text{ST0}} +$

$\text{W1} \cdot \overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \text{SWA} +$

$\text{W1} \cdot \overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \overline{\text{ST0}}$

MBUS $\leftarrow$

$\text{W1} \cdot \overline{\text{SWC}} \cdot \text{SWB} \cdot \overline{\text{SWA}} \cdot \text{ST0} +$

$$W3 \cdot \overline{IR7} \cdot IR6 \cdot \overline{IR5} \cdot IR4 \cdot \overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA}$$

ABUS ←

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot \overline{IR6} \cdot \overline{IR5} \cdot IR4 \cdot W2+$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot \overline{IR6} \cdot IR5 \cdot \overline{IR4} \cdot W2+$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot \overline{IR6} \cdot IR5 \cdot IR4 \cdot W2+$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot IR6 \cdot \overline{IR5} \cdot \overline{IR4} \cdot W2+$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot IR6 \cdot \overline{IR5} \cdot IR4 \cdot W2+$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot IR6 \cdot IR5 \cdot \overline{IR4} \cdot (W2 + W3)+$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot IR7 \cdot \overline{IR6} \cdot \overline{IR5} \cdot IR4 \cdot W2+$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot IR7 \cdot \overline{IR6} \cdot IR5 \cdot \overline{IR4} \cdot W2$$

LAR ←

$$W1 \cdot \overline{SWC} \cdot SWB \cdot \overline{SWA} \cdot \overline{ST0}+$$

$$W1 \cdot \overline{SWC} \cdot \overline{SWB} \cdot SWA \cdot \overline{ST0}+$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} + \cdot \overline{IR7} \cdot IR6 \cdot \overline{IR5} \cdot IR4 \cdot W2+$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} + \cdot \overline{IR7} \cdot IR6 \cdot IR5 \cdot \overline{IR4} \cdot W2$$

SST0 ←

$$W1 \cdot \overline{SWC} \cdot SWB \cdot \overline{SWA} \cdot \overline{ST0}+$$

$$W2 \cdot SWC \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{ST0}+$$

$$W1 \cdot \overline{SWC} \cdot \overline{SWB} \cdot SWA \cdot \overline{ST0}+$$

$$W1 \cdot \overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{ST0}$$

SHORT ←

$$W1 \cdot \overline{SWC} \cdot SWB \cdot \overline{SWA}+$$

$$W1 \cdot \overline{SWC} \cdot \overline{SWB} \cdot SWA+$$

$$W1 \cdot \overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{ST0}$$

ARINC ←

$$W1 \cdot \overline{SWC} \cdot SWB \cdot \overline{SWA} \cdot ST0+$$

$$W1 \cdot \overline{SWC} \cdot \overline{SWB} \cdot SWA \cdot ST0$$

MEMW ←

$$W1 \cdot \overline{SWC} \cdot \overline{SWB} \cdot SWA \cdot ST0+$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot IR6 \cdot IR5 \cdot \overline{IR4} \cdot W3$$

LIR ←

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot ST0 \cdot W1$$

CIN ←

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot \overline{IR6} \cdot \overline{IR5} \cdot \overline{IR4} \cdot W2$$

M ←

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot \overline{IR6} \cdot IR5 \cdot IR4 \cdot W2+$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot IR6 \cdot \overline{IR5} \cdot IR4 \cdot W2+$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot IR6 \cdot IR5 \cdot \overline{IR4} \cdot (W2 + W3)+$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot IR7 \cdot \overline{IR6} \cdot \overline{IR5} \cdot IR4 \cdot W2+$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot IR7 \cdot \overline{IR6} \cdot IR5 \cdot \overline{IR4} \cdot W2$$

SEL0←

$$\mathrm{SWC} \cdot \overline{\mathrm{SWB}} \cdot \overline{\mathrm{SWA}} \cdot \mathrm{W1}$$

SEL1←

$$\mathrm{SWC} \cdot \overline{\mathrm{SWB}} \cdot \overline{\mathrm{SWA}} \cdot \mathrm{W2} \cdot \mathrm{ST0}$$

$$\mathrm{SWC} \cdot \overline{\mathrm{SWB}} \cdot \overline{\mathrm{SWA}} \cdot \mathrm{W1} \cdot \overline{\mathrm{ST0}}$$

SEL2←

$$\mathrm{SWC} \cdot \overline{\mathrm{SWB}} \cdot \overline{\mathrm{SWA}} \cdot \mathrm{W2}$$

SEL3←

$$\mathrm{SWC} \cdot \overline{\mathrm{SWB}} \cdot \overline{\mathrm{SWA}} \cdot \mathrm{W1} \cdot \mathrm{ST0}+$$

$$\mathrm{SWC} \cdot \overline{\mathrm{SWB}} \cdot \overline{\mathrm{SWA}} \cdot \mathrm{W2} \cdot \overline{\mathrm{ST0}}$$

STOP←

$$\mathrm{SWA} + \mathrm{SWB} + \mathrm{SWC}+$$

$$\overline{\mathrm{SWC}} \cdot \overline{\mathrm{SWB}} \cdot \overline{\mathrm{SWA}} \cdot \mathrm{IR7} \cdot \mathrm{IR6} \cdot \mathrm{IR5} \cdot \overline{\mathrm{IR4}} \cdot \mathrm{ST0} \cdot \mathrm{W2}$$

SELCTL←

$$\mathrm{SWA} + \mathrm{SWB} + \mathrm{SWC}$$

DRW←

$$\mathrm{SWC} \cdot \overline{\mathrm{SWB}} \cdot \overline{\mathrm{SWA}}+$$

$$\overline{\mathrm{SWC}} \cdot \overline{\mathrm{SWB}} \cdot \overline{\mathrm{SWA}} \cdot \mathrm{ST0} \cdot \overline{\mathrm{IR7}} \cdot \overline{\mathrm{IR6}} \cdot \overline{\mathrm{IR5}} \cdot \mathrm{IR4} \cdot \mathrm{W2}+$$

$$\overline{\mathrm{SWC}} \cdot \overline{\mathrm{SWB}} \cdot \overline{\mathrm{SWA}} \cdot \mathrm{ST0} \cdot \overline{\mathrm{IR7}} \cdot \overline{\mathrm{IR6}} \cdot \mathrm{IR5} \cdot \overline{\mathrm{IR4}} \cdot \mathrm{W2}+$$

$$\overline{\mathrm{SWC}} \cdot \overline{\mathrm{SWB}} \cdot \overline{\mathrm{SWA}} \cdot \mathrm{ST0} \cdot \overline{\mathrm{IR7}} \cdot \overline{\mathrm{IR6}} \cdot \mathrm{IR5} \cdot \mathrm{IR4} \cdot \mathrm{W2}+$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot ST0 \cdot \overline{IR7} \cdot IR6 \cdot \overline{IR5} \cdot \overline{IR4} \cdot W2+$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot ST0 \cdot \overline{IR7} \cdot IR6 \cdot \overline{IR5} \cdot IR4 \cdot W3$$

PCADD←

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot ST0 \cdot \overline{IR7} \cdot IR6 \cdot IR5 \cdot IR4 \cdot C \cdot W2+$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot ST0 \cdot IR7 \cdot \overline{IR6} \cdot \overline{IR5} \cdot \overline{IR4} \cdot Z \cdot W2$$

PCINC←

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot ST0 \cdot W1$$

LPC←

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{ST0} \cdot W2$$

LONG←

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot W2 \cdot \overline{IR7} \cdot IR6 \cdot \overline{IR5} \cdot IR4+$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot W2 \cdot \overline{IR7} \cdot IR6 \cdot IR5 \cdot \overline{IR4}$$

LDC←

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot ST0 \cdot \overline{IR7} \cdot \overline{IR6} \cdot \overline{IR5} \cdot IR4 \cdot W2+$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot ST0 \cdot \overline{IR7} \cdot \overline{IR6} \cdot IR5 \cdot \overline{IR4} \cdot W2+$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot ST0 \cdot \overline{IR7} \cdot \overline{IR6} \cdot IR5 \cdot IR4 \cdot W2+$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot ST0 \cdot \overline{IR7} \cdot IR6 \cdot \overline{IR5} \cdot \overline{IR4} \cdot W2$$

LDZ←

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot ST0 \cdot \overline{IR7} \cdot \overline{IR6} \cdot \overline{IR5} \cdot IR4 \cdot W2+$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot ST0 \cdot \overline{IR7} \cdot \overline{IR6} \cdot IR5 \cdot \overline{IR4} \cdot W2+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \text{ST0} \cdot \overline{\text{IR7}} \cdot \overline{\text{IR6}} \cdot \text{IR5} \cdot \text{IR4} \cdot \text{W2}+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \text{ST0} \cdot \overline{\text{IR7}} \cdot \text{IR6} \cdot \overline{\text{IR5}} \cdot \overline{\text{IR4}} \cdot \text{W2}$$

4.1.3 翻译成多分支程序

观察硬连线信号, 事实上如果写成 VHDL 语句, 我们可以将 $SWCBA$ 信号合并. 然后再在 $\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA}$ 分支上将 IR_{7654} 合并. 用两个大 switch 语句完成逻辑分类.

```vhdl
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;
entity CPU is
        port (
                CLR,C,Z,T3,W1,W2,W3: in std_logic;
                IRH:in std_logic_vector(3 downto 0);
                SWCBA:in std_logic_vector(2 downto 0);
                SELCTL,ABUS,M,SEL1,SEL0,SEL2,SEL3,DRW,SBUS,LIR,MBUS,MEMW,LAR,ARINC,LPC,
                PCINC,PCADD,CIN,LONG,SHORT,STOP,LDC,LDZ: out std_logic;
                S:out std_logic_vector(3 downto 0);
                CP1,CP2,CP3:out std_logic;
                QD:in std_logic
        );
end CPU;

architecture arc of CPU is
signal ST0,ST0_1,ST0_2,STOP_1,STOP_2: std_logic;
begin
        CP1 <= '1';
        CP2 <= '1';
        CP3 <= QD;

        with SWCBA select
                STOP <= '0'                                     when "000",
                                STOP_1 or STOP_2        when others;
        ST0 <= ST0_1;

        process (CLR, T3)
        begin
                --- 任何时候按下CLR, 都会返回
                if (CLR = '0') then
                        ST0_1   <= '0';
                        STOP_1  <= '1';
                --- 如果到节拍电位下降沿, T3ST0_1 |= ST0_2
                elsif (T3'event and T3 = '0') then
```

```vhdl
                    if (ST0_2 = '1') then
                            ST0_1 <= '1';
                    end if;
            end if;
    end process;

    process (SWCBA, IRH, W1, W2, W3, ST0, C, Z)
    begin
            -- 初始化和状态参数
            SHORT <= '0';
            LONG <= '0';
            -- 设置STOP
            STOP_2 <= '1';
            -- 设置标志ST0
            ST0_2 <= '0';
            -- ALU
            ABUS <= '0';
            M <= '0';
            CIN <= '0';
            S <= "0000";
            ARINC <= '0';
            -- 保存标志Z
            LDZ <= '0';
            -- 保存标志C
            LDC <= '0';
            SBUS <= '0';
            MBUS <= '0';
            -- 控制台操作标志
            SELCTL <= '0';
            -- RD1~RD0
            SEL3 <= '0';
            SEL2 <= '0';
            -- RS1~RS0
            SEL1 <= '0';
            SEL0 <= '0';
            -- 送指令寄存器标志
            LIR <= '0';
            -- 送地址寄存器标志
            LAR <= '0';
            -- 送程序计数器标志
            LPC <= '0';
            -- (~R)/W
            MEMW <= '0';
            DRW <= '0';
            -- 程序计数器自增标志
            PCINC <= '0';
```

```vhdl
            —— 程序计数器增量标志
            PCADD <= '0';
            case SWCBA is
                    when "000" =>  ——执行程序
                            case ST0 is
                                    when '0' =>
                                            —— load pc
                                            LPC <= W1;
                                            SBUS <= W1;
                                            ST0_2 <= W1;
                                            SHORT <= W1;
                                            STOP_2 <= '0';
                                    when '1' =>
                                            if(W1='1')then
                                                    LIR<=W1;
                                                    PCINC<=W1;
                                            else
                                            case IRH is
                                                    when "0001" =>  ——ADD
                                                            —— ABUS = W2
                                                            ABUS <= W2;
                                                            CIN <= W2;
                                                            —— 选择加法
                                                            —— 选择算术运算，已经被初始化为M0
                                                            S <= "1001";
                                                            —— 加法操作
                                                            DRW <= W2;
                                                            LDZ <= W2;
                                                            LDC <= W2;
                                                    when "0010" =>  —— SUB
                                                            —— 选择算术运算，选择减法
                                                            —— 已经被初始化为M0
                                                            S <= "0110";
                                                            —— 减法操作
                                                            ABUS <= W2;
                                                            DRW <= W2;
                                                            LDZ <= W2;
                                                            LDC <= W2;
                                                    when "0011" =>  —— AND
                                                            —— 选择逻辑运算，与运算
                                                            M <= W2;
                                                            S <= "1011";
                                                            ABUS <= W2;
                                                            DRW <= W2;
                                                            LDZ <= W2;
                                                    when "0100" => —— INC
```

```vhdl
                    —— 选择算术运算，与运算
                    —— 已经被初始化为M0
        S <= "0000";
        ABUS <= W2;
        DRW <= W2;
        LDZ <= W2;
        LDC <= W2;
when "0101" =>   —— LD
        —— 选择算术运算，传送（保留原值）B
        M <= W2;
        S <= "1010";
        ABUS <= W2;
        LONG<=W2;
        LAR <= W2;
        MBUS <= W3;
        DRW <= W3;
when "0110" =>   —— ST
        LONG<=W2;
        —— 设定...
        M <= W2 or W3;
        if(W2='1')then
                S<="1111";
        else
                S<="1010";
        end if;
        ABUS <= W2 or W3;
        LAR <= W2;
        MEMW <= W3;
when "0111" =>   —— JC
        PCADD <= C and W2;
when "1000" =>   —— JZ
        PCADD <= Z and W2;
when "1001" =>   —— JMP
        —— 设定算术运算
        M <= W2;
        S <= "1111";
        ABUS <= W2;
        LPC <= W2;
when "1010" =>   —— OUT
        —— 设定算术运算
        M <= W2;
        S <= "1010";
        ABUS <= W2;
when "1011" =>   —— SSP
        SEL3<='1';
        LONG<=W2;
```

```vhdl
                                        M <= W2 or W3;
                                        if (W2 = '1') then
                                                S <= "1000";
                                        elsif (W3 = '1') then
                                                S <= "1010";
                                        end if;
                                        ABUS <= W2 or W3;
                                        LAR <= W2;
                                        MEMW <= W3;
                                when "1100" =>  -- PUSH
                                        --无法自减PUSH
                                        M <= W2 or W3;
                                        if (W2 = '1') then
                                                S <= "1111";
                                        elsif (W3 = '1') then
                                                S <= "1010";
                                        end if;
                                        ABUS <=W2 or W3;
                                        LAR <= W2;
                                        MEMW <= W3;
                                        LONG <= W2;
                                when "1101" =>  -- MOV B->A
                                        -- 选择逻辑运算，MOV 运算
                                        M <= W2;
                                        S <= "1010";
                                        ABUS <= W2;
                                        DRW <= W2;
                                        LDZ <= W2;
                                when "1110" =>  -- STP
                                        STOP_2 <= W2;
                                when "1111" =>  -- LSP
                                        LONG<=W2;
                                        M <= W2;
                                        S <= "1000";
                                        ABUS <= W2;
                                        LAR <= W2;
                                        MBUS <= W3;
                                        DRW <= W3;
                                when others =>  -- 公操作
                            end case;
                                end if;
                            when others =>
                                        -- 不可能到这吧?
                    end case;
                when "001" =>
                    --      SEL0<=ST0;
```

```vhdl
            —— SBUS = (ST0=0 or ST0=1) and W1
            SBUS <= W1;
            —— STOP = (ST0=0 or ST0=1) and W1
            STOP_2 <= W1;
            —— SHORT = (ST0=0 or ST0=1) and W1
            SHORT <= W1;
            —— SELCTL = (ST0=0 or ST0=1) and W1
            SELCTL <= W1;
            —— LAR = (ST0=0) and W1
            LAR <= W1 and (not ST0);
            —— LAR = (ST0=1) and W1
            ARINC <= W1 and ST0;
            —— MEMW = (ST0=1) and W1
            MEMW <= W1 and ST0;
            ST0_2 <= W1;
    when "010" =>
            —— SHORT = (ST0=0 or ST0=1) and W1
            SHORT<=W1;
            —— SELCTL = (ST0=0 or ST0=1) and W1
            SELCTL <= W1;
            —— STOP = (ST0=0 or ST0=1) and W1
            STOP_2<=W1;
            —— SBUS = (ST0=0) and W1
            SBUS<=W1 and (not ST0);
            —— LAR = (ST0=0) and W1
            LAR<=W1 and (not ST0);
            —— MBUS = (ST0=1) and W1
            MBUS<=W1 and ST0;
            —— ARINC = (ST0=1) and W1
            ARINC<=W1 and ST0;
            ST0_2<=W1;
    when "011" =>
            —— SELCTL = W1 or W2
            SELCTL <= '1';
            —— STOP = W1 or W2
            STOP_2 <= W1 or W2;
            —— SEL0 = W1 or W2
            SEL0<=W1 or W2;
            —— SEL1 = W2
            SEL1<=W2;
            —— SEL2 = 0
            —— SEL3 = W2
            SEL3<=W2;
    when "100" =>
            —— SELCTL = (ST0=0 or ST0=1) and (W1 or W2)
            SELCTL <= '1';
```

```
                                  —— SBUS = (ST0=0 or ST0=1) and (W1 or W2)
                                  SBUS <= W1 or W2;
                                  —— STOP = (ST0=0 or ST0=1) and (W1 or W2)
                                  STOP_2 <= W1 or W2;
                                  —— DRW = (ST0=0 or ST0=1) and (W1 or W2)
                                  DRW <= W1 or W2;
                                  —— SEL0 = (ST0=0 or ST0=1) and W1
                                  SEL0 <= W1;
                                  —— SEL1 = ((ST0=0) and W1) or ((ST0=1) and W2)
                                  SEL1 <= ((not ST0) and W1) or (ST0 and W2);
                                  —— SEL2 = (ST0=0 or ST0=1) and W2
                                  SEL2 <= W2;
                                  —— SEL3 = (ST0=1) and (W1 or W2)
                                  SEL3 <= ST0 and (W1 or W2);
                                  ST0_2 <= W2;
                        when others=>
                end case;
        end process;
end arc;
```

4.2 流水硬连线控制器

4.2.1 设计硬连线控制器运行流程图

流水硬连线和硬连线的 *SW* 部分几乎是完全一样的. 只不过 LIR 和 PCINC 被合并到了指令运行周期中.
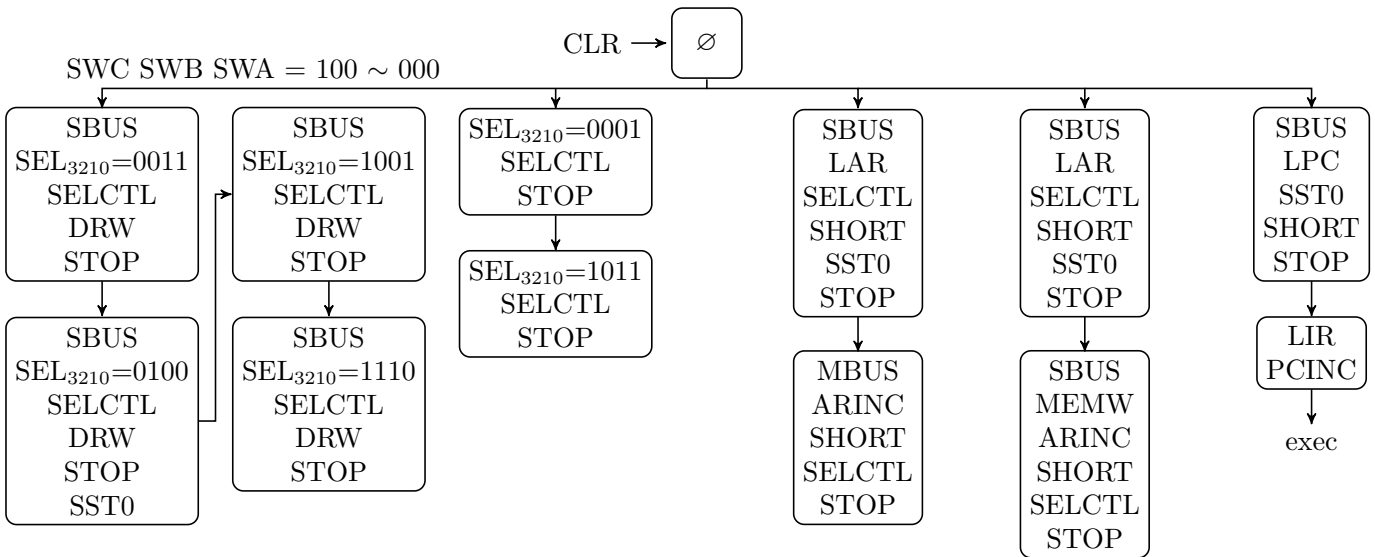
4.2.2　翻译成硬连线信号

SBUS ←

$$(W1 + W2) \cdot SWC \cdot \overline{SWB} \cdot \overline{SWA} +$$

$$W1 \cdot \overline{SWC} \cdot SWB \cdot \overline{SWA} \cdot \overline{ST0} +$$

$$W1 \cdot \overline{SWC} \cdot \overline{SWB} \cdot SWA +$$

$$W1 \cdot \overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{ST0}$$

MBUS ←

$$W1 \cdot \overline{SWC} \cdot SWB \cdot \overline{SWA} \cdot ST0 +$$

$$W2 \cdot \overline{IR7} \cdot IR6 \cdot \overline{IR5} \cdot IR4 \cdot \overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA}$$

ABUS ←

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot \overline{IR6} \cdot \overline{IR5} \cdot IR4 \cdot W1 +$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot \overline{IR6} \cdot IR5 \cdot \overline{IR4} \cdot W1 +$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot \overline{IR6} \cdot IR5 \cdot IR4 \cdot W1 +$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot IR6 \cdot \overline{IR5} \cdot \overline{IR4} \cdot W1 +$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot IR6 \cdot \overline{IR5} \cdot IR4 \cdot W1 +$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot IR6 \cdot IR5 \cdot \overline{IR4} \cdot (W1 + W2) +$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot IR7 \cdot \overline{IR6} \cdot \overline{IR5} \cdot IR4 \cdot W1 +$$

$$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot IR7 \cdot \overline{IR6} \cdot IR5 \cdot \overline{IR4} \cdot W1$$

LAR ←

$$W1 \cdot \overline{SWC} \cdot SWB \cdot \overline{SWA} \cdot \overline{ST0} +$$

$W1 \cdot \overline{SWC} \cdot \overline{SWB} \cdot SWA \cdot \overline{ST0}+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot IR6 \cdot \overline{IR5} \cdot IR4 \cdot W1+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot IR6 \cdot IR5 \cdot \overline{IR4} \cdot W1$

SST0 ←

$W1 \cdot \overline{SWC} \cdot SWB \cdot \overline{SWA} \cdot \overline{ST0}+$

$W2 \cdot SWC \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{ST0}+$

$W1 \cdot \overline{SWC} \cdot \overline{SWB} \cdot SWA \cdot \overline{ST0}+$

$W1 \cdot \overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{ST0}$

SHORT ←

$W1 \cdot \overline{SWC} \cdot SWB \cdot \overline{SWA}$

$W1 \cdot \overline{SWC} \cdot \overline{SWB} \cdot SWA$

$W1 \cdot \overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{ST0}+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot \overline{IR6} \cdot \overline{IR5} \cdot \overline{IR4} \cdot W1+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot \overline{IR6} \cdot \overline{IR5} \cdot IR4 \cdot W1+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot \overline{IR6} \cdot IR5 \cdot \overline{IR4} \cdot W1+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot \overline{IR6} \cdot IR5 \cdot IR4 \cdot W1+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot IR6 \cdot \overline{IR5} \cdot \overline{IR4} \cdot W1+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot IR6 \cdot IR5 \cdot IR4 \cdot W1 \cdot \overline{C}+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot IR7 \cdot \overline{IR6} \cdot \overline{IR5} \cdot \overline{IR4} \cdot W1 \cdot \overline{Z}$

ARINC ←

$W1 \cdot \overline{SWC} \cdot SWB \cdot \overline{SWA} \cdot ST0+$

$W1 \cdot \overline{SWC} \cdot \overline{SWB} \cdot SWA \cdot ST0$

MEMW ←

$W1 \cdot \overline{SWC} \cdot \overline{SWB} \cdot SWA \cdot ST0+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot IR6 \cdot IR5 \cdot \overline{IR4} \cdot W2$

LIR ←

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot \overline{IR6} \cdot \overline{IR5} \cdot \overline{IR4} \cdot W1+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot \overline{IR6} \cdot \overline{IR5} \cdot IR4 \cdot W1+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot \overline{IR6} \cdot IR5 \cdot \overline{IR4} \cdot W1+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot \overline{IR6} \cdot IR5 \cdot IR4 \cdot W1+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot IR6 \cdot \overline{IR5} \cdot \overline{IR4} \cdot W1+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot IR6 \cdot IR5 \cdot IR4 \cdot W1 \cdot \overline{C}+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot IR7 \cdot \overline{IR6} \cdot \overline{IR5} \cdot \overline{IR4} \cdot W1 \cdot \overline{Z}+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot IR6 \cdot IR5 \cdot IR4 \cdot W2 \cdot C+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot IR7 \cdot \overline{IR6} \cdot \overline{IR5} \cdot \overline{IR4} \cdot W2 \cdot Z+$

$W2 \cdot \overline{IR7} \cdot IR6 \cdot \overline{IR5} \cdot IR4 \cdot \overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA}+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot IR6 \cdot IR5 \cdot \overline{IR4} \cdot W2+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{ST0} \cdot W1$

CIN ←

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot \overline{IR6} \cdot \overline{IR5} \cdot \overline{IR4} \cdot W1$

M ←

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot \overline{IR6} \cdot IR5 \cdot IR4 \cdot W2+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot IR6 \cdot \overline{IR5} \cdot IR4 \cdot W2+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot \overline{IR7} \cdot IR6 \cdot IR5 \cdot \overline{IR4} \cdot (W2 + W3)+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot IR7 \cdot \overline{IR6} \cdot \overline{IR5} \cdot IR4 \cdot W2+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot IR7 \cdot \overline{IR6} \cdot IR5 \cdot \overline{IR4} \cdot W2$

SEL0←

$SWC \cdot \overline{SWB} \cdot \overline{SWA} \cdot W1$

SEL1←

$SWC \cdot \overline{SWB} \cdot \overline{SWA} \cdot W2 \cdot ST0+$

$SWC \cdot \overline{SWB} \cdot \overline{SWA} \cdot W1 \cdot \overline{ST0}$

SEL2←

$SWC \cdot \overline{SWB} \cdot \overline{SWA} \cdot W2$

SEL3←

$SWC \cdot \overline{SWB} \cdot \overline{SWA} \cdot W1 \cdot ST0+$

$SWC \cdot \overline{SWB} \cdot \overline{SWA} \cdot W2 \cdot \overline{ST0}$

STOP←

$SWA + SWB + SWC+$

$\overline{SWC} \cdot \overline{SWB} \cdot \overline{SWA} \cdot IR7 \cdot IR6 \cdot IR5 \cdot \overline{IR4} \cdot ST0 \cdot W2$

SELCTL←

$$\overline{\text{SWA}} + \overline{\text{SWB}} + \overline{\text{SWC}}$$

DRW←

$$\text{SWC} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}}+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \text{ST0} \cdot \overline{\text{IR7}} \cdot \overline{\text{IR6}} \cdot \overline{\text{IR5}} \cdot \text{IR4} \cdot \text{W2}+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \text{ST0} \cdot \overline{\text{IR7}} \cdot \overline{\text{IR6}} \cdot \text{IR5} \cdot \overline{\text{IR4}} \cdot \text{W2}+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \text{ST0} \cdot \overline{\text{IR7}} \cdot \overline{\text{IR6}} \cdot \text{IR5} \cdot \text{IR4} \cdot \text{W2}+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \text{ST0} \cdot \overline{\text{IR7}} \cdot \text{IR6} \cdot \overline{\text{IR5}} \cdot \overline{\text{IR4}} \cdot \text{W2}+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \text{ST0} \cdot \overline{\text{IR7}} \cdot \text{IR6} \cdot \overline{\text{IR5}} \cdot \text{IR4} \cdot \text{W3}$$

PCADD←

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \text{ST0} \cdot \overline{\text{IR7}} \cdot \text{IR6} \cdot \text{IR5} \cdot \text{IR4} \cdot \text{C} \cdot \text{W2}+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \text{ST0} \cdot \text{IR7} \cdot \overline{\text{IR6}} \cdot \overline{\text{IR5}} \cdot \overline{\text{IR4}} \cdot \text{Z} \cdot \text{W2}$$

PCINC ←

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \overline{\text{IR7}} \cdot \overline{\text{IR6}} \cdot \overline{\text{IR5}} \cdot \overline{\text{IR4}} \cdot \text{W1}+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \overline{\text{IR7}} \cdot \overline{\text{IR6}} \cdot \overline{\text{IR5}} \cdot \text{IR4} \cdot \text{W1}+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \overline{\text{IR7}} \cdot \overline{\text{IR6}} \cdot \text{IR5} \cdot \overline{\text{IR4}} \cdot \text{W1}+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \overline{\text{IR7}} \cdot \overline{\text{IR6}} \cdot \text{IR5} \cdot \text{IR4} \cdot \text{W1}+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \overline{\text{IR7}} \cdot \text{IR6} \cdot \overline{\text{IR5}} \cdot \overline{\text{IR4}} \cdot \text{W1}+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \overline{\text{IR7}} \cdot \text{IR6} \cdot \text{IR5} \cdot \text{IR4} \cdot \text{W1} \cdot \overline{C}+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \text{IR7} \cdot \overline{\text{IR6}} \cdot \overline{\text{IR5}} \cdot \overline{\text{IR4}} \cdot \text{W1} \cdot \overline{Z}+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \overline{\text{IR7}} \cdot \text{IR6} \cdot \text{IR5} \cdot \text{IR4} \cdot \text{W2} \cdot C+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \text{IR7} \cdot \overline{\text{IR6}} \cdot \overline{\text{IR5}} \cdot \overline{\text{IR4}} \cdot W2 \cdot Z+$$

$$W2 \cdot \overline{\text{IR7}} \cdot \text{IR6} \cdot \overline{\text{IR5}} \cdot \text{IR4} \cdot \overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}}+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \overline{\text{IR7}} \cdot \text{IR6} \cdot \text{IR5} \cdot \overline{\text{IR4}} \cdot W2+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \overline{\text{ST0}} \cdot W1$$

LPC←

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \overline{\text{ST0}} \cdot W1$$

LDC←

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \text{ST0} \cdot \overline{\text{IR7}} \cdot \overline{\text{IR6}} \cdot \overline{\text{IR5}} \cdot \text{IR4} \cdot W1+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \text{ST0} \cdot \overline{\text{IR7}} \cdot \overline{\text{IR6}} \cdot \text{IR5} \cdot \overline{\text{IR4}} \cdot W1+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \text{ST0} \cdot \overline{\text{IR7}} \cdot \overline{\text{IR6}} \cdot \text{IR5} \cdot \text{IR4} \cdot W1+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \text{ST0} \cdot \overline{\text{IR7}} \cdot \text{IR6} \cdot \overline{\text{IR5}} \cdot \overline{\text{IR4}} \cdot W1$$

LDZ←

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \text{ST0} \cdot \overline{\text{IR7}} \cdot \overline{\text{IR6}} \cdot \overline{\text{IR5}} \cdot \text{IR4} \cdot W1+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \text{ST0} \cdot \overline{\text{IR7}} \cdot \overline{\text{IR6}} \cdot \text{IR5} \cdot \overline{\text{IR4}} \cdot W1+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \text{ST0} \cdot \overline{\text{IR7}} \cdot \overline{\text{IR6}} \cdot \text{IR5} \cdot \text{IR4} \cdot W1+$$

$$\overline{\text{SWC}} \cdot \overline{\text{SWB}} \cdot \overline{\text{SWA}} \cdot \text{ST0} \cdot \overline{\text{IR7}} \cdot \text{IR6} \cdot \overline{\text{IR5}} \cdot \overline{\text{IR4}} \cdot W1$$

4.2.3 翻译成多分支程序

```vhdl
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;
entity CPU is
        port (
                CLR,C,Z,T3,W1,W2,W3: in std_logic;
```

```vhdl
                IRH:in std_logic_vector(3 downto 0);
                SWCBA:in std_logic_vector(2 downto 0);
                SELCTL,ABUS,M,SEL1,SEL0,SEL2,SEL3,DRW,SBUS,LIR,MBUS,MEMW,LAR,ARINC,LPC,
                PCINC,PCADD,CIN,LONG,SHORT,STOP,LDC,LDZ: out std_logic;
                S:out std_logic_vector(3 downto 0);
                CP1,CP2,CP3:out std_logic;
                QD:in std_logic
        );
end CPU;

architecture arc of CPU is
signal ST0,ST0_1,ST0_2,STOP_1,STOP_2: std_logic;
begin

        CP1 <= '1';
        CP2 <= '1';
        CP3 <= QD;

        with SWCBA select
                STOP <= '0'                                             when "000",
                                STOP_1 or STOP_2                when others;
        ST0 <= ST0_1;

        process (CLR, T3)
        begin
                -- 任何时候按下CLR，都会返回
                if (CLR = '0') then
                        ST0_1   <= '0';
                        STOP_1  <= '1';
                -- 如果到节拍电位下降沿，T3ST0_1 |= ST0_2
                elsif (T3'event and T3 = '0') then
                        if (ST0_2 = '1') then
                                ST0_1 <= '1';
                        end if;
                end if;
        end process;

        process (SWCBA, IRH, W1, W2, W3, ST0, C, Z)
        begin
                -- 初始化和状态参数
                SHORT <= '0';
                LONG <= '0';
                -- 设置STOP
                STOP_2 <= '1';
                -- 设置标志ST0
                ST0_2 <= '0';
```

```vhdl
―― ALU
ABUS <= '0';
M <= '0';
CIN <= '0';
S <= "0000";
ARINC <= '0';
―― 保存标志Z
LDZ <= '0';
―― 保存标志C
LDC <= '0';
SBUS <= '0';
MBUS <= '0';
―― 控制台操作标志
SELCTL <= '0';
―― RD1~RD0
SEL3 <= '0';
SEL2 <= '0';
―― RS1~RS0
SEL1 <= '0';
SEL0 <= '0';
―― 送指令寄存器标志
LIR <= '0';
―― 送地址寄存器标志
LAR <= '0';
―― 送程序计数器标志
LPC <= '0';
―― (~R)/W
MEMW <= '0';
DRW <= '0';
―― 程序计数器自增标志
PCINC <= '0';
―― 程序计数器增量标志
PCADD <= '0';
case SWCBA is
        when "000" =>  ――执行程序
                case ST0 is
                        when '0' =>
                                ―― load pc
                                LPC <= W1;
                                SBUS <= W1;
                                ST0_2 <= W1;
                                SHORT <= W1;
                                STOP_2 <= '0';
                        when '1' =>
                        case IRH is
                                when "0000" =>  ―― NOP
```

```
                                  —— 设定PC
                        LIR <= W1;
                        PCINC <= W1;
                                  —— 短周期
                        SHORT <= W1;
            when "0001" =>  ——ADD ()
                                  —— 设定PC
                        LIR <= W1;
                        PCINC <= W1;
                                  —— 短周期
                        SHORT <= W1;
                                  —— ABUS = W1
                        ABUS <= W1;
                        CIN <= W1;
                                  —— 选择加法
                                  —— 选择算术运算，传送 B
                                  —— 已经被初始化为M0
                        S <= "1001";
                                  —— 加法操作
                        DRW <= W1;
                        LDZ <= W1;
                        LDC <= W1;
            when "0010" =>  —— SUB ()
                                  —— 设定PC
                        LIR <= W1;
                        PCINC <= W1;
                                  —— 短周期
                        SHORT <= W1;
                                  —— 选择算术运算，选择减法
                                  —— 已经被初始化为M0
                        S <= "0110";
                                  —— 减法操作
                        ABUS <= W1;
                        DRW <= W1;
                        LDZ <= W1;
                        LDC <= W1;
            when "0011" =>  —— AND ()
                                  —— 设定PC
                        LIR <= W1;
                        PCINC <= W1;
                                  —— 短周期
                        SHORT <= W1;
                                  —— 选择逻辑运算，与运算
                        M <= W1;
                        S <= "1011";
                        ABUS <= W1;
```

```vhdl
                    DRW <= W1;
                    LDZ <= W1;
        when "0100" => —— INC ()
                    —— 设定PC
                    LIR <= W1;
                    PCINC <= W1;
                    —— 短周期
                    SHORT <= W1;
                    —— 选择算术运算，与运算
                    —— 已经被初始化为M0
                    S <= "0000";
                    ABUS <= W1;
                    DRW <= W1;
                    LDZ <= W1;
                    LDC <= W1;
        when "0101" =>  —— LD
                    —— 选择算术运算，传送 B
                    M <= W1;
                    S <= "1010";
                    ABUS <= W1;
                    LAR <= W1;
                    —— 设定PC
                    LIR <= W2;
                    PCINC <= W2;
                    MBUS <= W2;
                    DRW <= W2;
        when "0110" =>  —— ST
                    —— 设定...
                    M <= W1 or W2;
                    if(W1='1')then
                            S<="1111";
                    else
                            S<="1010";
                    end if;
                    ABUS <= W1 or W2;
                    LAR <= W1;
                    MEMW <= W2;
                    —— 设定PC
                    LIR <= W2;
                    PCINC <= W2;
        when "0111" =>  —— JC
                    —— 设定PC
                    LIR <= (W1 and (not C)) or (W2 and C);
                    PCINC <= (W1 and (not C)) or (W2 and C);
                    PCADD <= C and W1;
                    SHORT <= W1 and (not C);
```

```vhdl
when "1000" =>  -- JZ
        -- 设定PC
        LIR <= (W1 and (not Z)) or (W2 and Z);
        PCINC <= (W1 and (not Z)) or (W2 and Z);
        PCADD <= Z and W1;
        SHORT <= W1 and (not Z);
when "1001" =>  -- JMP
        -- 设定算术运算
        M <= W1;
        S <= "1111";
        ABUS <= W1;
        LPC <= W1;
        -- 设定PC
        LIR <= W2;
        PCINC <= W2;
when "1010" =>  -- OUT
        -- 设定PC
        LIR <= W1;
        PCINC <= W1;
        -- 短周期
        SHORT <= W1;
        -- 设定算术运算
        M <= W1;
        S <= "1010";
        ABUS <= W1;
when "1011" =>  -- SSP
        SEL3<='1';
        M <= W1 or W2;
        if (W1 = '1') then
                S <= "1000";
        elsif (W2 = '1') then
                -- or S <= "1111"
                S <= "1010";
        end if;
        ABUS <= W1 or W2;
        LAR <= W1;
        MEMW <= W2;
        -- 设定PC
        LIR <= W2;
        PCINC <= W2;
when "1100" =>  -- PUSH
        M <= W1 or W2;
        CIN <= W3;
        if (W1 = '1') then
                S <= "1111";
        elsif (W2 = '1') then
```

```vhdl
                                S <= "1010";
                    elsif (W3 = '1') then
                                S <= "1111";
                    end if;
                    ABUS <= W1 or W2 or W3;
                    LAR <= W1;
                    MEMW <= W2;
                    LONG <= W2;
                    DRW <= W3;
                    LIR <= W3;
                    PCINC <= W3;
            when "1101" =>  -- MOV B->A
                    -- 设定PC
                    LIR <= W1;
                    PCINC <= W1;
                    -- 短周期
                    SHORT <= W1;
                    -- 选择逻辑运算，MOV 运算
                    M <= W1;
                    S <= "1010";
                    ABUS <= W1;
                    DRW <= W1;
                    LDZ <= W1;
            when "1110" =>  -- STP
                    STOP_2 <= W1;
            when "1111" =>  -- LSP
                    M <= W1;
                    S <= "1000";
                    ABUS <= W1;
                    LAR <= W1;
                    MBUS <= W2;
                    DRW <= W2;
                    -- 设定PC
                    LIR <= W2;
                    PCINC <= W2;
            when others =>  -- 公操作
                    -- 设定PC
                    LIR <= W1;
                    PCINC <= W1;
        end case;
            when others =>
                    -- 不可能到这吧?
        end case;
    when "001" =>
--          SEL0<=ST0;
            -- SBUS = (ST0=0 or ST0=1) and W1
```

```vhdl
                SBUS <= W1;
                -- STOP = (ST0=0 or ST0=1) and W1
                STOP_2 <= W1;
                -- SHORT = (ST0=0 or ST0=1) and W1
                SHORT <= W1;
                -- SELCTL = (ST0=0 or ST0=1) and W1
                SELCTL <= W1;
                -- LAR = (ST0=0) and W1
                LAR <= W1 and (not ST0);
                -- LAR = (ST0=1) and W1
                ARINC <= W1 and ST0;
                -- MEMW = (ST0=1) and W1
                MEMW <= W1 and ST0;
                ST0_2 <= W1;
            when "010" =>
                -- SHORT = (ST0=0 or ST0=1) and W1
                SHORT<=W1;
                -- SELCTL = (ST0=0 or ST0=1) and W1
                SELCTL <= W1;
                -- STOP = (ST0=0 or ST0=1) and W1
                STOP_2<=W1;
                -- SBUS = (ST0=0) and W1
                SBUS<=W1 and (not ST0);
                -- LAR = (ST0=0) and W1
                LAR<=W1 and (not ST0);
                -- MBUS = (ST0=1) and W1
                MBUS<=W1 and ST0;
                -- ARINC = (ST0=1) and W1
                ARINC<=W1 and ST0;
                ST0_2<=W1;
            when "011" =>
                -- SELCTL = W1 or W2
                SELCTL <= '1';
                -- STOP = W1 or W2
                STOP_2 <= W1 or W2;
                -- SEL0 = W1 or W2
                SEL0<=W1 or W2;
                -- SEL1 = W2
                SEL1<=W2;
                -- SEL2 = 0
                -- SEL3 = W2
                SEL3<=W2;
            when "100" =>
                -- SELCTL = (ST0=0 or ST0=1) and (W1 or W2)
                SELCTL <= '1';
                -- SBUS = (ST0=0 or ST0=1) and (W1 or W2)
```

```vhdl
                        SBUS <= W1 or W2;
                        --- STOP = (ST0=0 or ST0=1) and (W1 or W2)
                        STOP_2 <= W1 or W2;
                        --- DRW = (ST0=0 or ST0=1) and (W1 or W2)
                        DRW <= W1 or W2;
                        --- SEL0 = (ST0=0 or ST0=1) and W1
                        SEL0 <= W1;
                        --- SEL1 = ((ST0=0) and W1) or ((ST0=1) and W2)
                        SEL1 <= ((not ST0) and W1) or (ST0 and W2);
                        --- SEL2 = (ST0=0 or ST0=1) and W2
                        SEL2 <= W2;
                        --- SEL3 = (ST0=1) and (W1 or W2)
                        SEL3 <= ST0 and (W1 or W2);
                        ST0_2 <= W2;
                  when others=>
            end case;
      end process;
end arc;
```

5　调试过程中的问题及讨论

6　设计调试小结