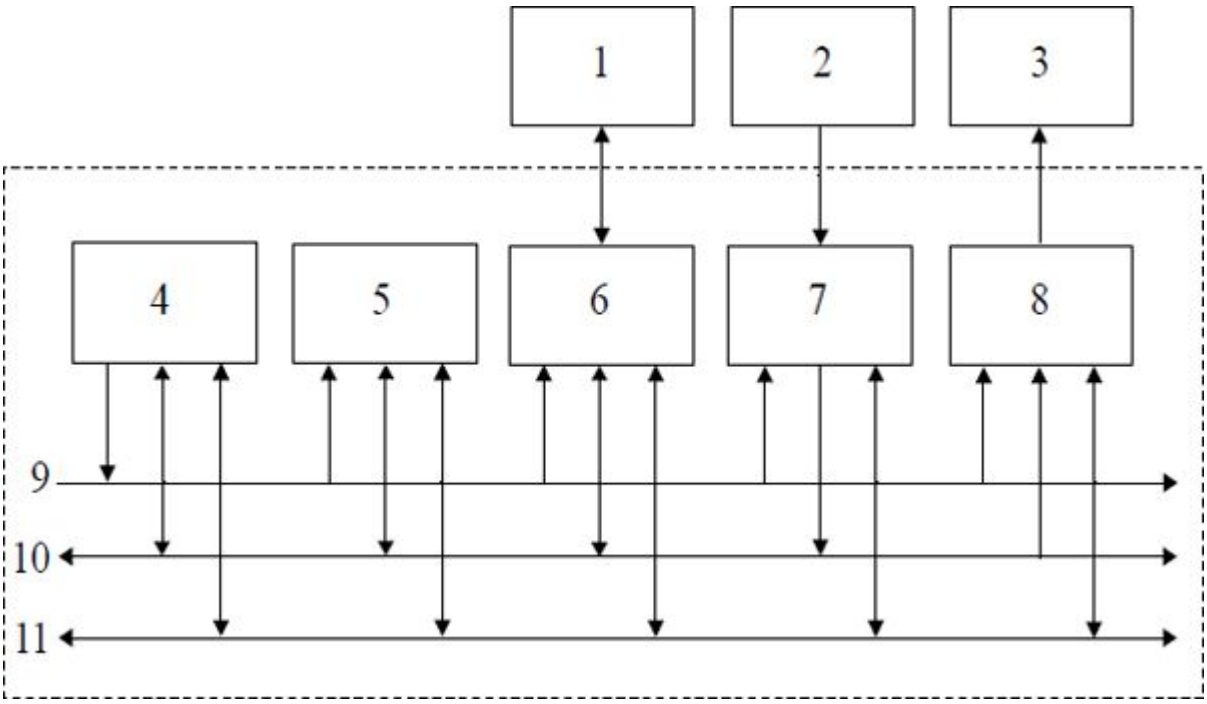
Q1.

The diagram below is a diagram of some of the components of a computer system.



Match the component names to the numbers shown in the diagram above by completing the tables below. Some of the numbers have already been written in for you.

Internal Components	
Data Bus	
Address Bus	
Control Bus	11
VDU Controller	
Disk Controller	6
Keyboard Controller	
Main Memory	
Processor	

External Components	
Keyboard	
Visual Display Unit	
Secondary Storage	1

(Total 6 marks)

Q2.

An integrated circuit manufacturer is looking to develop a new processor.

(a) What would be the direct consequence on potential performance of increasing the width of the data bus? _____

_____

increasing the width of the address bus? _____

_____

increasing the clock speed? _____

_____

(3)

(b) A company has designed a new peripheral and is developing the I / O controller for it.

(i) What do we mean by the term peripheral?

_____

_____

(1)

(ii) The I / O controller is an electronic circuit consisting of three parts. One of these parts is known as the I / O port.

What is the role of the I / O port?

_____

_____

(1)

(iii) Describe another part of the I / O controller.

_____

_____

(1)

(iv) Peripheral devices are not directly connected to the processor but make use of the system bus.

Give **two** reasons why it is **not** sensible to connect peripherals directly to the processor.

Reason 1 _____

_____

Reason 2 _____

_____

(2)

(Total 8 marks)

Q3.

The following registers are used in the Fetch-Execute cycle:

- Current Instruction Register (CIR)
- Memory Address Register (MAR)
- Memory Buffer Register (MBR)

- Program Counter (PC)
- Status Register (SR)

Describe, **using full sentences**, the steps involved in the Fetch-Execute cycle, making reference to how the registers above are used. Your description should cover the fetch, decode and execute phases of the cycle. You may use the abbreviations given above for the register names in your response; for example PC for Program Counter.

In your answer you will be assessed on your ability to use good English and to organise your answer clearly in complete sentences, using specialist vocabulary where appropriate.

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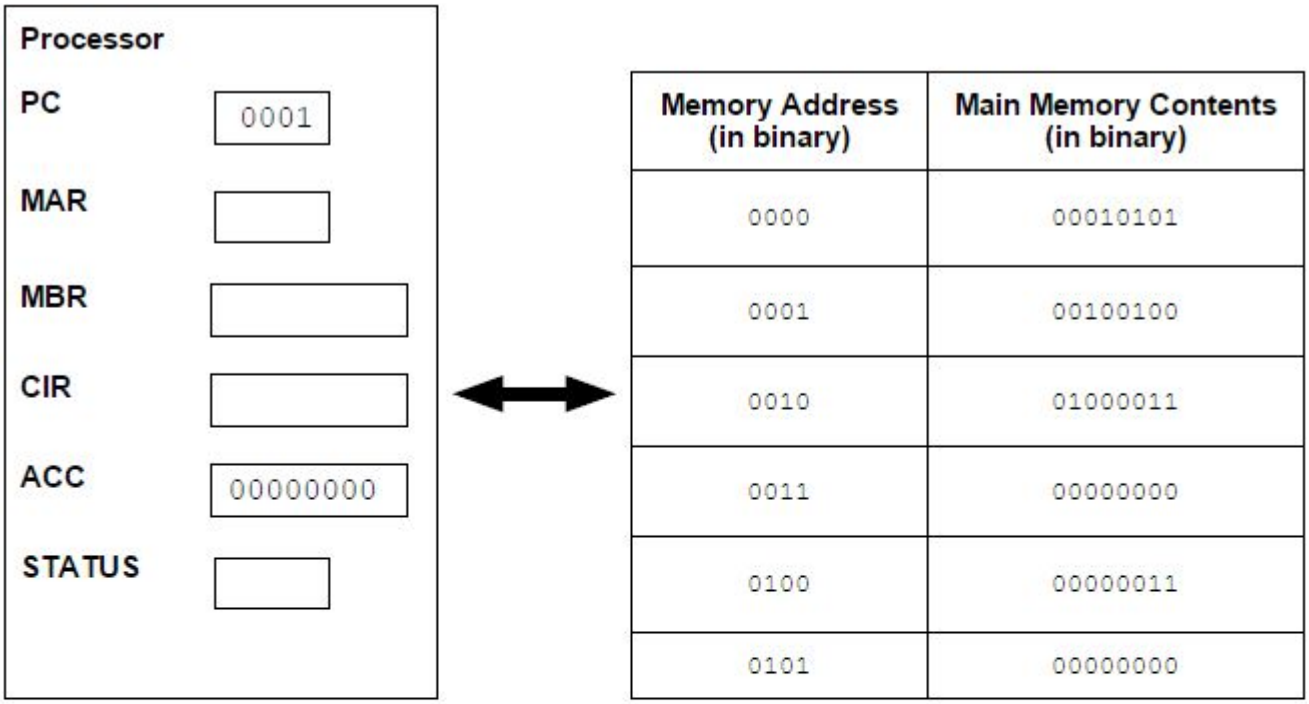
(Total 6 marks)

Q4.

The diagram below shows some of the registers used in the fetch-execute cycle of a simple processor and the contents of a small section of main memory that it is connected to by the system bus (◄►).



Memory Address (in binary)	Main Memory Contents (in binary)
0000	00010101
0001	00100100
0010	01000011
0011	00000000
0100	00000011
0101	00000000

OPCODE	INSTRUCTION	DESCRIPTION
0001	LOAD	Load the contents of the provided memory location into the accumulator
0010	ADD	Add the contents of the provided memory location to the current contents of the accumulator, storing the result in the accumulator
0100	STORE	Copy the contents of the accumulator into the provided memory location

(a) In the diagram above the first 4 bits of an instruction represent the opcode and give the type of instruction to be executed.

What name is given to the second 4 bits of an instruction?

_____

(1)

(b) (i) Currently the value in the Program Counter (PC) is example 0001.

Complete the table below by writing the values, expressed in binary, in the following registers after completing the fetch part of the fetch-execute cycle.

Register	Value
PC	
MAR	
MBR	

(3)

(ii) Describe what will happen during the decode and execute part of the cycle.

_____

_____

_____

_____

_____

_____

_____

(3)

(c) What would be the outcome of executing the instruction `01000011`?

_____

_____

_____

_____

(1)

(Total 8 marks)