Key to Tutorial 5
Memory Devices

Exercise 1

Let us consider the two following ROM devices:

1. How many 4-bit words does the memory device **M1** contain?

   We have to work out the depth of the memory device **M1**.
   256 Kib = (256 Ki / 4) words of 4 bits = 64 Ki words of 4 bits.
   The memory device M1 contains 64 Ki words of 4 bits.

2. How many 8-bit words does the memory device **M2** contain?

   We have to work out the depth of the memory device **M2**.
   512 Kib = (512 Ki / 8) words of 8 bits = 64 Ki words of 8 bits.
   The memory device M2 contains 64 Ki words of 8 bits (64 KiB).

3. How many address lines does each of the two memory devices have?

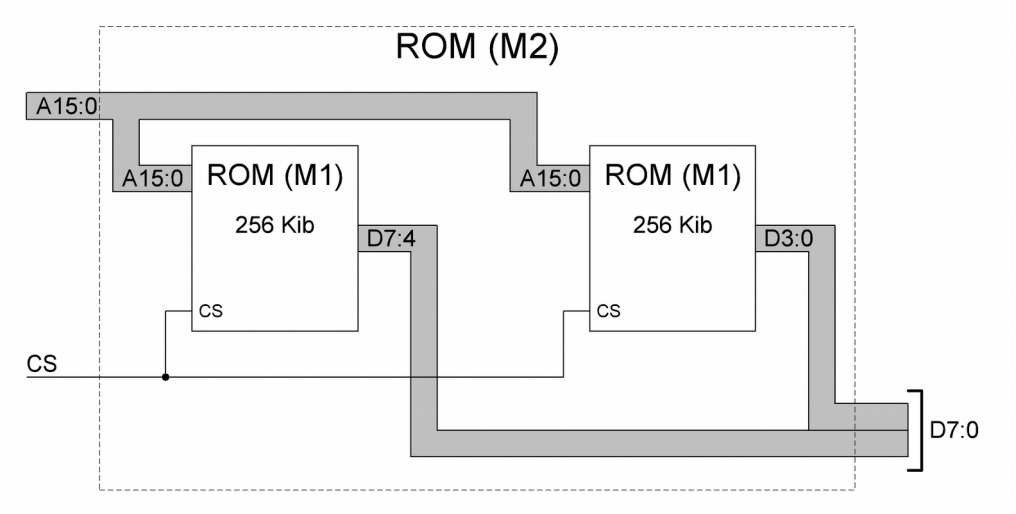
   The number of address lines can be determined from the memory depth.
   64 Ki words = 2^{16} words.
   Both of the memory devices have 16 address lines.

A memory device **M2** should be built from two memory devices **M1**.

4. In which way should the memory devices be connected to each other?

   A 4-bit data bus must be turned into an 8-bit data bus.
   Therefore, 2 memory devices M1 should be connected in parallel.

5. Draw the circuit diagram.



Exercise 2

A RAM device (**M1**) has a capacity of 2 Mib, a 4-bit data bus, a *CS* input and a *WE* input. A RAM device (**M2**) has a capacity of 4 Mib. The data and control buses of these two RAM devices are identical. A memory device **M2** should be built from several memory devices **M1**.

1. Work out the number of address lines for each of the two memory devices.

   The number of address lines can be determined from the memory depth.

   M1: 2 Mib = (2 Mi / 4) words of 4 bits = 512 Ki words of 4 bits.
   512 Ki words = 2^{19} words.
   The memory device M1 has 19 address lines.

   M2: 4 Mib = (4 Mi / 4) words of 4 bits = 1 Mi words of 4 bits.
   1 Mi words = 2^{20} words.
   The memory device M2 has 20 address lines.

2. In which way should the memory devices be connected to each other?

   A 19-bit address bus must be turned into a 20-bit address bus.
   Therefore, 2 memory devices M1 should be connected in series.

3. How many address lines are required to control the *CS* input of each memory device **M1**?

   The memory device **M2** has one more address line than the memory device **M1** (20 – 19 = 1).
   This address line should be used to control the *CS* of each memory device M1.

4. Draw the circuit diagram.

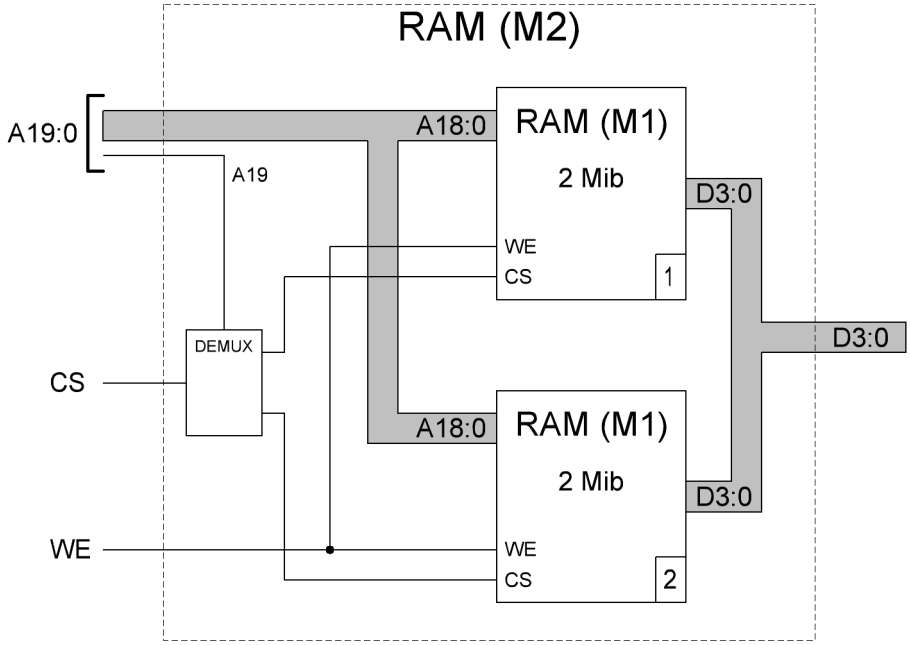
   Each *WE* input of the memory devices **M1** is connected to the *WE* inputs of the memory device **M2**. There is no particular difficulty for these kinds of entries.

   A demultiplexer should be used to select one of the memory devices **M1**. This demultiplexer will be controlled by the address line *A19*.

   - When *A19* = 0, the *CS* of the memory device **M2** is transferred to the *CS* of the first memory device **M1** (at the top of the diagram). The other output of the demultiplexer is set to 0 and the second memory device **M1** (at the bottom of the diagram) is deactivated.

   - When *A19* = 1, the *CS* of the memory device **M2** is transferred to the *CS* of the second memory device **M1**. The other output of the demultiplexer is set to 0 and the first memory device **M1** is deactivated.

   It can be noticed that when *CS* = 0, both of the memory devices **M1** are deactivated.



5. Which memory device **M1** is selected when the address 515_{10} is being read?

   The address line *A19* controls the demultiplexer; in other words, *A19* selects the first or the second memory device **M1**.
   $515_{10} = 00203_{16} \rightarrow A19 = 0 \rightarrow$ **The memory device M1 number 1 is selected.**

6. Which memory device **M1** is selected when the address $9A844_{16}$ is being written?

   Using the same line of reasoning:
   $9A844_{16} \rightarrow A19 = 1 \rightarrow$ **The memory device M1 number 2 is selected.**

Exercise 3

A RAM device (**M1**) has a capacity of 512 bytes and a 4-bit data bus. A RAM device (**M2**) has a capacity of 8 KiB and a 16-bit data bus. A memory device **M2** should be built from several memory devices **M1**.

1. Work out the number of cells and the size of the address bus for the two memory devices.

   M1 : 512 bytes = (512 × 8 / 4) words of 4 bits = **1 Ki words of 4 bits**.
   1 Ki words = 2^{10} words.
   The memory device M1 has 10 address lines and 1 Ki cells.

   M2 : 8 KiB = (8 Ki × 8 / 16) words of 16 bits = **4 Ki words of 16 bits**.
   4 Ki words = 2^{12} words.
   The memory device M2 has 12 address lines and 4 Ki cells.

2. How many memory devices should be put in series?

   A depth of 1 Ki words must be turned into a depth of 4 Ki words.
   Therefore, 4 memory devices should be put in series (4 Ki / 1 Ki = 4).

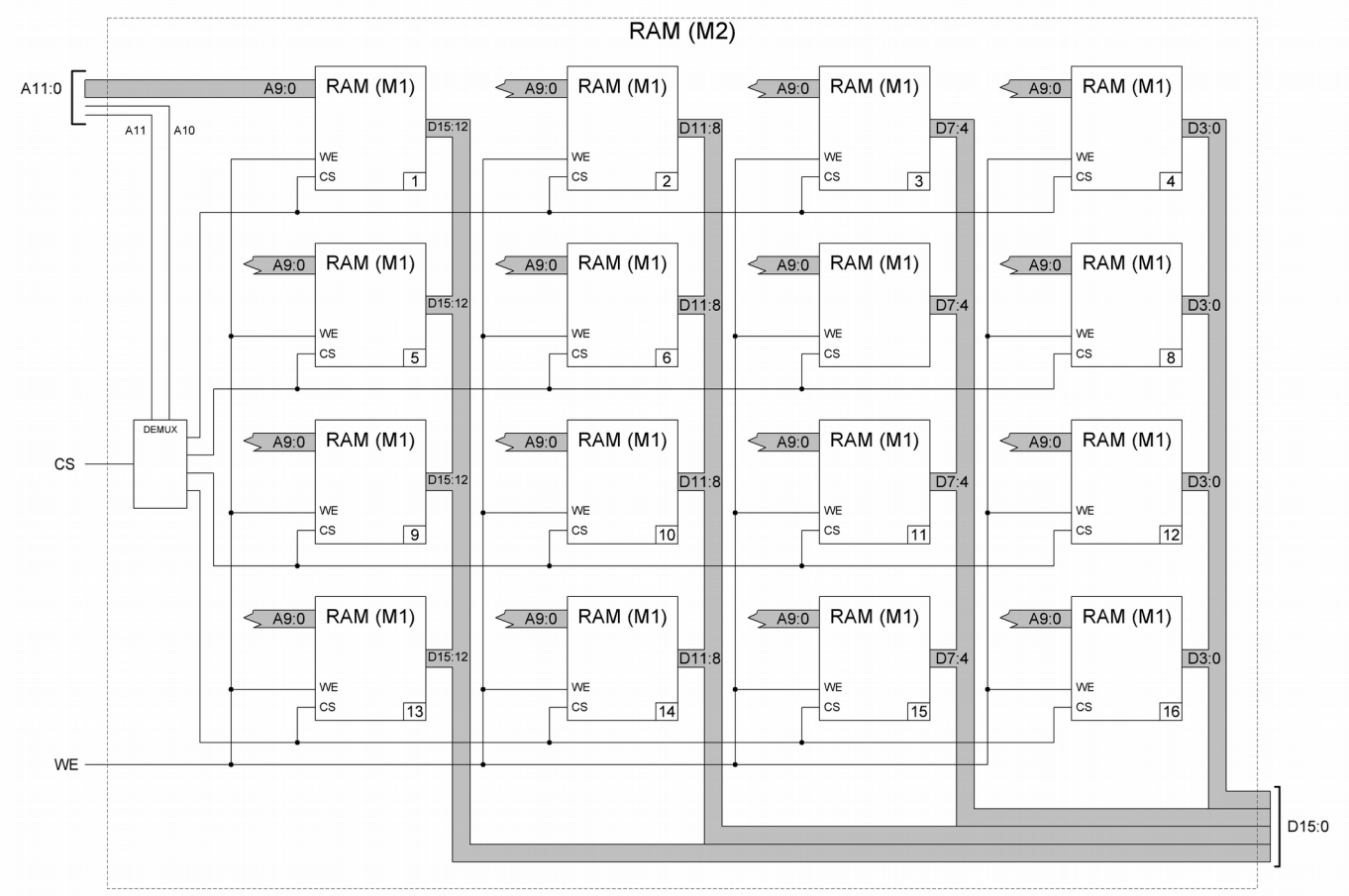
3. How many memory devices should be put in parallel?

   A 4-bit data bus must be turned into a 16-bit data bus.
   Therefore, 4 memory devices should be put in parallel (16 / 4 = 4).

4. How many address lines are required to control the *CS* input of each memory device **M1**?

   The memory device **M2** has two more address lines than the memory device **M1** (12 – 10 = 2).
   These two address lines should be used to control the *CS* of each memory device M1.

5. Draw the circuit diagram.



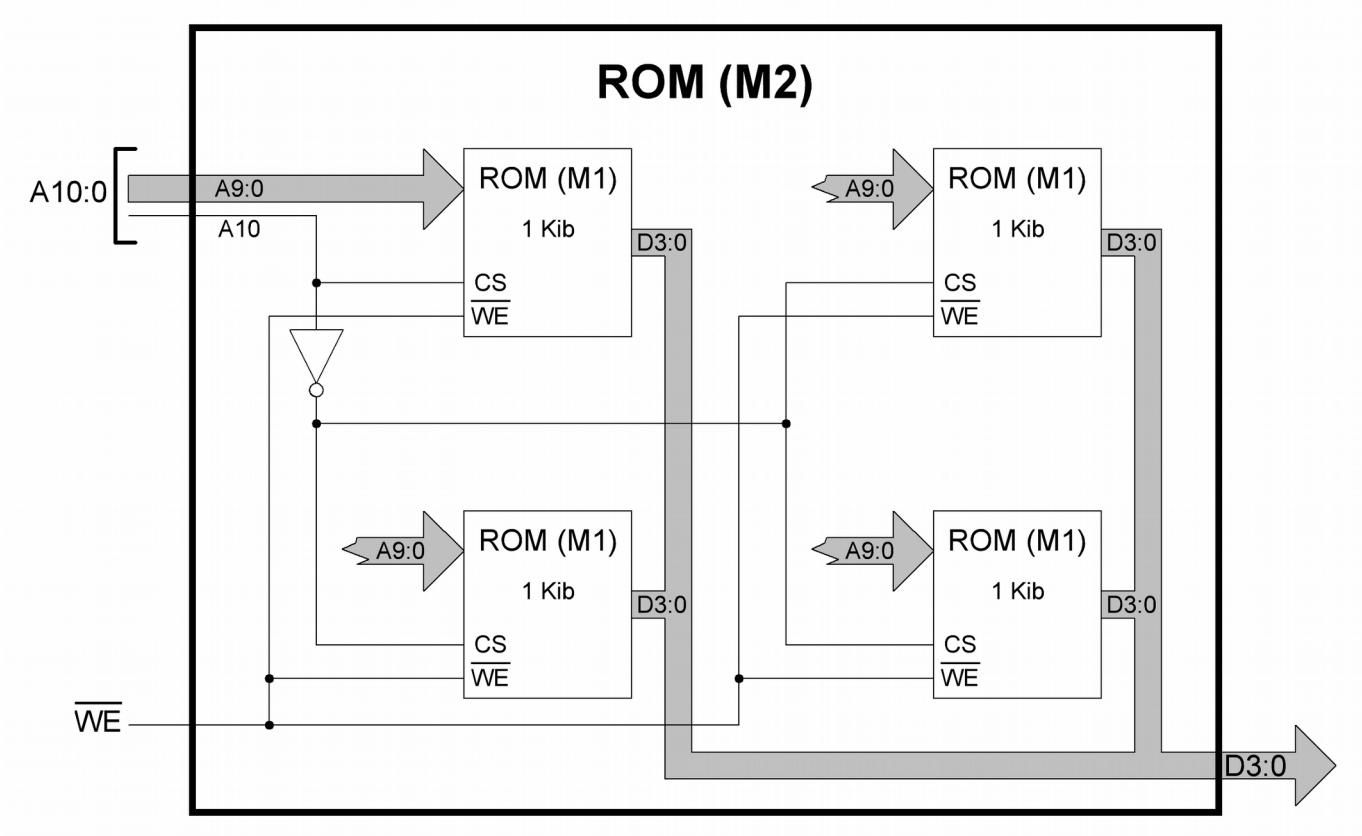
6. Which memory devices **M1** are selected for each of the following addresses: $95A_{16}$, $E03_{16}$, $1FF_{16}$, 725_{16}.

   For each address, we have to find the values of *A11* and *A10*.

   - $95A_{16}$: *A11* = 1, *A10* = 0: the memory devices **M1** number 9, 10, 11 and 12 are selected.
   - $E03_{16}$: *A11* = 1, *A10* = 1: the memory devices **M1** number 13, 14, 15 and 16 are selected
   - $1FF_{16}$: *A11* = 0, *A10* = 0: the memory devices **M1** number 1, 2, 3 and 4 are selected.
   - 725_{16} : *A11* = 0, *A10* = 1: the memory devices **M1** number 5, 6, 7 and 8 are selected.

Exercise 4

The memory device below has a few mistakes. Find them and correct them.



Indications :

- The number of memory devices **M1** is right.
- The capacity (in bits) of the memory device **M1** is right.
- The size of the data bus of the memory device **M1** is right.
- Parallel connections are displayed horizontally.
- Series connections are displayed vertically.

From the indications above, we can work out the number of address lines for each memory device:

M1: 1 Kib = (1 Ki / 4) words of 4 bits = 256 words of 4 bits = 2^8 words of 4 bits.
The memory device **M1** has 8 address lines (*A7:0*).

M2: Since two blocks of **M1** are connected in series, **M2** has one more address line than **M1**.
The memory device **M2** has 9 address lines (*A8:0*).

Since two blocks of **M1** are connected in parallel, the data bus of **M2** is twice as wide as the data bus of **M1**. Therefore, the memory device **M2** has an 8-bit data bus (*D7:0*).

There is never an input $\overline{WE}$ (Write Enable) on a ROM device (Read Only Memory).

A demultiplexer should be used to handle the inputs *CS*.

We obtain the following circuit diagram: