Tutorial 6
Address Decoding

Exercise 1

Let us consider *P*, the number of address lines of a microprocessor, and *C*, the number of address lines of the largest device connected to the microprocessor.

1. Write down the total number of devices that can be connected to the microprocessor using the linear-decoding technique in terms of *C* and *P*.
2. Write down the total number of devices that can be connected to the microprocessor using the block-decoding technique in terms of *C* and *P*.

Exercise 2

A microprocessor system includes a ROM device, a RAM device and two peripheral devices (**P1** and **P2**). The capacities of these devices are 8 Mib, 8 Mib, 8 KiB and 4 KiB respectively. The microprocessor has a 24-bit address bus and all the components have an 8-bit data bus. The ROM should be located in the lowest part of the memory space, followed by the RAM, **P1** and **P2**.

1. Calculate the size of the address buses for each device.

To begin with, you should use the linear-decoding technique.

2. Which address lines are required to select the devices? Write down the devices associated with each of these address lines.
3. The *AS* (Address Strobe) output signal of the microprocessor is active when its address bus contains a valid address. Take the signal *AS* into account to obtain an expression for each output of the address decoder.
4. Draw the memory map. The lowest and highest addresses of each device should appear on the map.
5. What is the main drawback of this decoding technique?
6. Which addresses should never appear on the address bus of the microprocessor?
7. Suggest a simple solution to solve this problem.
8. Draw the circuit diagram.

A new peripheral device (P3) should be added. Its capacity is 2 KiB (11 address lines).

9. Can the linear-decoding technique still be used? Give reasons for your views.

The block-decoding technique should be used (P3 should still be added). There should be as few blocks as possible.

10. Which address lines are required to select the devices? Write down the devices associated with each of these address lines.

11. Obtain an expression for each output of the new address decoder.
12. Draw the new memory map. The lowest and highest addresses of each device should appear on the map.
13. Work out the number of redundant images for each device.
14. Using the 24-bit addresses of the microprocessor, find two different ways to select the address $1F2_{16}$ of each device.
15. Modify the circuit diagram.

The 1-MiB RAM device should be replaced by a 4-MiB RAM device.

16. Can the block-decoding technique still be used? Give reasons for your views.

In order to connect the 4-MiB RAM device, a derivative of the block-decoding technique should be used. Keeping the previous memory configuration of 8 blocks of 2 MiB each, you should use 2 blocks for the RAM device. The first block should contain the lower 2 MiB of the RAM device (labelled RAM0) and should be the same as the block used for the previous RAM device. The second block should contain the upper 2 MiB of the RAM device (labelled RAM1) and should be the block located after P3.

17. Draw the new memory map. The lowest and highest addresses of each device should appear on the map.
18. The *CS* input of the RAM device should be active for two blocks. Write down its new expression.
19. Is this new expression of the *CS* sufficient to decode the RAM device properly?
20. Find a solution to solve this problem.

The 1-MiB ROM device should be replaced by an 8-MiB ROM device. In order to connect this ROM device, it is proposed to use a new decoding technique: no empty space should be found between the memory spaces occupied by all the devices. The ROM should be located in the lowest part of the memory space, followed by the RAM (4 MiB), P1, P2 and P3.

21. Draw the new memory map. The lowest and highest addresses of each device should appear on the map.
22. Obtain an expression for each output of the new address decoder.