Key to Midterm Exam S2
Computer Architecture

Duration: 1 hr. 30 min.

Answer on the answer sheet only.
Do not show any calculation unless you are explicitly asked.
Do not use red ink.

Exercise 1 (5 points)

Answer on the answer sheet. Let us consider the following **11-bit** binary number: $\mathbf{10111101010_2}$.

1. Write down its hexadecimal representation.
2. Assuming that it is an unsigned integer, write down its decimal representation.
3. Assuming that it is a signed integer, write down its decimal representation.

4. Write down the 12-bit binary representation of the following signed number: $\mathbf{-94_{10}}$.
5. Write down the 12-bit binary representation of the following signed number: $\mathbf{-2{,}048_{10}}$.

6. Determine the minimum number of bits required to encode the following unsigned number: $\mathbf{2^{17}}$ **?**
7. Determine the minimum number of bits required to encode the following signed number: $\mathbf{2^{17}}$ **?**
8. Determine the minimum number of bits required to encode the following signed number: $\mathbf{-2^{17}}$ **?**

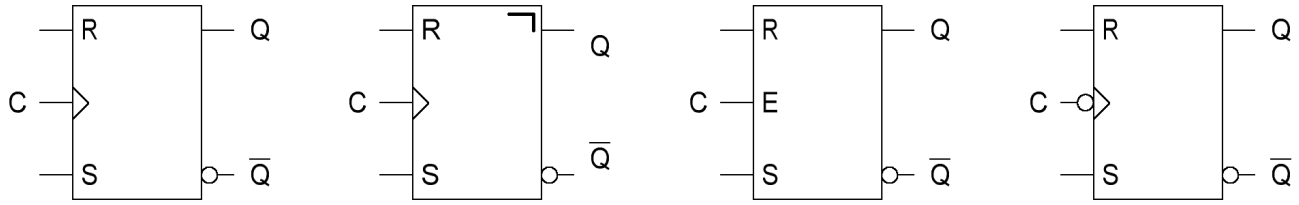
9. How many bytes does the value **2 Kib** contain? Use a power-of-two notation.
10. How many bits does the value **256 KiB** contain? Use binary prefixes (Ki, Mi or Gi) and choose the most appropriate prefix so that the integer numerical value will be as small as possible.

Exercise 2 (7 points)

1. Convert the numbers given on the answer sheet into their **single-precision** IEEE-754 representations. Write down the final result in its **binary form** and specify the three fields.
2. Convert the **double-precision** IEEE-754 words given on the answer sheet into their associated representations. If a representation is a number, use the following form: $k \times 2^n$ where k and n are integers (either positive or negative).

Exercise 3 (4 points)

1. Give the type of each flip-flop below (answer on the answer sheet).



Flip-Flop 1 Flip-Flop 2 Flip-Flop 3 Flip-Flop 4

2. Complete the timing diagrams shown on the answer sheet (up to the last vertical dotted line) for a gated RS latch (*Q0*), a positive-edge-triggered RS flip-flop (*Q1*), a negative-edge-triggered RS flip-flop (*Q2*) and a master-slave RS flip-flop (*Q3*).

Exercise 4 (4 points)

Complete the timing diagrams shown on the answer sheet (up to the last vertical dotted line) for the following circuits.

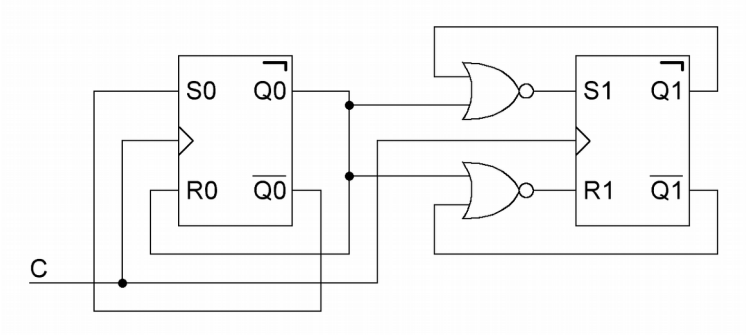


Figure 1

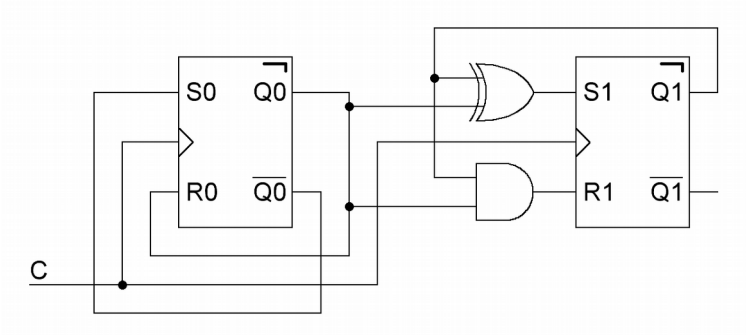


Figure 2

Last name: ..... First name: ..... Group: .....

ANSWER SHEET

Exercise 1

1. $5EA_{16}$	6. 18 bits
2. $1{,}514_{10}$	7. 19 bits
3. -534_{10}	8. 18 bits
4. $1111\ 1010\ 0010_2$	9. 256 bytes
5. $1000\ 0000\ 0000_2$	10. 2 Mib

Exercise 2

1.

Number	S	E	M
43	0	10000100	01011000000000000000000
–203.75	1	10000110	10010111100000000000000
0.171875	0	01111100	01100000000000000000000

2.

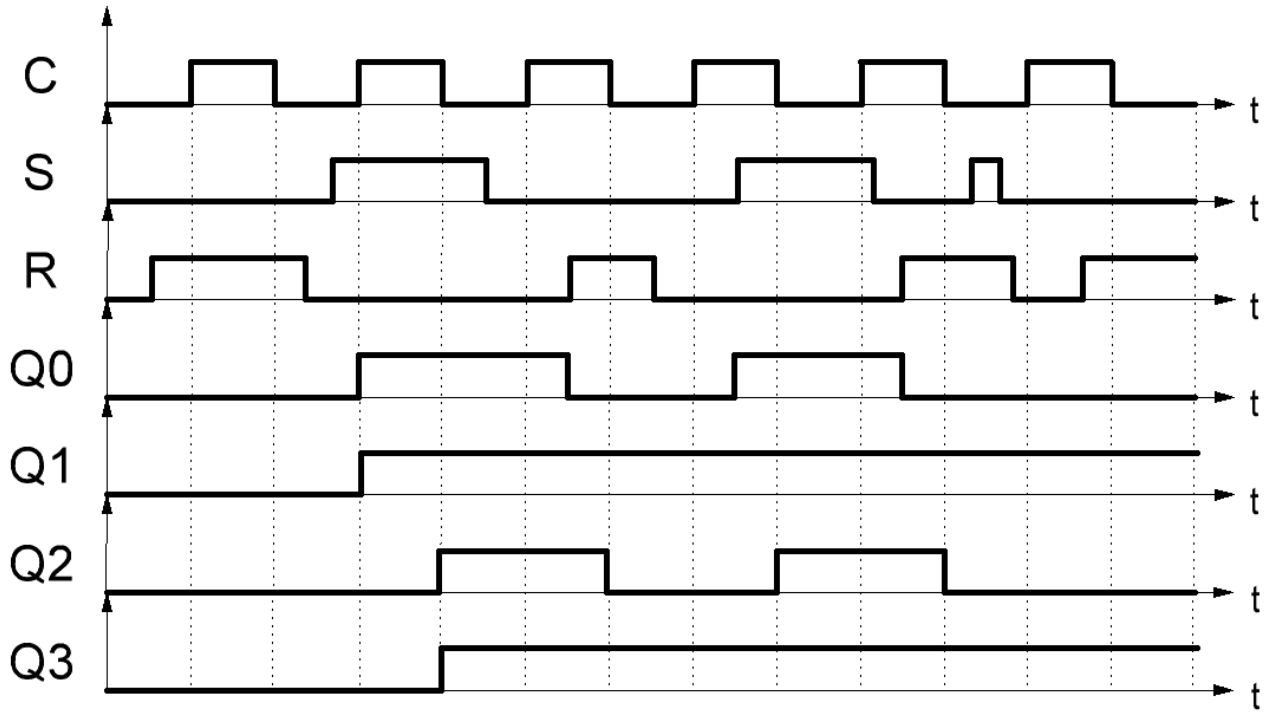
IEEE-754 Representation	Associated Representation
$403D\ 4000\ 0000\ 0000_{16}$	117×2^{-2}
$FFF0\ 0000\ 0000\ 0000_{16}$	$-\infty$
$FFFF\ 0000\ 0000\ 0000_{16}$	NaN
$0002\ 8000\ 0000\ 0000_{16}$	$5 \times 2^{-1{,}027}$

Exercise 3

1.

Flip-Flop	Type of Flip-Flop
1	Positive-edge-triggered RS flip-flop
2	Master-slave RS flip-flop
3	Gated RS latch
4	Negative-edge-triggered RS flip-flop

2.



Exercise 4

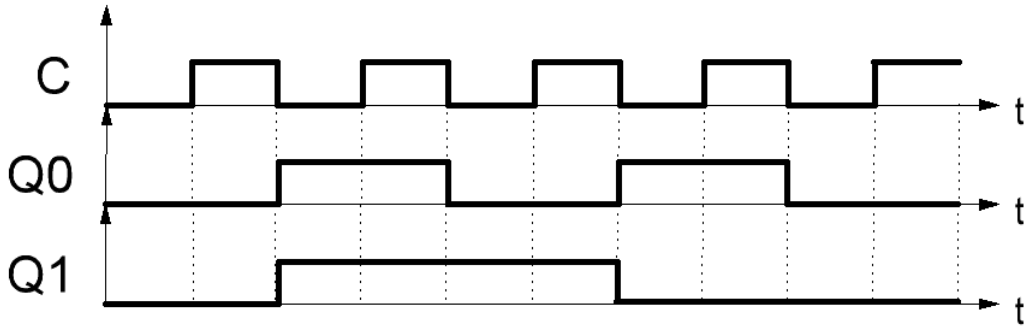


Figure 1

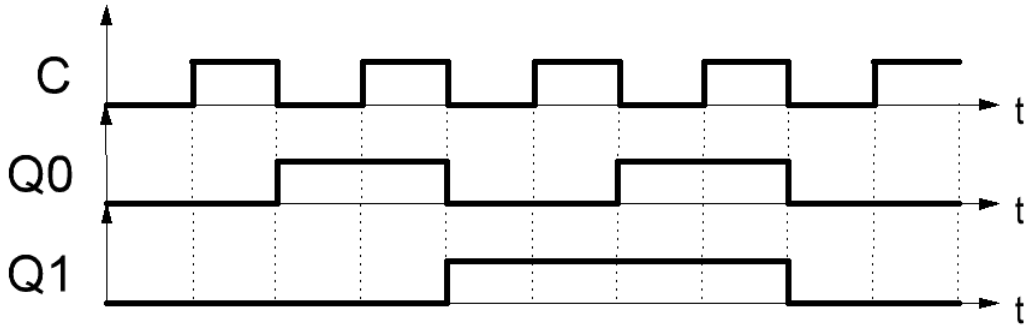


Figure 2

Feel free to use the blank space below if you need to: