

# Final Exam S2

## Computer Architecture

Duration: 1 hr 30 min.

Answer on the answer sheet only.

Do not show any calculation unless you are explicitly asked.

Do not use red ink.

### Exercise 1 (5 points)

1. Convert the numbers given on the [answer sheet](#) into their **single-precision** IEEE-754 representations. Write down the final result in its **binary form** and specify the three fields.
2. Convert the **double-precision** IEEE-754 words given on the [answer sheet](#) into their associated representations. If a representation is a number, use the following base-10 form:  $k \times 2^n$  where  $k$  and  $n$  are integers (either positive or negative).

### Exercise 2 (4 points)

We want to build a 2-Mib ROM device (labelled  $M$ ) from several 16-Kib ROM devices (labelled  $m$ ). The  $M$  device has a 16-bit data bus. The  $m$  devices have a 4-bit data bus. Answer the questions on the [answer sheet](#).

### Exercise 3 (5 points)

1. Wire the flip-flops ([figure 1](#)) in order to design a **modulo-11 asynchronous up counter**.
2. Wire the flip-flops ([figure 2](#)) in order to design a **modulo-11 asynchronous down counter**.
3. Wire the flip-flops ([figure 3](#)) in order to design a **shift register** ( $E \rightarrow Q0 \rightarrow Q1 \rightarrow Q2 \rightarrow Q3$ ).

### Exercise 4 (6 points)

The table shown on the [answer sheet](#) gives the sequence of a counter we want to design. This counter should be made up of JK flip-flops.

1. Complete the table shown on the [answer sheet](#).
2. Write down the most simplified expressions of  $J$  and  $K$  for each flip-flop on the [answer sheet](#). **Complete the Karnaugh maps for the solutions that are not obvious**. An obvious solution does not have any logical operations apart from the complement (for instance:  $J0 = 1$ ,  $K1 = \overline{Q2}$ ).



Last name: ..... First name: ..... Group: .....

**ANSWER SHEET****Exercise 1**

1.

Number	S	E	M
75.75			
0.46875			

2.

IEEE-754 Representation	Associated Representation
20A1 8000 0000 0000 <sub>16</sub>	
7FF7 0000 0000 0000 <sub>16</sub>	
0004 2000 0000 0000 <sub>16</sub>	

**Exercise 2**

Question	Answer
What is the depth of the <i>m</i> memory?	
What is the depth of the <i>M</i> memory?	
What is the number of address lines of the <i>m</i> memory?	
What is the number of address lines of the <i>M</i> memory?	
How many memory devices should be put in parallel?	
How many memory devices should be put in series?	
How many address lines are required to control the CS input of the memory devices?	
When the <i>M</i> memory is active, how many <i>m</i> memory devices are active simultaneously?	

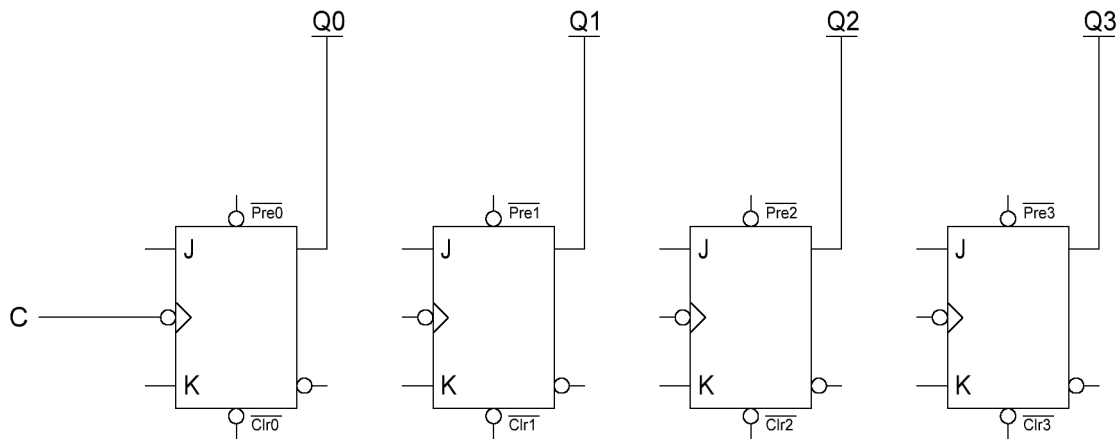
**Exercise 3**

Figure 1

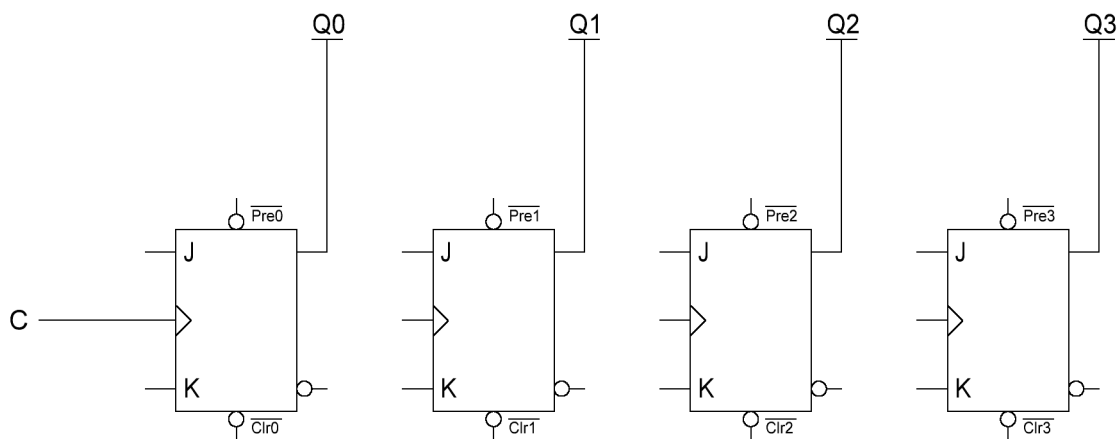


Figure 2

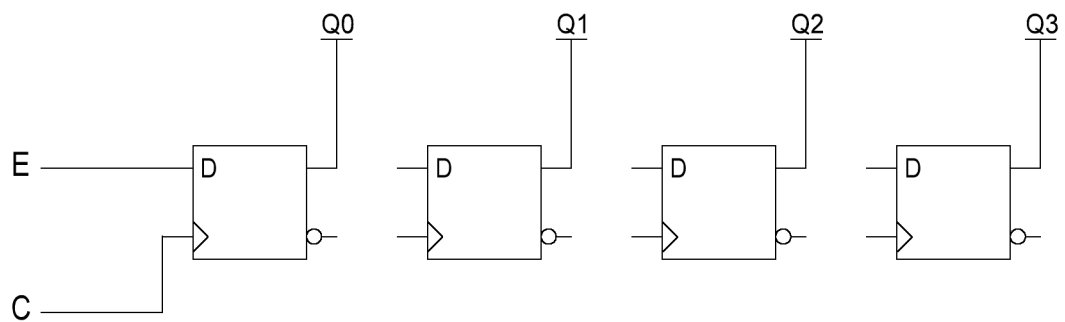


Figure 3

**Exercise 4**

Q2	Q1	Q0	J2	K2	J1	K1	J0	K0
0	0	0						
0	0	1						
0	1	1						
0	1	0						
1	1	0						
1	1	1						
1	0	1						
1	0	0						

**Do not use Karnaugh maps for obvious solutions.**

		Q1 Q0				
		J0	00	01	11	10
Q2	0					
	1					

**J0 =**

		Q1 Q0				
		K0	00	01	11	10
Q2	0					
	1					

**K0 =**

		Q1 Q0				
		J1	00	01	11	10
Q2	0					
	1					

**J1 =**

		Q1 Q0				
		K1	00	01	11	10
Q2	0					
	1					

**K1 =**

		Q1 Q0				
		J2	00	01	11	10
Q2	0					
	1					

**J2 =**

		Q1 Q0				
		K2	00	01	11	10
Q2	0					
	1					

**K2 =**

Feel free to use the blank space below if you need to: