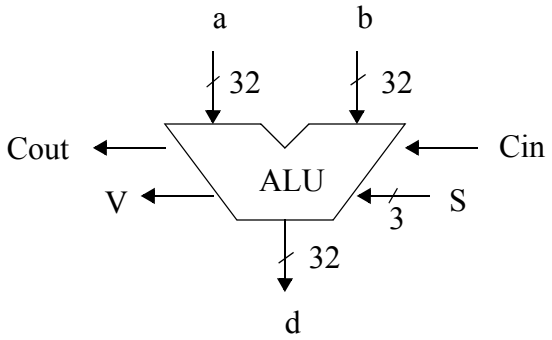
ECEN 4243
Spring 2016
Design Project 1

Use the logic synthesizer (e.g., Modelsim) to design a 32-bit ALU with a worst case delay of 20 nsec. The ALU should have the following inputs and outputs.



All busses shall be numbered with 0 as the least significant bit. The inputs and outputs are defined as follows.

a,b are 32 bit input busses
d is the 32 bit output buss
Cin is the carry into bit 0
Cout is the carry out of bit 31
V is the overflow output
S is the 3 bit function select input

The d, Cout and V outputs should implement the correct function according to the following code for the S input.

S	ALU function
000	a xor b
001	a xnor b
010	a + b
011	a - b
100	a or b
101	a nor b
110	a and b
111	X

The ALU function X means that we “don’t care” what the ALU output is for these values of S. You will erroneously generate latches in your ALU if you leave the outputs undefined for these S inputs. Set the outputs to something, e.g. ‘0’; never leave them undefined.

A Verilog testbench file to provide inputs to your design will be provided by your lab instructor. A similar file will be used to grade your design.

You must demonstrate your design to your lab instructor by the end of the lab period on the due date. Be sure that all of your structural Verilog files have been synthesized. Your highest level Verilog file should be named alu32.v to be compatible with the testbench file.