Floating-Point accumulator

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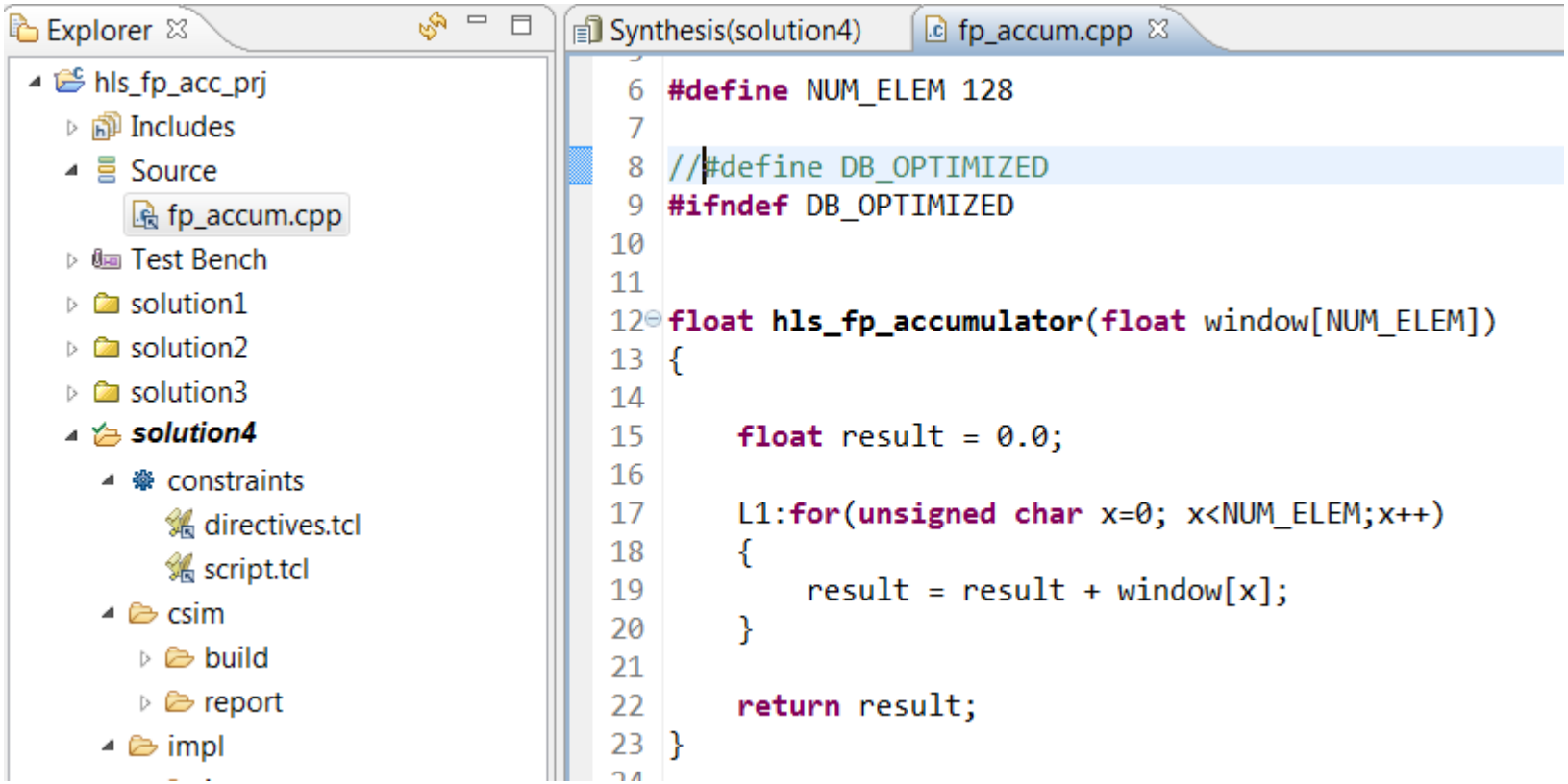
July, 2015

FP Accumulator: the original code 1/2

- The original code is the worst from HLS point of view: purely sequential and with a **feedback**
  - UNROLL will never work here



FP Accumulator: the original code 2/2

- The latency of the core prevents any parallelism

Vivado HLS - hls_fp_acc_prj (C:\BagniD\seminar\HLSjul15\3_FP_accum\hls_fp_acc_prj)

File Edit Project Solution Window Help

Module Hierarchy

	BRAM	DSP	FF	LUT	Latency	Interval	Pipeline type
hls_fp_accumulator	0	2	492	308	1539	1540	none

Performance Profile | Resource Profile

	Pipelined	Latency	Initiation Interval	Iteration Latency	Trip count
hls_fp_accumulator	-	1539	1540	-	-
L1	yes	1537	12	14	128

Debug Synthesis

Synthesis(solution4) | fp_accum.cpp | compare reports | directives.tcl | directives.tcl | Performance(solution2)

Current Module : hls_fp_accumulator

	Operation\Control S...	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14
1	L1														
2	result(phi mux)														
3	x(phi mux)														
4	exitcond(icmp)														
5	x_1(+)														
6	window_load(read)														
7	result_1(fadd)														

Synthesis Estimations comparison 1/2

Explorer

- hls_fp_acc_prj
  - Includes
  - Source
  - Test Bench
  - solution1
  - solution2
  - solution3
  - **solution4**
    - constraints
    - csim
    - impl
    - sim
    - syn

compare reports

Vivado HLS Report Comparison

All Compared Solutions

solution1: xc7k325tffg900-2

solution2: xc7k325tffg900-2

solution3: xc7k325tffg900-2

solution4: xc7k325tffg900-2

Performance Estimates

Timing (ns)

Clock		solution1	solution2	solution3	solution4
ap_clk	Target	2.50	2.50	2.50	2.50
	Estimated	2.10	2.10	2.74	3.38

Latency (clock cycles)

		solution1	solution2	solution3	solution4
Latency	min	1793	1539	356	245
	max	1793	1539	356	245
Interval	min	1794	1540	357	64
	max	1794	1540	357	64

Utilization Estimates

	solution1	solution2	solution3	solution4
BRAM_18K	0	0	4	0
DSP48E	2	2	2	4
FF	489	492	1511	4632
LUT	304	308	1451	2369

Synthesis Estimates Comparison: 2/2

- **(original code) Solution1: baseline**
- **(original code) Solution2:**
  - set_directive_pipeline "hls_fp_accumulator/L1“
- **(optimized code) Solution3: baseline**
- **(optimized code) Solution4: all inner loop are pipelined plus**
  - set_directive_pipeline "hls_fp_accumulator“

CoSimulation report

Explorer

- hls_fp_acc_prj
  - Includes
  - Source
  - Test Bench
  - solution1
  - solution2
  - solution3
  - ***solution4***
    - constraints
      - directives.tcl
      - script.tcl
    - csim
    - impl
    - sim
      - autowrap
      - report
        - hls_fp_accumulator_cosi
        - verilog
      - tv
      - verilog
      - wrapc
      - wrapc_pc
    - syn

Simulation(solution4)

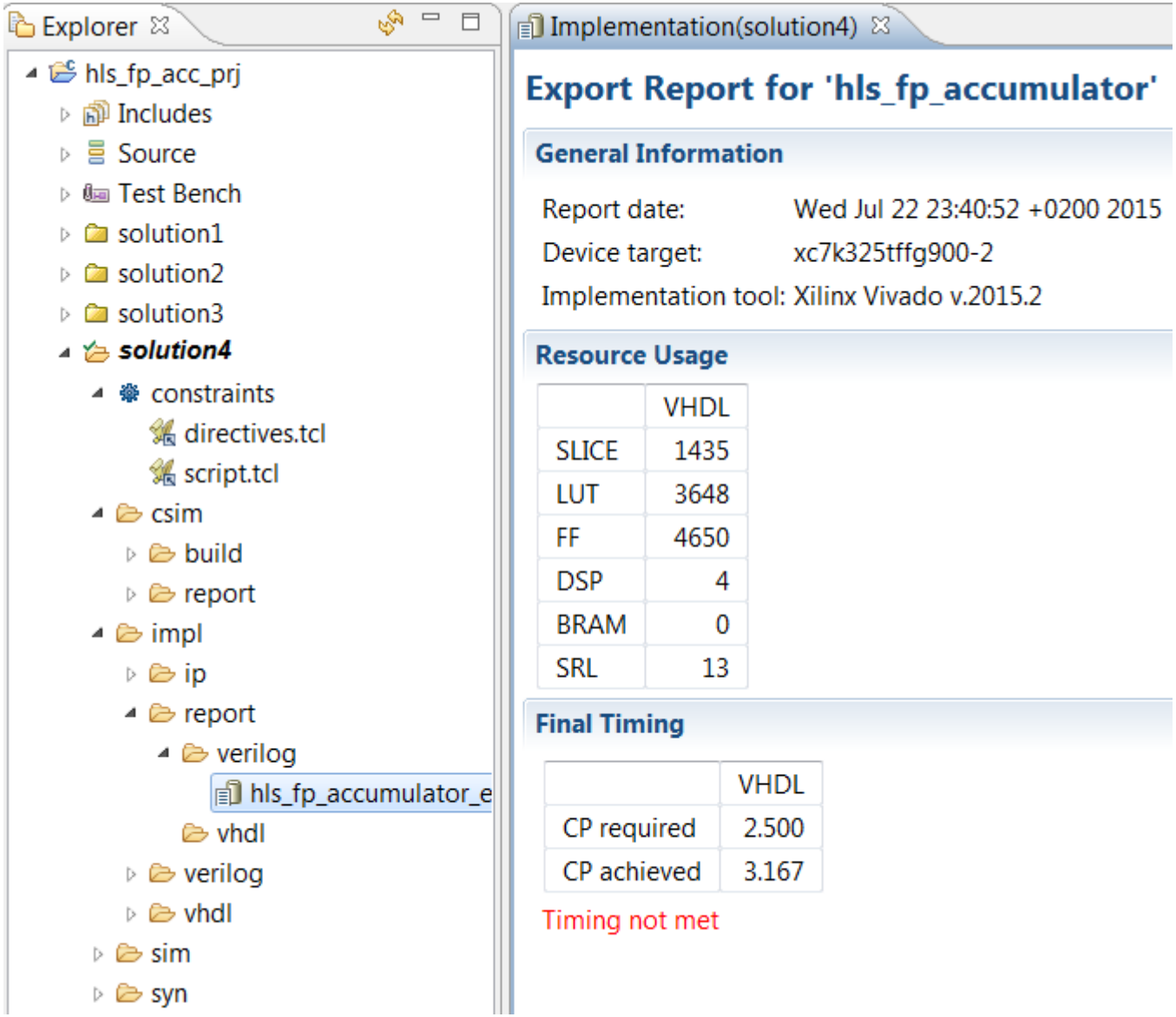
Cosimulation Report for 'hls_fp_accumulator'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	245	245	245	64	64	64

Export the report(.html) using the Export Wizard

Implementation report



Agenda

- 1) FIR filter case: 1 channel, in fractional fixed-point precision
  - ARRAY_PARTITION, ALLOCATION, PIPELINE, UNROLL
  - LATENCY, LOOP TRIP_COUNT
- 2) FIR filter case: 1 channel, in Floating-Point
  - RESOURCE
- **3) Floating-Point Accumulator**
- 4) Dependency
- 5) image Histogram computation and equalization
- 6) Siemens' application "Gamma LUT" case study
- 7) Image Processing: from HLS to IPI, from IPI to ZC702 board
- 8) cordic arctan2
- 9) cordic sqrt