POLITECNICO DI MILANO

Target Customization and Tool Integration

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Outline

- Target Selection
- Integration with Simulator and Synthesis tools

Target Selection

- Target = FPGA device(+synthesis tool) + clock period
  - Different delays of FPGA elements (i.e., delay of a DSP)
  - Different sizes of FPGA elements (i.e., size of LUTs)
  - Different HDL description of memory elements
- Target device + target clock period can be specified
  - Default is
    - Target device: xc7z020-1clg484-VVD
    - Target clock period: **10ns**

Target Information

- Target information is embedded in XML files
  - Supported devices → included in bambu executable
  - New devices → must be passed to the tool
- XML file mainly contains characterization of functional units
  - Area
  - Delay
- XML files are automatically generated by means of eucalyptus (distributed in PandA)
  - New devices can be easily added

Currently supported devices

- Intel
  - Cyclone II: EP2C70F896C6, EP2C70F896C6-R
  - Cyclone V: 5CSEMA5F31C6
  - Stratix IV: EP4SGX530KH40C2
  - Stratix V: 5SGXEA7N2F45C1
- Lattice
  - ECP3: LFE335EA8FN484C
- Xilinx
  - Virtex 4: xc4vlx100-10ff1513
  - Virtex 5: xc5vlx110t-1ff1136 xc5vlx330t-2ff1738 xc5vlx50-3ff1153
  - Virtex 6: xc6vlx240t-1ff1156
  - Artix 7: xc7a100t-1csg324-VVD
  - Virtex 7: xc7vx330t-1ffg1157 xc7vx485t-2ffg1761-VVD xc7vx690t-3ffg1930-VVD
  - Zynq: xc7z020-1clg484-VVD (default), xc7z020-1clg484, xc7z020-1clg484-YOSYS-VVD

Command line options


```
--device-name=<value>
```

Specify the name of the device (see previous slide)

Default is xc7z020-1clg484 (Xilinx Zynq)

```
--clock-period=<value>
```

Specify the period of the clock signal (in nanoseconds)

Default is 10

Example:

```
--device-name=5SGXEA7N2F45C1 --clock-period=5
```

Interfacing Synthesis Tools

- Bambu can directly interface synthesis tools:
  - Quartus / Quartus Prime
  - ISE
  - Vivado
  - Diamond
- Bambu
  - generates synthesis scripts
  - collects information about generated solutions

```
--evaluation
```

Interfacing Synthesis Tools

- User can provide
  - VHDL/Verilog implementation of custom module
  - Constraint files
- Customization of design flow
  - User can provide XML files containing custom TCL scripts

Interfacing Simulation Tools

- Bambu can directly interface simulation tools
- Support to single tools must be enabled during configuration
  - isim
  - xsim
  - modelsim
  - icarus
  - verilator (enabled in VM)
- Bambu can
  - generate testbench + simulation scripts
  - collect data

Testbench Generation

- Testbench is automatically generated in Verilog by bambu starting from:
  - Randomly generated values
  - XML file `--generate-tb=<file.xml>`
  - command line option `--generate-tb=<values>`
  - Annotated C file
    - Support to `open`, `read`, `write` of files
- Result of the simulation is compared with
  - C input or
  - C generated from bambu IR
- Maximum allowed ULP can be set