

Atan2() case study with Vivado HLS



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ver. 7
28 Apr. 2015

atan2_cordic code: 1/3

```
void cordic_atan2( fix_coord_t y0, fix_coord_t x0, fix_phase_t *zn)
{
    fix_coord_t x, y, xp, yp; fix_phase_t z, zp; bool dneg; unsigned char i, quadrant = 0;
    static const fix_phase_t atan_2Mi[] = {45.0, 26.56, 14.03, 7.12, 3.57, 1.78, 0.89, 0.44};
    if (x0 < 0) x = -x0; else x = x0; if (y0 < 0) y = -y0; else y = y0; z=0;
    if (y0==0) { // SPECIAL CASE Y==0
        if (x0<0) *zn = 180; else *zn = 0; return;
    }
    if (x0==0) { // SPECIAL CASE X==0
        if (y0<0) *zn = -90; else *zn = 90; return;
    }
    if ((x0>0) & (y0>0)) quadrant = 1; else if ((x0<0) & (y0>0)) quadrant = 2;
    else if ((x0<0) & (y0<0)) quadrant = 3; else if ((x0>0) & (y0<0)) quadrant = 4;
    LOOP1:for (i=0;i<=ROT;i++) {
        dneg= (y>0);
        if (dneg) { xp = x+(y>>i); yp = y-(x>>i); zp = z + atan_2Mi[i];}
        else { xp = x - (y>>i); yp = y + (x>>i); zp = z - atan_2Mi[i]; }
        x = xp; y = yp; z = zp;
    }
    if (quadrant==1) *zn = z; else if (quadrant==2) *zn = 180 - z;
    else if (quadrant==3) *zn = z - 180; else if (quadrant==4) *zn = -z;
}
```

atan2_cordic code: 2/3

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
default	5.00	4.36	0.63

Latency (clock cycles)

Summary

Latency		Interval		Type
min	max	min	max	
12	12	1	1	function

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
Expression	-	-	0	1446
FIFO	-	-	-	-
Instance	-	-	-	-
Memory	-	-	-	-
Multiplexer	-	-	-	16
Register	-	-	582	14
Total	0	0	582	1476
Available	280	220	106400	53200
Utilization (%)	0	0	~0	2

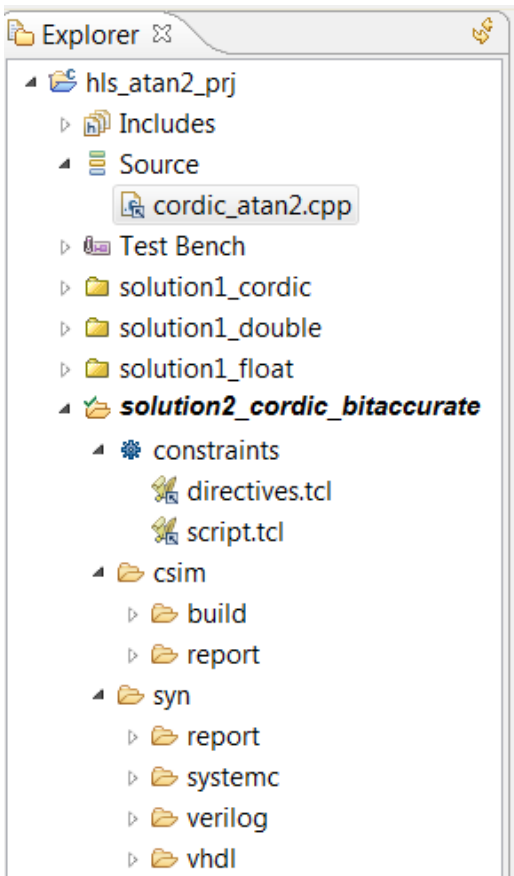
➤ atan2_cordic HLS synthesis performance estimate:

- Fully pipelined core delivering one output every clock cycle
- Fractional fixed point data types:
 - 18 bits for coordinates with 9-bit for integer values
 - 16 bits for phases (angles in radians) with 4-bit for integer values

atan2_cordic code: 3/3 (cordic.h)

```
#if defined(DB_DOUBLE_PRECISION)
    typedef double coord_t;
    typedef double phase_t;
    typedef unsigned char    uint6_t;
#elif defined(DB_SINGLE_PRECISION)
    typedef float coord_t;
    typedef float phase_t;
    typedef unsigned char    uint6_t;
#elif defined(DB_CORDIC)
    #include <ap_int.h>
    #include <ap_fixed.h>
    typedef ap_fixed<18,9> coord_t;
    typedef ap_fixed<16,4> phase_t;
    typedef ap_uint<6> uint6_t;
#else
#error <UNDEFINED ATAN2 METHOD!>
#endif
```

Synthesis Estimates comparison



Performance Estimates

Timing (ns)

Clock		solution1_double	solution1_float	solution1_cordic	solution2_cordic_bitaccurate
ap_clk	Target	2.50	2.50	2.50	2.50
	Estimated	3.52	2.91	6.64	4.50

Latency (clock cycles)

		solution1_double	solution1_float	solution1_cordic	solution2_cordic_bitaccurate
Latency	min	4	4	3	3
	max	353	205	298	20
Interval	min	5	5	4	4
	max	354	206	299	21

Utilization Estimates

	solution1_double	solution1_float	solution1_cordic	solution2_cordic_bitaccurate
BRAM_18K	4	4	0	0
DSP48E	6	6	0	0
FF	18631	6623	6060	250
LUT	13506	5492	6227	646

Place And Route results

The screenshot displays the Xilinx Vivado IDE interface. On the left, a project tree for 'hls_atan2_prj' is shown, including folders for 'Includes', 'Source' (containing 'cordic_atan2.cpp'), 'Test Bench' (containing 'cordic_test.cpp' and a 'test_data' folder with 'check_res.m', 'input_data.txt', 'ref_results.txt', and 'vector.dat'), and three solution folders: 'solution1_cordic', 'solution1_double', 'solution1_float', and 'solution2_cordic_bitaccurate' (which is selected and contains 'constraints', 'csim', 'impl' (with 'ip'), and 'report' (with 'verilog')). On the right, the 'Export Report for 'top_atan2'' is displayed, featuring sections for 'General Information', 'Resource Usage', and 'Final Timing'.

Export Report for 'top_atan2'

General Information

Report date: Fri Jul 24 16:27:41 +0200 2015
Device target: xc7z045ffg900-2
Implementation tool: Xilinx Vivado v.2015.2

Resource Usage

	Verilog
SLICE	161
LUT	508
FF	256
DSP	0
BRAM	0
SRL	0

Final Timing

	Verilog
CP required	2.500
CP achieved	3.266