Lab Report

Created By: Bab

Introduction

The goal of this lab will be to create a baseline design that interfaces with some external interfaces and provide a baseline design for the remainder of the course. We will be making use of the Buttons, Switches, and LEDs on the FPGA development boards.

Equipment Used

Xilinix board (Nexys A7)

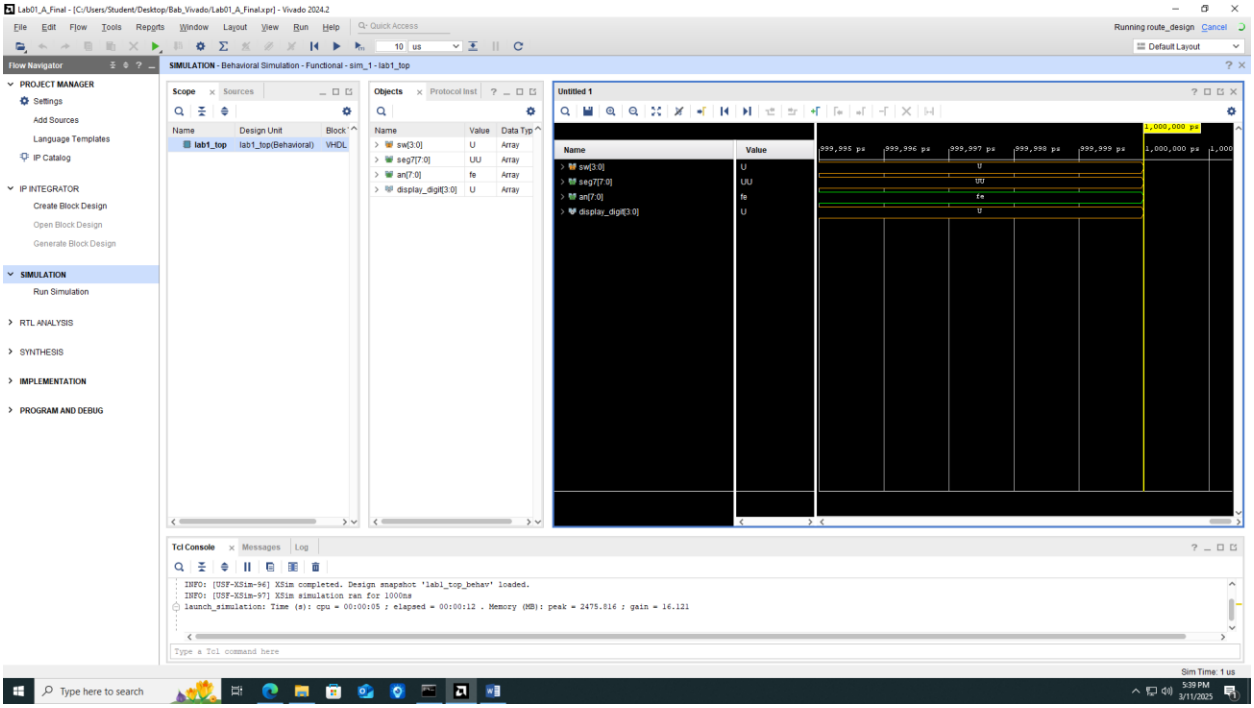
Procedure

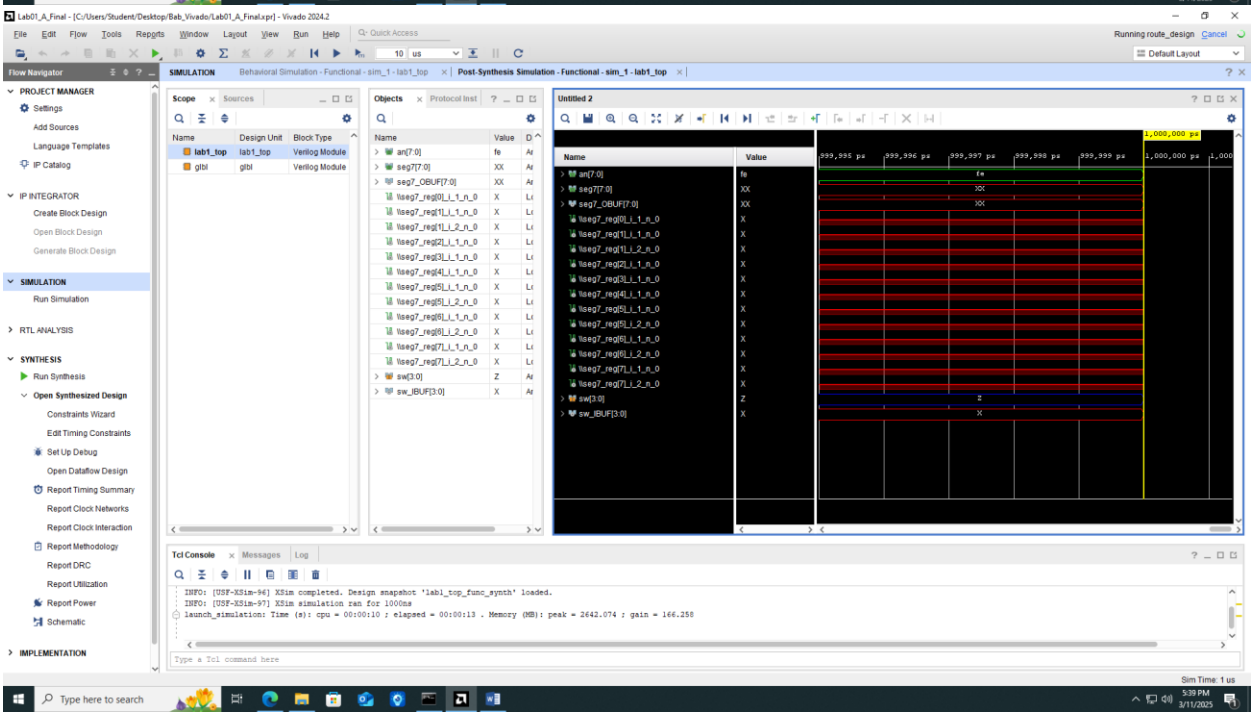
1) Downloading Vivado
2) Downloading diligent Board files
3) Creating a Vivado Project
4) Adding VHDL
5) Assigning pins
6) Vivado Design Flow
    a. Run Synthesis
    b. Run Implementation
    c. Generate Bitatream

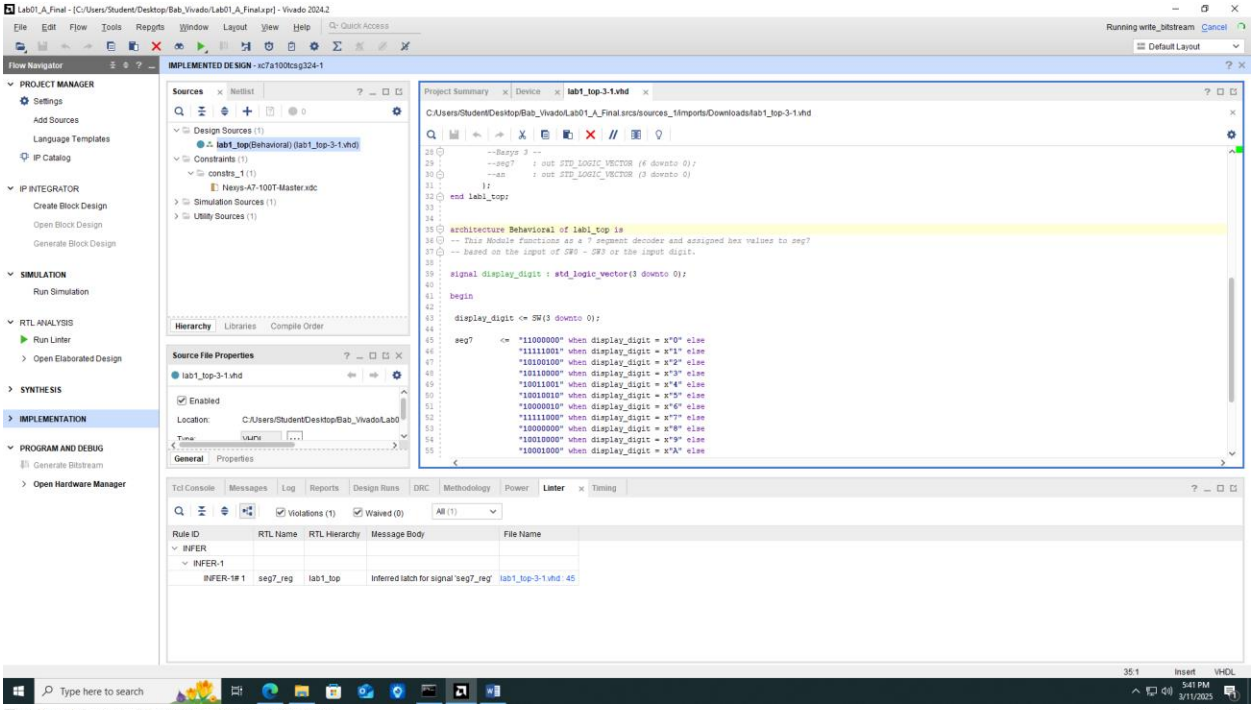
7) Programing FPGA
8) Hardware Board Setup (Xilinix) and programing the device

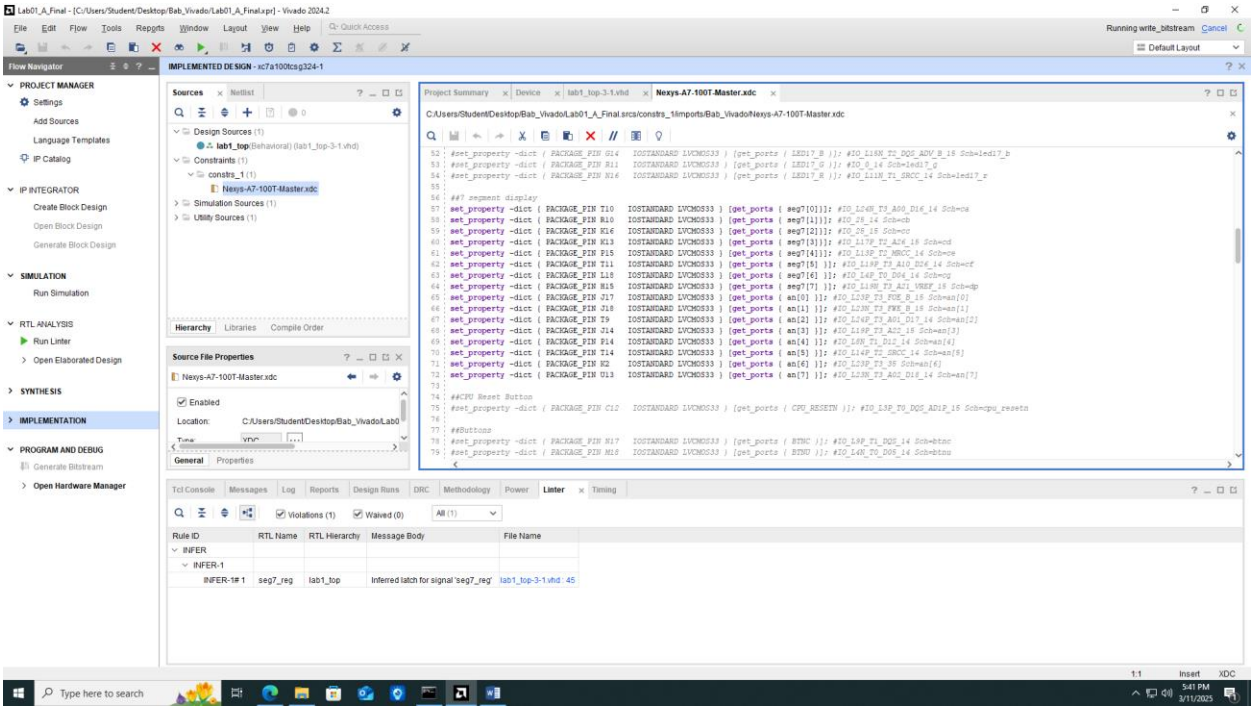
Results

Here the results of the lab. Including the graphs or pictures or the like depicting or showcasing Lab's results.


Lab01_A_Final - [C:/Users/Student/Desktop/Bab_Vivado/Lab01_A_Final.xpr] - Vivado 2024.2
File Edit Flow Tools Reports Window Layout View Run Help
Quick Access
Running route_design Cancel
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
SYNTHESIS
IMPLEMENTATION
PROGRAM AND DEBUG
SIMULATION - Behavioral Simulation - Functional - sim_1 - lab1_top
Scope
Sources
Name
Design Unit
Block
lab1_top
lab1_top(Behavioral)
VHDL
Objects
Protocol Inst
Name
Value
Data Typ
sw[3:0]
U
Array
seg7[7:0]
UU
Array
an[7:0]
fe
Array
display_digit[3:0]
U
Array
Untitled 1
Name
Value
999,995 ps
999,996 ps
999,997 ps
999,998 ps
999,999 ps
1,000,000 ps
Tcl Console
Messages
Log
INFO: [USF-XSim-96] XSim completed. Design snapshot 'lab1_top_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:05 ; elapsed = 00:00:12 . Memory (MB): peak = 2475.816 ; gain = 16.121
Type a Tcl command here
Sim Time: 1 us
Type here to search
5:39 PM
3/11/2025


Lab01_A_Final - [C:/Users/Student/Desktop/Bab_Vivado/Lab01_A_Final.xpr] - Vivado 2024.2
File Edit Flow Tools Reports Window Layout View Run Help
Quick Access
Running route_design Cancel
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
SYNTHESIS
Run Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
Open Dataflow Design
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Utilization
Report Power
Schematic
IMPLEMENTATION
SIMULATION
Behavioral Simulation - Functional - sim_1 - lab1_top
Post-Synthesis Simulation - Functional - sim_1 - lab1_top
Scope
Sources
Name
Design Unit
Block Type
lab1_top
lab1_top
Verilog Module
glbl
glbl
Verilog Module
Objects
Protocol Inst
Name
Value
an[7:0]
fe
seg7[7:0]
XX
seg7_OBUF[7:0]
XX
sw[3:0]
Z
sw_IBUF[3:0]
X
Untitled 2
Name
Value
999,995 ps
999,996 ps
999,997 ps
999,998 ps
999,999 ps
1,000,000 ps
Tcl Console
Messages
Log
INFO: [USF-XSim-96] XSim completed. Design snapshot 'lab1_top_func_synth' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:10 ; elapsed = 00:00:13 . Memory (MB): peak = 2642.074 ; gain = 166.258
Type a Tcl command here
Sim Time: 1 us
Type here to search
5:39 PM
3/11/2025


Lab01_A_Final - [C:/Users/Student/Desktop/Bab_Vivado/Lab01_A_Final.xpr] - Vivado 2024.2
File Edit Flow Tools Reports Window Layout View Help
Running write_bitstream Cancel
Default Layout
Flow Navigator
IMPLEMENTED DESIGN - xc7a100tcsg324-1
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
SYNTHESIS
IMPLEMENTATION
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Sources
Netlist
Design Sources (1)
lab1_top(Behavioral) (lab1_top-3-1.vhd)
Constraints (1)
constrs_1 (1)
Nexys-A7-100T-Master.xdc
Simulation Sources (1)
Utility Sources (1)
Hierarchy Libraries Compile Order
Source File Properties
lab1_top-3-1.vhd
Enabled
Location: C:/Users/Student/Desktop/Bab_Vivado/Lab0
General Properties
Project Summary
Device
lab1_top-3-1.vhd
C:/Users/Student/Desktop/Bab_Vivado/Lab01_A_Final.srcs/sources_1/imports/Downloads/lab1_top-3-1.vhd
--Basys 3 --
--seg7 : out STD_LOGIC_VECTOR (6 downto 0);
--an : out STD_LOGIC_VECTOR (3 downto 0)
);
end lab1_top;
architecture Behavioral of lab1_top is
-- This Module functions as a 7 segment decoder and assigned hex values to seg7
-- based on the input of SW0 - SW3 or the input digit.
signal display_digit : std_logic_vector(3 downto 0);
begin
display_digit <= SW(3 downto 0);
seg7 <= "11000000" when display_digit = x"0" else
"11111001" when display_digit = x"1" else
"10100100" when display_digit = x"2" else
"10110000" when display_digit = x"3" else
"10011001" when display_digit = x"4" else
"10010010" when display_digit = x"5" else
"10000010" when display_digit = x"6" else
"11111000" when display_digit = x"7" else
"10000000" when display_digit = x"8" else
"10010000" when display_digit = x"9" else
"10001000" when display_digit = x"A" else
Tcl Console Messages Log Reports Design Runs DRC Methodology Power Linter Timing
Violations (1) Waived (0)
All (1)
Rule ID RTL Name RTL Hierarchy Message Body File Name
INFER
INFER-1
INFER-1# 1 seg7_reg lab1_top Inferred latch for signal 'seg7_reg' lab1_top-3-1.vhd : 45
35:1 Insert VHDL
Type here to search
5:41 PM
3/11/2025


Lab01_A_Final - [C:/Users/Student/Desktop/Bab_Vivado/Lab01_A_Final.xpr] - Vivado 2024.2
File Edit Flow Tools Reports Window Layout View Help
Running write_bitstream Cancel
Default Layout
Flow Navigator
IMPLEMENTED DESIGN - xc7a100tcsg324-1
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
SYNTHESIS
IMPLEMENTATION
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Sources
Netlist
Design Sources (1)
lab1_top(Behavioral) (lab1_top-3-1.vhd)
Constraints (1)
constrs_1 (1)
Nexys-A7-100T-Master.xdc
Simulation Sources (1)
Utility Sources (1)
Hierarchy Libraries Compile Order
Source File Properties
Nexys-A7-100T-Master.xdc
Enabled
Location: C:/Users/Student/Desktop/Bab_Vivado/Lab0
General Properties
Project Summary
Device
lab1_top-3-1.vhd
Nexys-A7-100T-Master.xdc
C:/Users/Student/Desktop/Bab_Vivado/Lab01_A_Final.srcs/constrs_1/imports/Bab_Vivado/Nexys-A7-100T-Master.xdc
#set_property -dict { PACKAGE_PIN G14 IOSTANDARD LVCMOS33 } [get_ports { LED17_B }]; #IO_L18N_T2_DQS_ADV_B_15 Sch=led17_b
#set_property -dict { PACKAGE_PIN R11 IOSTANDARD LVCMOS33 } [get_ports { LED17_G }]; #IO_0_14 Sch=led17_g
#set_property -dict { PACKAGE_PIN N16 IOSTANDARD LVCMOS33 } [get_ports { LED17_R }]; #IO_L11N_T1_SRCC_14 Sch=led17_r
##7 segment display
set_property -dict { PACKAGE_PIN T10 IOSTANDARD LVCMOS33 } [get_ports { seg7[0] }]; #IO_L24N_T3_A00_D16_14 Sch=ca
set_property -dict { PACKAGE_PIN R10 IOSTANDARD LVCMOS33 } [get_ports { seg7[1] }]; #IO_25_14 Sch=cb
set_property -dict { PACKAGE_PIN K16 IOSTANDARD LVCMOS33 } [get_ports { seg7[2] }]; #IO_25_15 Sch=cc
set_property -dict { PACKAGE_PIN K13 IOSTANDARD LVCMOS33 } [get_ports { seg7[3] }]; #IO_L17P_T2_A24_15 Sch=cd
set_property -dict { PACKAGE_PIN P15 IOSTANDARD LVCMOS33 } [get_ports { seg7[4] }]; #IO_L13P_T2_MRCC_14 Sch=ce
set_property -dict { PACKAGE_PIN T11 IOSTANDARD LVCMOS33 } [get_ports { seg7[5] }]; #IO_L19P_T3_A10_D26_14 Sch=cf
set_property -dict { PACKAGE_PIN L18 IOSTANDARD LVCMOS33 } [get_ports { seg7[6] }]; #IO_L4P_T0_D04_14 Sch=cg
set_property -dict { PACKAGE_PIN H15 IOSTANDARD LVCMOS33 } [get_ports { seg7[7] }]; #IO_L19N_T3_A21_VREF_15 Sch=dp
set_property -dict { PACKAGE_PIN J17 IOSTANDARD LVCMOS33 } [get_ports { an[0] }]; #IO_L23P_T3_FOE_B_15 Sch=an[0]
set_property -dict { PACKAGE_PIN J18 IOSTANDARD LVCMOS33 } [get_ports { an[1] }]; #IO_L23N_T3_FWE_B_15 Sch=an[1]
set_property -dict { PACKAGE_PIN T9 IOSTANDARD LVCMOS33 } [get_ports { an[2] }]; #IO_L24P_T3_A01_D17_14 Sch=an[2]
set_property -dict { PACKAGE_PIN J14 IOSTANDARD LVCMOS33 } [get_ports { an[3] }]; #IO_L19P_T3_A22_15 Sch=an[3]
set_property -dict { PACKAGE_PIN P14 IOSTANDARD LVCMOS33 } [get_ports { an[4] }]; #IO_L8N_T1_D12_14 Sch=an[4]
set_property -dict { PACKAGE_PIN T14 IOSTANDARD LVCMOS33 } [get_ports { an[5] }]; #IO_L14P_T2_SRCC_14 Sch=an[5]
set_property -dict { PACKAGE_PIN K2 IOSTANDARD LVCMOS33 } [get_ports { an[6] }]; #IO_L23P_T3_35 Sch=an[6]
set_property -dict { PACKAGE_PIN U13 IOSTANDARD LVCMOS33 } [get_ports { an[7] }]; #IO_L23N_T3_A02_D18_14 Sch=an[7]
##CPU Reset Button
#set_property -dict { PACKAGE_PIN C12 IOSTANDARD LVCMOS33 } [get_ports { CPU_RESETN }]; #IO_L3P_T0_DQS_AD1P_15 Sch=cpu_resetn
##Buttons
#set_property -dict { PACKAGE_PIN N17 IOSTANDARD LVCMOS33 } [get_ports { BTNC }]; #IO_L9P_T1_DQS_14 Sch=btnc
#set_property -dict { PACKAGE_PIN M18 IOSTANDARD LVCMOS33 } [get_ports { BTNU }]; #IO_L4N_T0_D05_14 Sch=btnu
Tcl Console Messages Log Reports Design Runs DRC Methodology Power Linter Timing
Violations (1) Waived (0)
All (1)
Rule ID RTL Name RTL Hierarchy Message Body File Name
INFER
INFER-1
INFER-1# 1 seg7_reg lab1_top Inferred latch for signal 'seg7_reg' lab1_top-3-1.vhd : 45
1:1 Insert XDC
Type here to search
5:41 PM
3/11/2025


NEXYS A7
DIGILENT
XILINX
ANALOG DEVICES
HOUKEM-2841-0SR
20231123
HOUKEM-2841-0SR
20231123

Conclusion

The Objective of the Lab was met the program was run on hardware as well with the successful out put.