Final Project: FPGA-Based Real-Time Heart Rate Monitoring System

Created By: Bab Jan

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## Introduction

The objective of this project was to design and implement a **real-time heart rate monitoring system** using an FPGA. The system processes signals from a **PPG/ECG heart rate sensor**, filters noise, calculates beats per minute (BPM), and displays the result on a **7-segment display or LED indicators**. The implementation was carried out using **Vivado** with **VHDL** for hardware description and **digital signal processing (DSP) techniques** to extract heart rate data.

This project aligns with FPGA-based **real-time medical applications**, ensuring fast and efficient heart rate detection compared to software-based implementations.

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## Equipment Used

### Hardware:

- Xilinx Nexys A7-100T FPGA Board (Artix-7)
- PPG/ECG Heart Rate Sensor
- 7-Segment Display / LED Indicators
- USB Cable for FPGA Programming

### Software:

- **Xilinx Vivado** (for RTL Design and Bitstream Generation)
- **VHDL** (for FPGA Logic Implementation)
- **Simulation Tools** (for validating digital signal processing algorithms)

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## Procedure

### Step 1: Setting Up Vivado and FPGA Board

1. Download and install **Vivado Design Suite**.
2. Install **Digilent Board Files** to configure the Nexys A7-100T FPGA.
3. Create a new **Vivado Project** and select **Artix-7 (XC7A100TCSG324-1)** as the FPGA device.

## Step 2: Implementing the FPGA Design

1. **Creating and Adding VHDL Files:**
    - **Signal Acquisition Module** (Captures heart rate sensor data)
    - **Digital Filtering Module** (Removes noise from the raw signal)
    - **Heart Rate Calculation Module** (Detects peaks and calculates BPM)
    - **Display Interface Module** (Drives 7-segment display and LEDs)
2. **Vivado Design Flow:**
    - Write **VHDL Code** for each module.
    - Define **top-level entity** to connect all components.
    - Verify **port mapping and signal connections**.

## Step 3: Configuring Constraints File (.xdc)

1. Assign **FPGA pins** for input and output signals.
2. Define **clock constraints** for timing analysis.
3. Ensure **IOSTANDARD LVCMOS33** for proper signal interfacing.

Example of Constraints File:

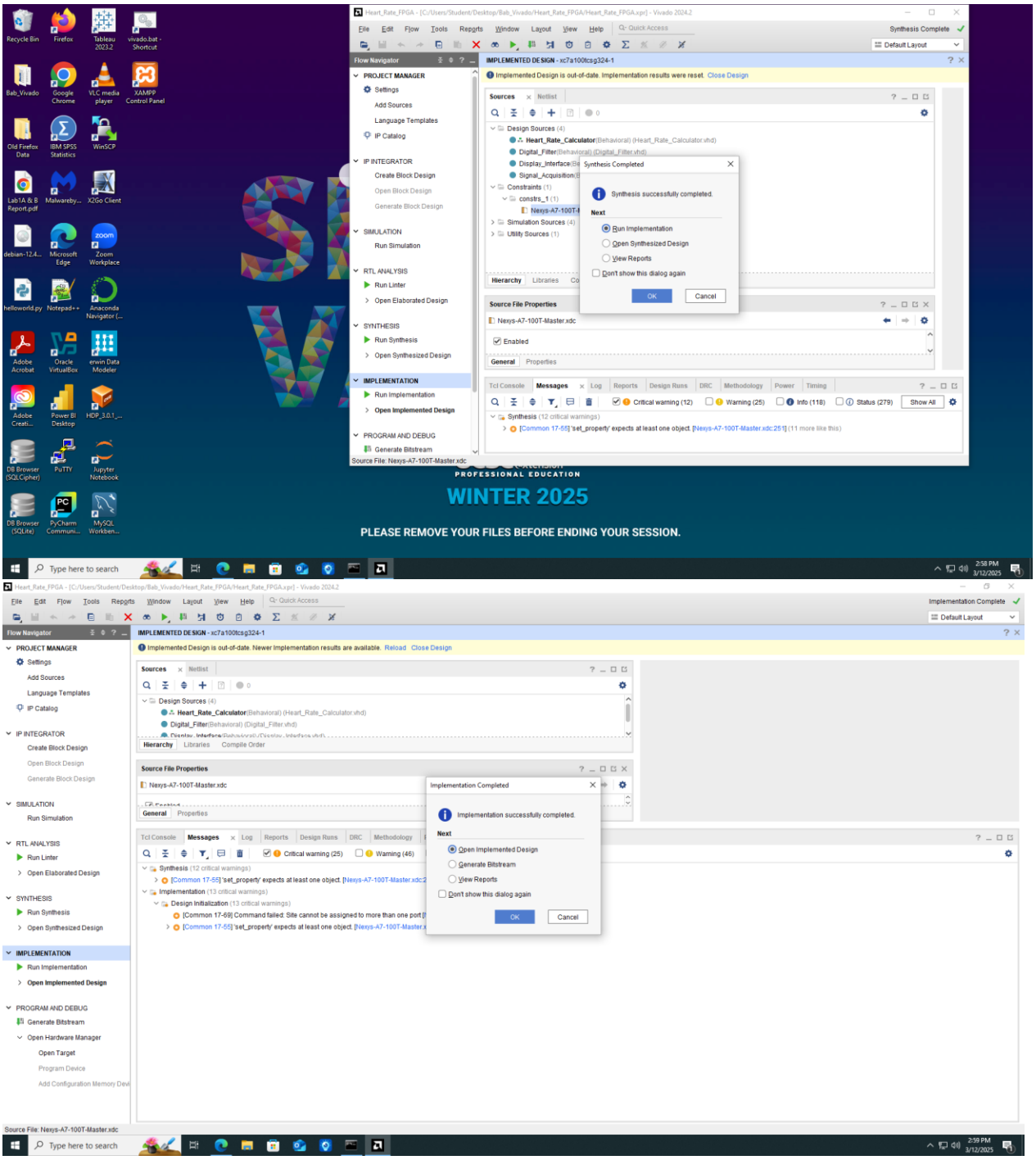
```
## Clock Signal (100 MHz)
set_property PACKAGE_PIN E3 [get_ports clk]
set_property IOSTANDARD LVCMOS33 [get_ports clk]

## Heart Rate Sensor Input
set_property PACKAGE_PIN A1 [get_ports heart_rate]
set_property IOSTANDARD LVCMOS33 [get_ports heart_rate]
```

## Step 4: Synthesis and Implementation

1. **Run Synthesis** to convert VHDL into FPGA logic.
2. **Run Implementation** to optimize design placement.
3. **Generate Bitstream** for FPGA programming.

## Step 5: Programming the FPGA

1. Connect **Nexys A7-100T** board to the PC.
2. Open **Vivado Hardware Manager**.
3. Select **FPGA Device** and **Program with Bitstream (.bit file)**.
4. Observe real-time heart rate output on **LEDs/7-Segment Display**.


Heart_Rate_FPGA - [C:/Users/Student/Desktop/Bab_Vivado/Heart_Rate_FPGA/Heart_Rate_FPGA.xpr] - Vivado 2024.2
Synthesis Complete
IMPLEMENTED DESIGN - xc7a100tcsg324-1
Synthesis Completed
Synthesis successfully completed.
Run Implementation
Open Synthesized Design
View Reports
Don't show this dialog again
OK
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PROFESSIONAL EDUCATION
WINTER 2025
PLEASE REMOVE YOUR FILES BEFORE ENDING YOUR SESSION.
Implementation Completed
Implementation successfully completed.
Open Implemented Design
Generate Bitstream
View Reports
Don't show this dialog again
OK
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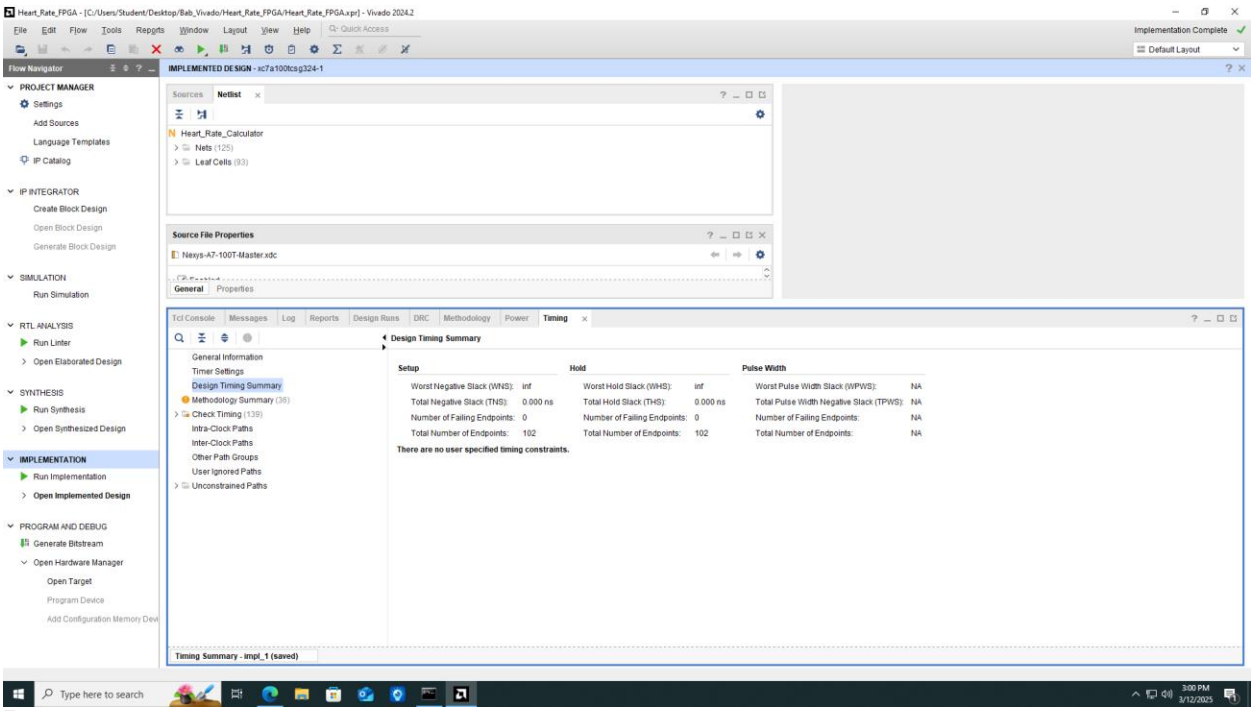
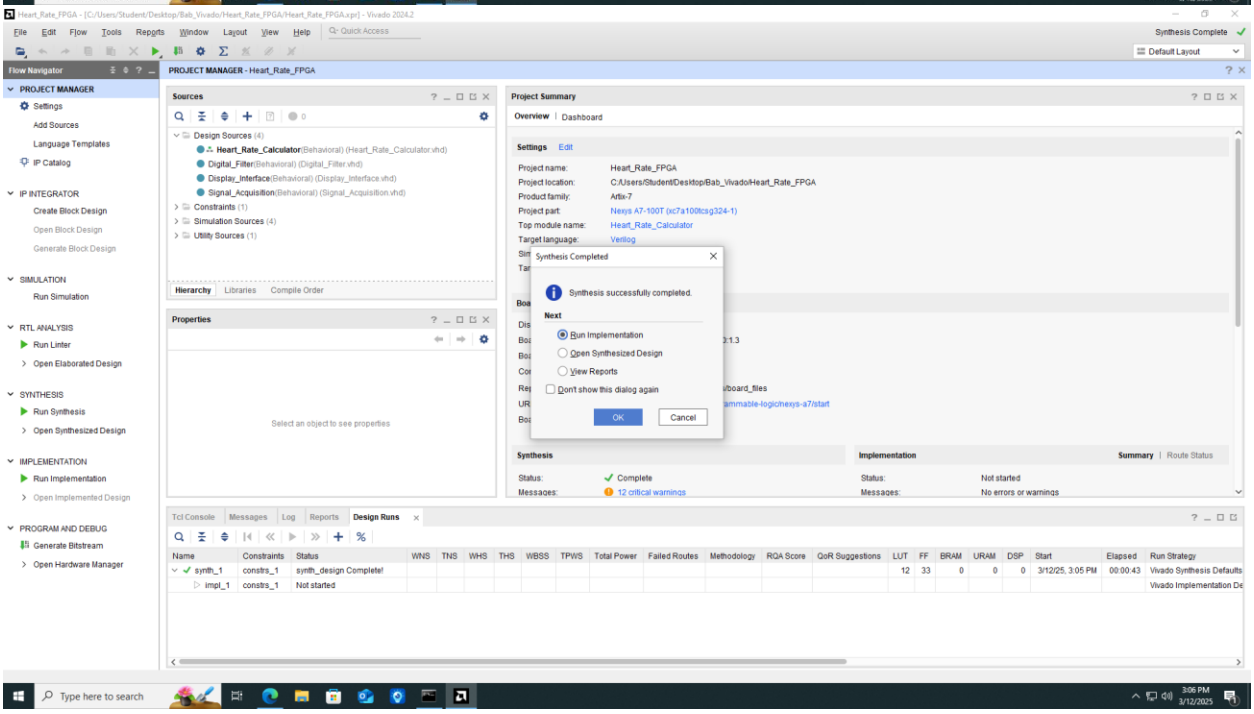

Heart_Rate_FPGA - [C:/Users/Student/Desktop/Bab_Vivado/Heart_Rate_FPGA/Heart_Rate_FPGA.xpr] - Vivado 2024.2
Implementation Complete
IMPLEMENTED DESIGN - xc7a100tcsg324-1
Heart_Rate_Calculator
Nets (125)
Leaf Cells (93)
Nexys-A7-100T-Master.xdc
Design Timing Summary
Setup
Hold
Pulse Width
Worst Negative Slack (WNS): inf
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 102
Worst Hold Slack (WHS): inf
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 102
Worst Pulse Width Slack (WPWS): NA
Total Pulse Width Negative Slack (TPWS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
There are no user specified timing constraints.
Timing Summary - impl_1 (saved)


Heart_Rate_FPGA - [C:/Users/Student/Desktop/Bab_Vivado/Heart_Rate_FPGA/Heart_Rate_FPGA.xpr] - Vivado 2024.2
Synthesis Complete
PROJECT MANAGER - Heart_Rate_FPGA
Design Sources (4)
Heart_Rate_Calculator(Behavioral) (Heart_Rate_Calculator.vhd)
Digital_Filter(Behavioral) (Digital_Filter.vhd)
Display_Interface(Behavioral) (Display_Interface.vhd)
Signal_Acquisition(Behavioral) (Signal_Acquisition.vhd)
Project Summary
Project name: Heart_Rate_FPGA
Project location: C:/Users/Student/Desktop/Bab_Vivado/Heart_Rate_FPGA
Product family: Artix-7
Project part: Nexys A7-100T (xc7a100tcsg324-1)
Top module name: Heart_Rate_Calculator
Target language: Verilog
Synthesis Completed
Synthesis successfully completed.
Next
Run Implementation
Open Synthesized Design
View Reports
Don't show this dialog again
OK
Cancel
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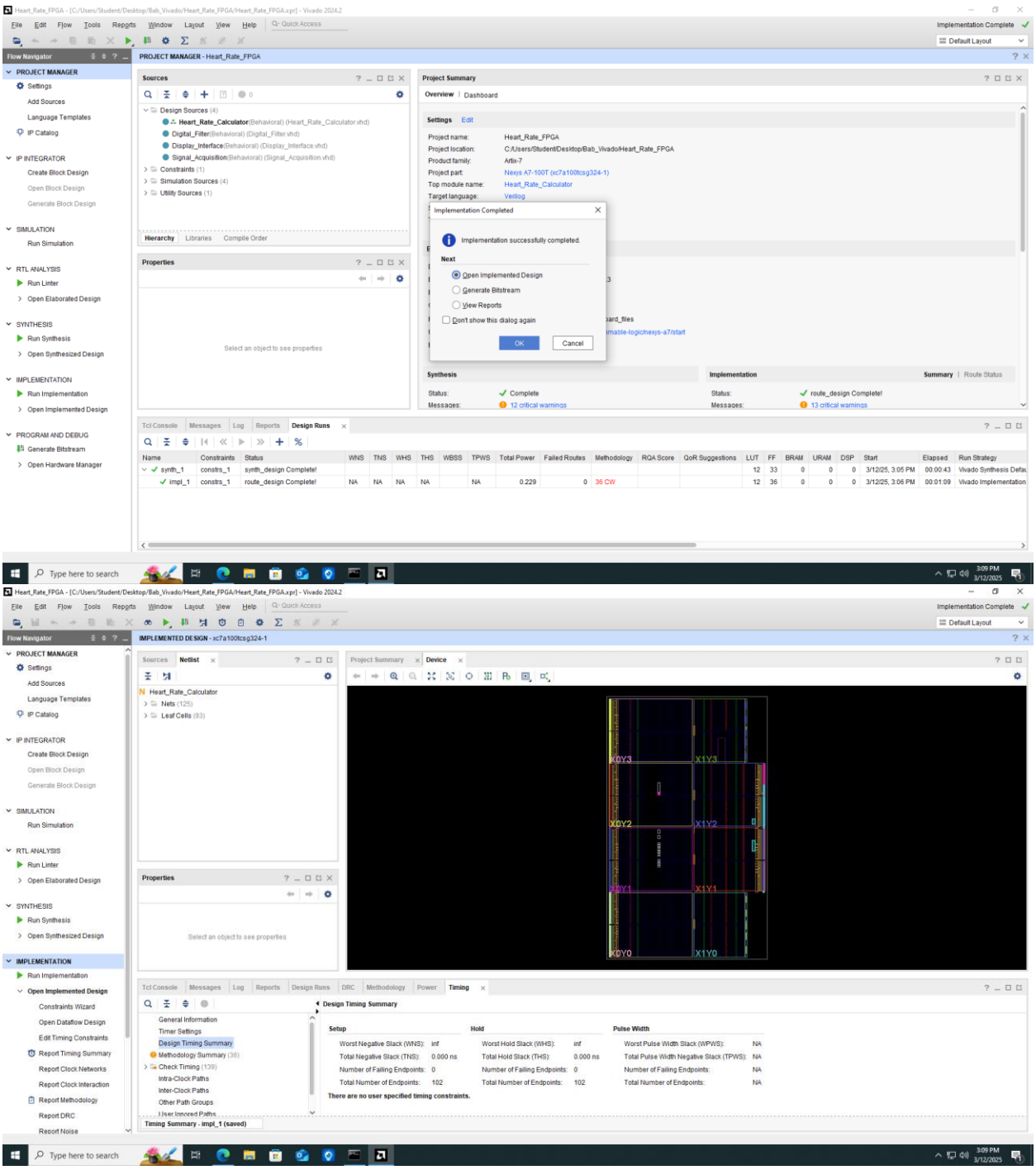
synth_1 | constrs_1 | synth_design Complete! | 12 | 33 | 0 | 0 | 0 | 3/12/25, 3:05 PM | 00:00:43 | Vivado Synthesis Defaults
impl_1 | constrs_1 | Not started | Vivado Implementation De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File Edit Flow Tools Reports Window Layout View Help
Implementation Complete
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PROJECT MANAGER - Heart_Rate_FPGA
PROJECT MANAGER
Settings
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IP INTEGRATOR
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Run Linter
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Run Synthesis
Open Synthesized Design
IMPLEMENTATION
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Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Sources
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Digital_Filter(Behavioral) (Digital_Filter.vhd)
Display_Interface(Behavioral) (Display_Interface.vhd)
Signal_Acquisition(Behavioral) (Signal_Acquisition.vhd)
Constraints (1)
Simulation Sources (4)
Utility Sources (1)
Hierarchy Libraries Compile Order
Properties
Select an object to see properties
Project Summary
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Settings Edit
Project name: Heart_Rate_FPGA
Project location: C:/Users/Student/Desktop/Bab_Vivado/Heart_Rate_FPGA
Product family: Artix-7
Project part: Nexys A7-100T (xc7a100tcsg324-1)
Top module name: Heart_Rate_Calculator
Target language: Verilog
Implementation Completed
Implementation successfully completed.
Next
Open Implemented Design
Generate Bitstream
View Reports
Don't show this dialog again
OK
Cancel
Synthesis
Status: Complete
Messages: 12 critical warnings
Implementation
Summary | Route Status
Status: route_design Complete!
Messages: 13 critical warnings
Tcl Console Messages Log Reports Design Runs
Name Constraints Status WNS TNS WHS THS WBSS TPWS Total Power Failed Routes Methodology QoR Score QoR Suggestions LUT FF BRAM URAM DSP Start Elapsed Run Strategy
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Heart_Rate_FPGA - [C:/Users/Student/Desktop/Bab_Vivado/Heart_Rate_FPGA/Heart_Rate_FPGA.xpr] - Vivado 2024.2
IMPLEMENTED DESIGN - xc7a100tcsg324-1
Sources Netlist
Heart_Rate_Calculator
Nets (125)
Leaf Cells (93)
Project Summary Device
X0Y3 X1Y3
X0Y2 X1Y2
X0Y1 X1Y1
X0Y0 X1Y0
Tcl Console Messages Log Reports Design Runs DRC Methodology Power Timing
Design Timing Summary
General Information
Timer Settings
Design Timing Summary
Methodology Summary (36)
Check Timing (139)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Setup
Worst Negative Slack (WNS): inf
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 102
Hold
Worst Hold Slack (WHS): inf
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 102
Pulse Width
Worst Pulse Width Slack (WPWS): NA
Total Pulse Width Negative Slack (TPWS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
There are no user specified timing constraints.
Timing Summary - impl_1 (saved)
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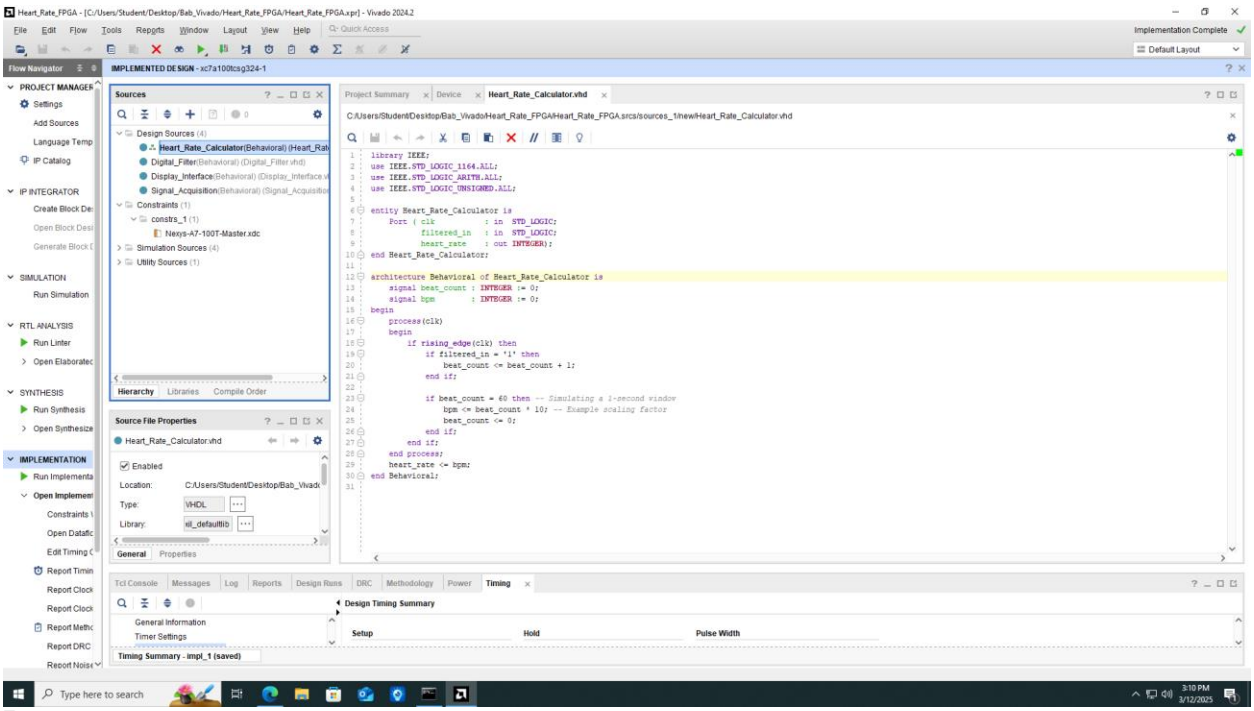
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Simulation Sources (4)
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Hierarchy Libraries Compile Order
Source File Properties
Heart_Rate_Calculator.vhd
Enabled
Location: C:/Users/Student/Desktop/Bab_Vivad
Type: VHDL
Library: xil_defaultlib
General Properties
Project Summary Device Heart_Rate_Calculator.vhd
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity Heart_Rate_Calculator is
Port ( clk : in STD_LOGIC;
filtered_in : in STD_LOGIC;
heart_rate : out INTEGER);
end Heart_Rate_Calculator;
architecture Behavioral of Heart_Rate_Calculator is
signal beat_count : INTEGER := 0;
signal bpm : INTEGER := 0;
begin
process(clk)
begin
if rising_edge(clk) then
if filtered_in = '1' then
beat_count <= beat_count + 1;
end if;
if beat_count = 60 then -- Simulating a 1-second window
bpm <= beat_count * 10; -- Example scaling factor
beat_count <= 0;
end if;
end if;
end process;
heart_rate <= bpm;
end Behavioral;
Tcl Console Messages Log Reports Design Runs DRC Methodology Power Timing
General Information
Timer Settings
Design Timing Summary
Setup Hold Pulse Width
Timing Summary - impl_1 (saved)
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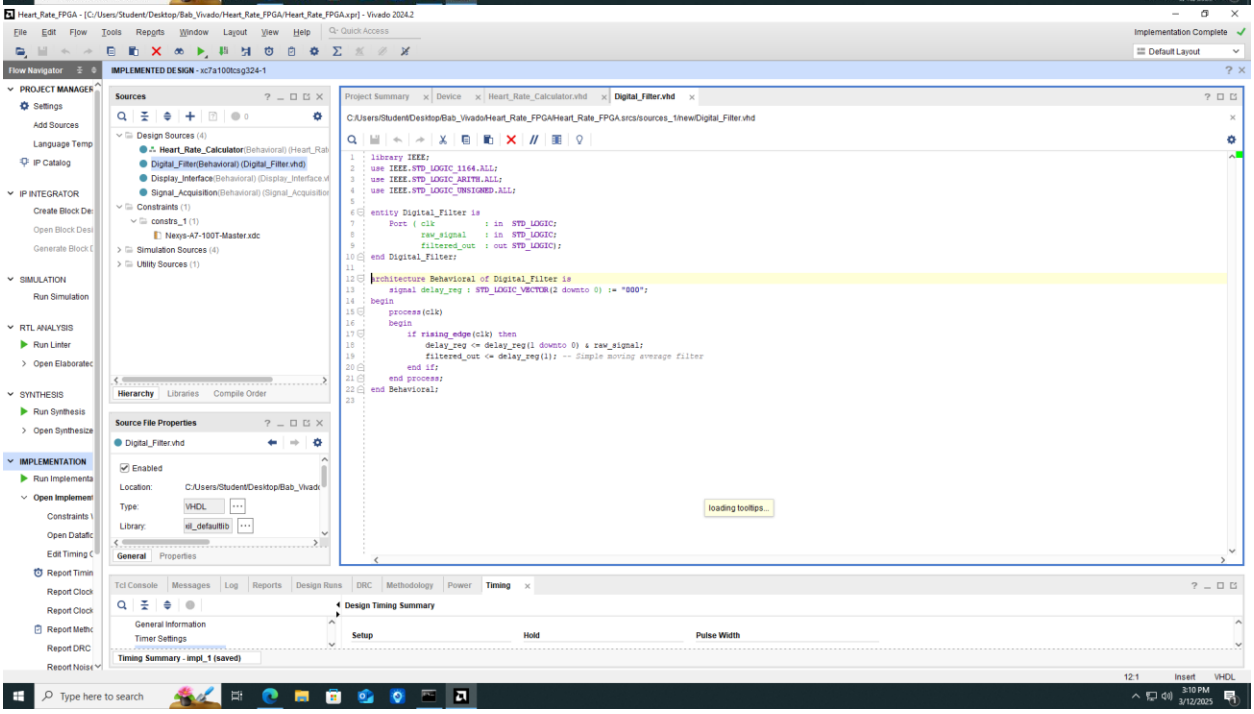
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Source File Properties
Digital_Filter.vhd
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Type: VHDL
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General Properties
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity Digital_Filter is
Port ( clk : in STD_LOGIC;
raw_signal : in STD_LOGIC;
filtered_out : out STD_LOGIC);
end Digital_Filter;
architecture Behavioral of Digital_Filter is
signal delay_reg : STD_LOGIC_VECTOR(2 downto 0) := "000";
begin
process(clk)
begin
if rising_edge(clk) then
delay_reg <= delay_reg(1 downto 0) & raw_signal;
filtered_out <= delay_reg(1); -- Simple moving average filter
end if;
end process;
end Behavioral;
loading tooltips...
Tcl Console Messages Log Reports Design Runs DRC Methodology Power Timing
General Information
Timer Settings
Design Timing Summary
Setup Hold Pulse Width
Timing Summary - impl_1 (saved)
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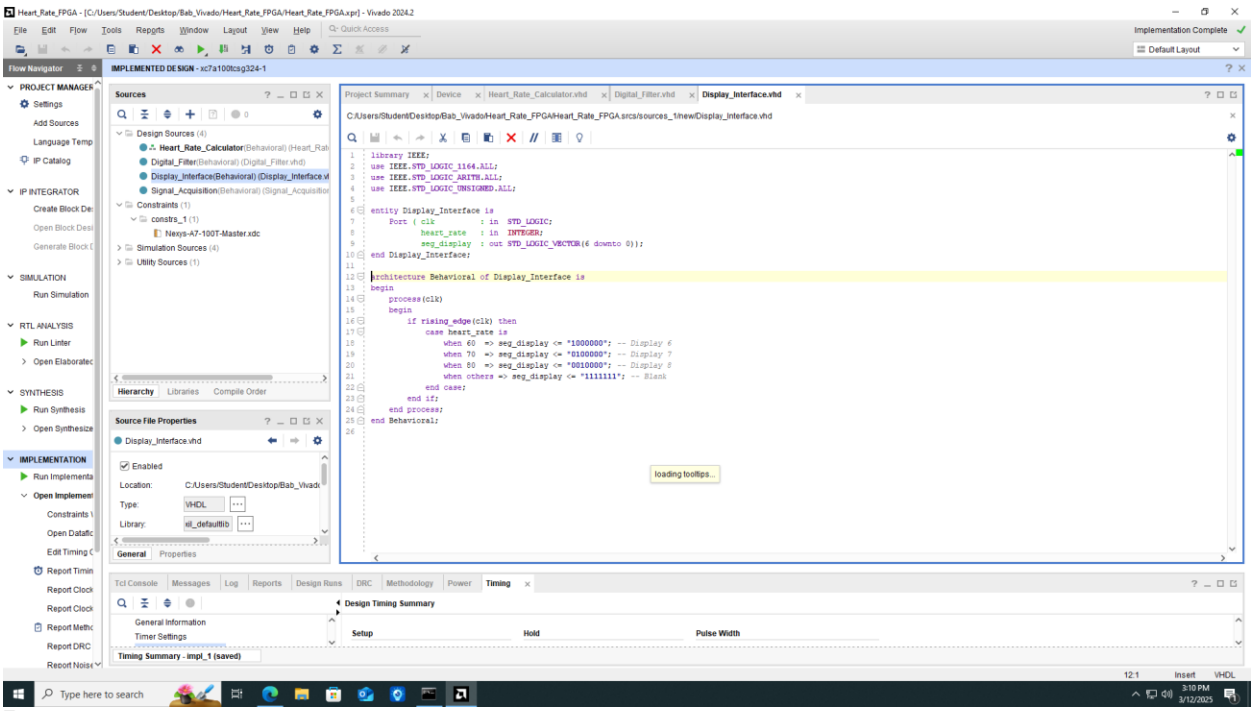
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Hierarchy Libraries Compile Order
Source File Properties
Display_Interface.vhd
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Location: C:/Users/Student/Desktop/Bab_Vivad
Type: VHDL
Library: xil_defaultlib
General Properties
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity Display_Interface is
Port ( clk : in STD_LOGIC;
heart_rate : in INTEGER;
seg_display : out STD_LOGIC_VECTOR(6 downto 0));
end Display_Interface;
architecture Behavioral of Display_Interface is
begin
process(clk)
begin
if rising_edge(clk) then
case heart_rate is
when 60 => seg_display <= "1000000"; -- Display 6
when 70 => seg_display <= "0100000"; -- Display 7
when 80 => seg_display <= "0010000"; -- Display 8
when others => seg_display <= "1111111"; -- Blank
end case;
end if;
end process;
end Behavioral;
loading tooltips...
Tcl Console Messages Log Reports Design Runs DRC Methodology Power Timing
General Information
Timer Settings
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Timing Summary - impl_1 (saved)
12:1 Insert VHDL
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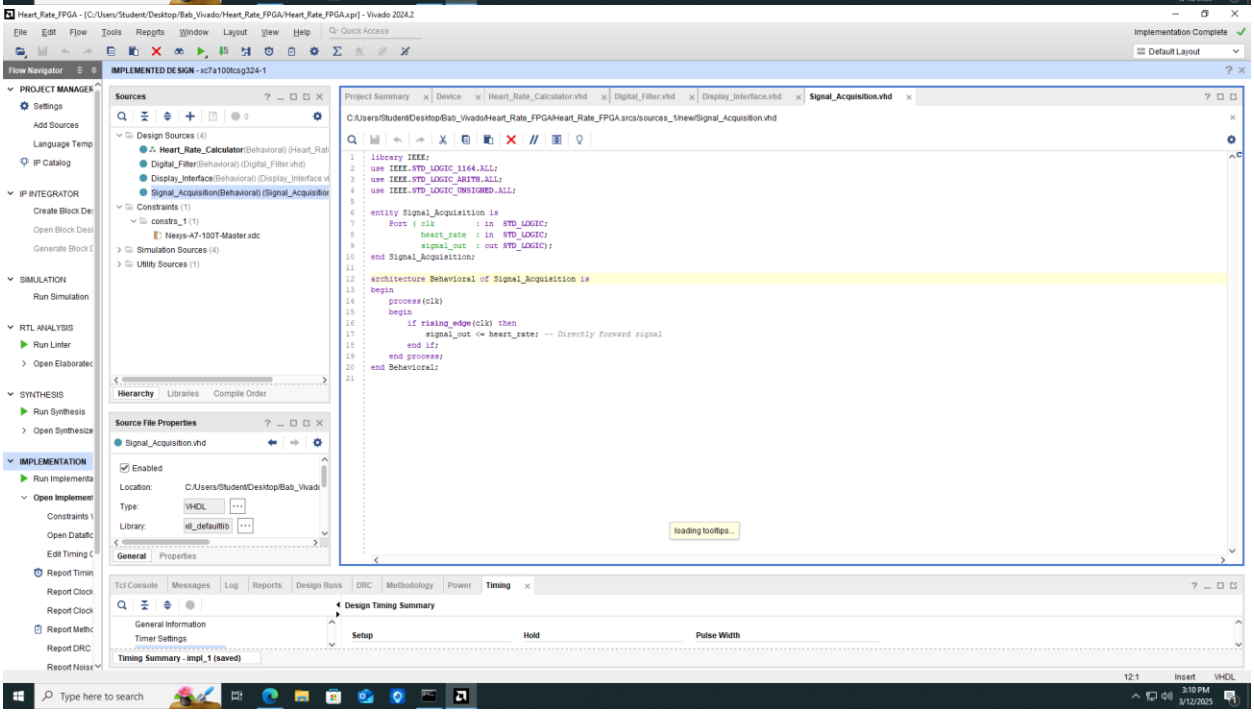
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Simulation Sources (4)
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Hierarchy Libraries Compile Order
Source File Properties
Signal_Acquisition.vhd
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Location: C:/Users/Student/Desktop/Bab_Vivad
Type: VHDL
Library: xil_defaultlib
General Properties
Project Summary
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Heart_Rate_Calculator.vhd
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Display_Interface.vhd
Signal_Acquisition.vhd
C:/Users/Student/Desktop/Bab_Vivado/Heart_Rate_FPGA/Heart_Rate_FPGA.srcs/sources_1/new/Signal_Acquisition.vhd
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity Signal_Acquisition is
Port ( clk : in STD_LOGIC;
heart_rate : in STD_LOGIC;
signal_out : out STD_LOGIC);
end Signal_Acquisition;
architecture Behavioral of Signal_Acquisition is
begin
process(clk)
begin
if rising_edge(clk) then
signal_out <= heart_rate; -- Directly forward signal
end if;
end process;
end Behavioral;
loading tooltips...
Tcl Console Messages Log Reports Design Runs DRC Methodology Power Timing
General Information
Timer Settings
Design Timing Summary
Setup Hold Pulse Width
Timing Summary - impl_1 (saved)
12:1 Insert VHDL
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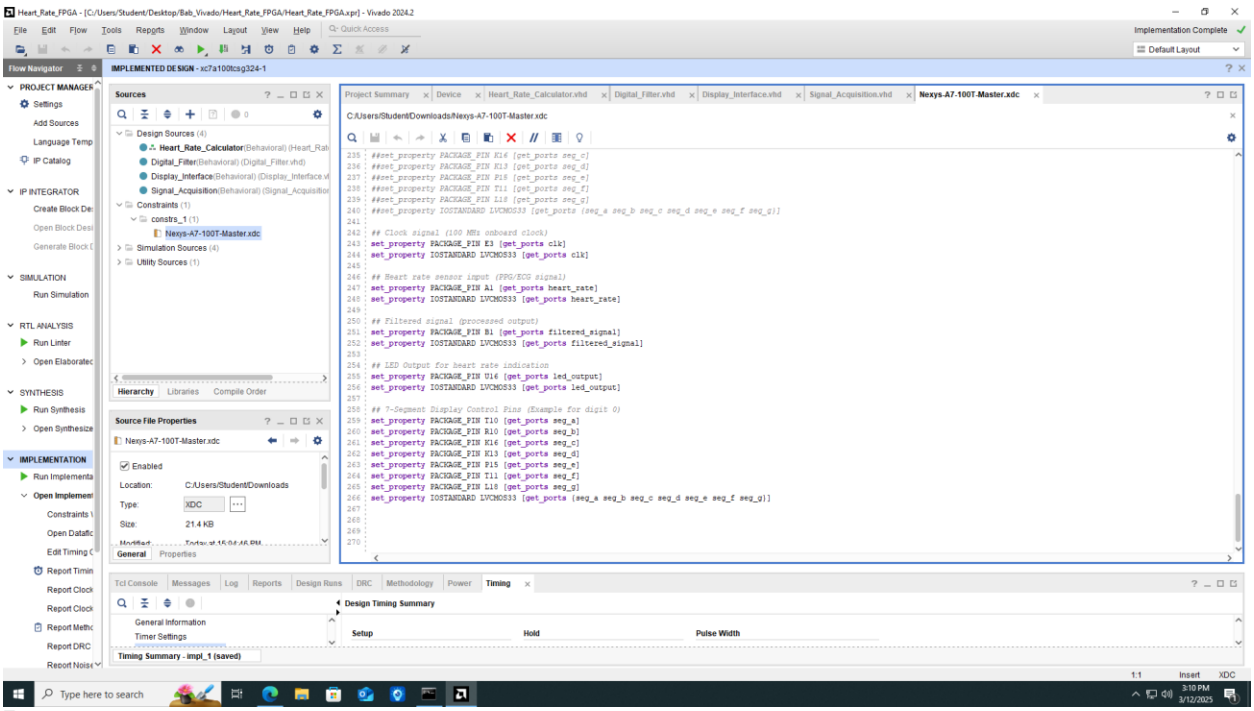
Heart_Rate_FPGA - [C:/Users/Student/Desktop/Bab_Vivado/Heart_Rate_FPGA/Heart_Rate_FPGA.xpr] - Vivado 2024.2
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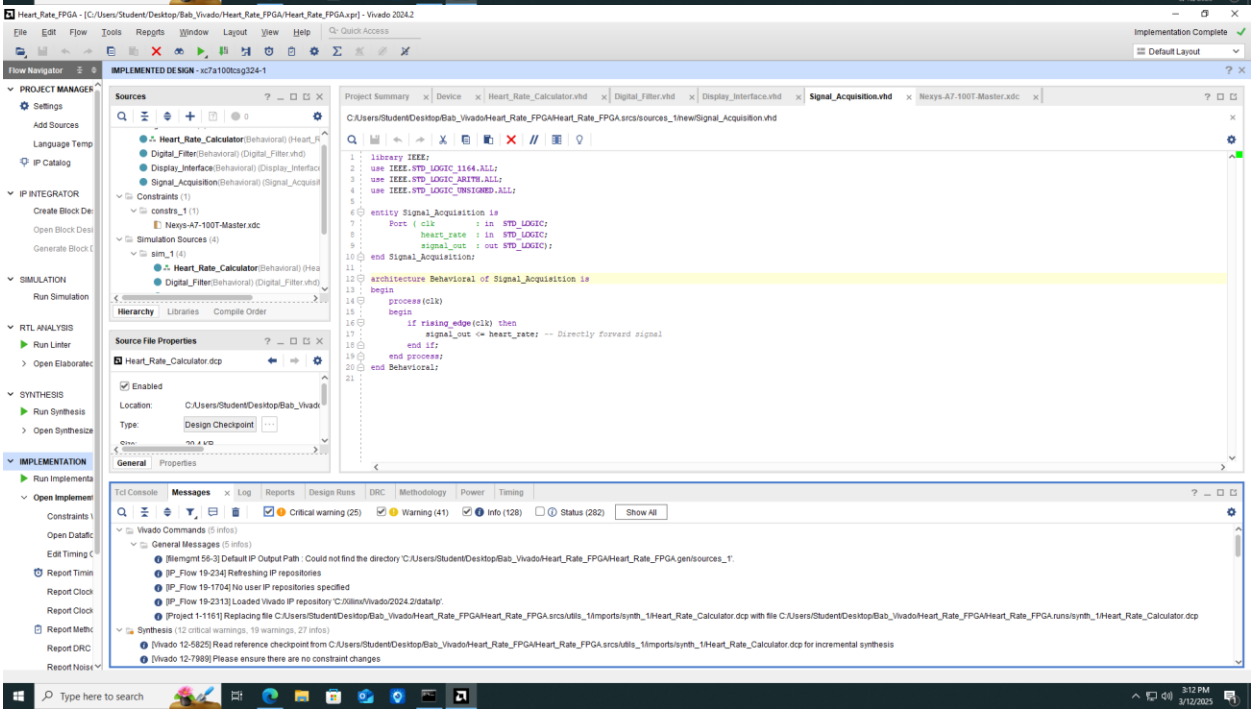
Simulation Sources (4)
Utility Sources (1)
Hierarchy Libraries Compile Order
Source File Properties
Nexys-A7-100T-Master.xdc
Enabled
Location: C:/Users/Student/Downloads
Type: XDC
Size: 21.4 KB
General Properties
Project Summary Device Heart_Rate_Calculator.vhd Digital_Filter.vhd Display_Interface.vhd Signal_Acquisition.vhd Nexys-A7-100T-Master.xdc
C:/Users/Student/Downloads/Nexys-A7-100T-Master.xdc
##set_property PACKAGE_PIN K16 [get_ports seg_c]
##set_property PACKAGE_PIN K13 [get_ports seg_d]
##set_property PACKAGE_PIN P15 [get_ports seg_e]
##set_property PACKAGE_PIN T11 [get_ports seg_f]
##set_property PACKAGE_PIN L18 [get_ports seg_g]
##set_property IOSTANDARD LVCMOS33 [get_ports {seg_a seg_b seg_c seg_d seg_e seg_f seg_g}]
## Clock signal (100 MHz onboard clock)
set_property PACKAGE_PIN E3 [get_ports clk]
set_property IOSTANDARD LVCMOS33 [get_ports clk]
## Heart rate sensor input (PPG/ECG signal)
set_property PACKAGE_PIN A1 [get_ports heart_rate]
set_property IOSTANDARD LVCMOS33 [get_ports heart_rate]
## Filtered signal (processed output)
set_property PACKAGE_PIN B1 [get_ports filtered_signal]
set_property IOSTANDARD LVCMOS33 [get_ports filtered_signal]
## LED Output for heart rate indication
set_property PACKAGE_PIN U16 [get_ports led_output]
set_property IOSTANDARD LVCMOS33 [get_ports led_output]
## 7-Segment Display Control Pins (Example for digit 0)
set_property PACKAGE_PIN T10 [get_ports seg_a]
set_property PACKAGE_PIN R10 [get_ports seg_b]
set_property PACKAGE_PIN K16 [get_ports seg_c]
set_property PACKAGE_PIN K13 [get_ports seg_d]
set_property PACKAGE_PIN P15 [get_ports seg_e]
set_property PACKAGE_PIN T11 [get_ports seg_f]
set_property PACKAGE_PIN L18 [get_ports seg_g]
set_property IOSTANDARD LVCMOS33 [get_ports {seg_a seg_b seg_c seg_d seg_e seg_f seg_g}]
Tcl Console Messages Log Reports Design Runs DRC Methodology Power Timing
General Information
Timer Settings
Design Timing Summary
Setup Hold Pulse Width
Timing Summary - impl_1 (saved)
1:1 Insert XDC
Type here to search
3:10 PM 3/12/2025


Heart_Rate_FPGA - [C:/Users/Student/Desktop/Bab_Vivado/Heart_Rate_FPGA/Heart_Rate_FPGA.xpr] - Vivado 2024.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Implementation Complete
Default Layout
Flow Navigator
IMPLEMENTED DESIGN - xc7a100tcsg324-1
PROJECT MANAGER
Settings
Add Sources
Language Temp
IP Catalog
IP INTEGRATOR
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SIMULATION
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Edit Timing C
Report Timin
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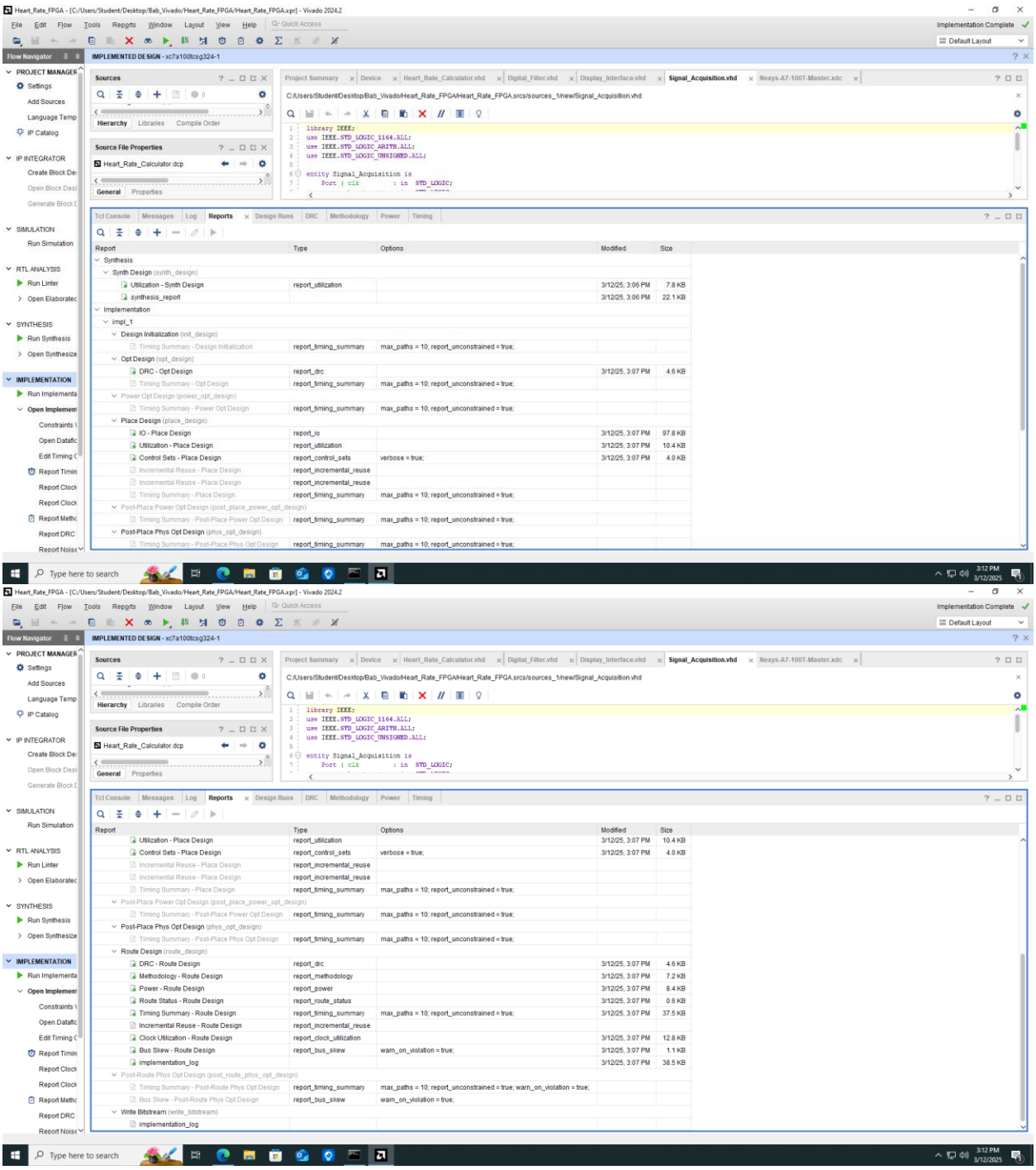
Report Metho
Report DRC
Report Noise
Sources
Heart_Rate_Calculator(Behavioral) (Heart_R
Digital_Filter(Behavioral) (Digital_Filter.vhd)
Display_Interface(Behavioral) (Display_Interfac
Signal_Acquisition(Behavioral) (Signal_Acquisit
Constraints (1)
constrs_1 (1)
Nexys-A7-100T-Master.xdc
Simulation Sources (4)
sim_1 (4)
Heart_Rate_Calculator(Behavioral) (Hea
Digital_Filter(Behavioral) (Digital_Filter.vhd)
Hierarchy Libraries Compile Order
Source File Properties
Heart_Rate_Calculator.dcp
Enabled
Location: C:/Users/Student/Desktop/Bab_Vivad
Type: Design Checkpoint
General Properties
Project Summary Device Heart_Rate_Calculator.vhd Digital_Filter.vhd Display_Interface.vhd Signal_Acquisition.vhd Nexys-A7-100T-Master.xdc
C:/Users/Student/Desktop/Bab_Vivado/Heart_Rate_FPGA/Heart_Rate_FPGA.srcs/sources_1/new/Signal_Acquisition.vhd
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity Signal_Acquisition is
Port ( clk : in STD_LOGIC;
heart_rate : in STD_LOGIC;
signal_out : out STD_LOGIC);
end Signal_Acquisition;
architecture Behavioral of Signal_Acquisition is
begin
process(clk)
begin
if rising_edge(clk) then
signal_out <= heart_rate; -- Directly forward signal
end if;
end process;
end Behavioral;
Tcl Console Messages Log Reports Design Runs DRC Methodology Power Timing
Critical warning (25) Warning (41) Info (128) Status (282) Show All
Vivado Commands (5 infos)
General Messages (5 infos)
[Memgmt 56-3] Default IP Output Path : Could not find the directory 'C:/Users/Student/Desktop/Bab_Vivado/Heart_Rate_FPGA/Heart_Rate_FPGA.gen/sources_1'.
[IP_Flow 19-234] Refreshing IP repositories
[IP_Flow 19-1704] No user IP repositories specified
[IP_Flow 19-2313] Loaded Vivado IP repository 'C:/Xilinx/Vivado/2024.2/data/ip'.
[Project 1-1161] Replacing file C:/Users/Student/Desktop/Bab_Vivado/Heart_Rate_FPGA/Heart_Rate_FPGA.srcs/utils_1/imports/synth_1/Heart_Rate_Calculator.dcp with file C:/Users/Student/Desktop/Bab_Vivado/Heart_Rate_FPGA/Heart_Rate_FPGA.runs/synth_1/Heart_Rate_Calculator.dcp
Synthesis (12 critical warnings, 19 warnings, 27 infos)
[Vivado 12-5825] Read reference checkpoint from C:/Users/Student/Desktop/Bab_Vivado/Heart_Rate_FPGA/Heart_Rate_FPGA.srcs/utils_1/imports/synth_1/Heart_Rate_Calculator.dcp for incremental synthesis
[Vivado 12-7989] Please ensure there are no constraint changes
Type here to search
3:12 PM 3/12/2025


Heart_Rate_FPGA - [C:/Users/Student/Desktop/Bab_Vivado/Heart_Rate_FPGA/Heart_Rate_FPGA.xpr] - Vivado 2024.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Implementation Complete
Default Layout
Flow Navigator
IMPLEMENTED DESIGN - xc7a100tcsg324-1
PROJECT MANAGER
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Add Sources
Language Temp
IP Catalog
IP INTEGRATOR
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RTL ANALYSIS
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Open Synthesize
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Report Timin
Report Clock
Report Clock
Report Metho
Report DRC
Report Noise
Sources
Hierarchy Libraries Compile Order
Source File Properties
Heart_Rate_Calculator.dcp
General Properties
Project Summary
Device
Heart_Rate_Calculator.vhd
Digital_Filter.vhd
Display_Interface.vhd
Signal_Acquisition.vhd
Nexys-A7-100T-Master.xdc
C:/Users/Student/Desktop/Bab_Vivado/Heart_Rate_FPGA/Heart_Rate_FPGA.srcs/sources_1/new/Signal_Acquisition.vhd
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity Signal_Acquisition is
Port ( clk : in STD_LOGIC;
Tcl Console Messages Log Reports Design Runs DRC Methodology Power Timing
Report Type Options Modified Size
Synthesis
Synth Design (synth_design)
Utilization - Synth Design report_utilization 3/12/25, 3:06 PM 7.8 KB
synthesis_report 3/12/25, 3:06 PM 22.1 KB
Implementation
impl_1
Design Initialization (init_design)
Timing Summary - Design Initialization report_timing_summary max_paths = 10; report_unconstrained = true;
Opt Design (opt_design)
DRC - Opt Design report_drc 3/12/25, 3:07 PM 4.6 KB
Timing Summary - Opt Design report_timing_summary max_paths = 10; report_unconstrained = true;
Power Opt Design (power_opt_design)
Timing Summary - Power Opt Design report_timing_summary max_paths = 10; report_unconstrained = true;
Place Design (place_design)
IO - Place Design report_io 3/12/25, 3:07 PM 97.8 KB
Utilization - Place Design report_utilization 3/12/25, 3:07 PM 10.4 KB
Control Sets - Place Design report_control_sets verbose = true; 3/12/25, 3:07 PM 4.0 KB
Incremental Reuse - Place Design report_incremental_reuse
Incremental Reuse - Place Design report_incremental_reuse
Timing Summary - Place Design report_timing_summary max_paths = 10; report_unconstrained = true;
Post-Place Power Opt Design (post_place_power_opt_design)
Timing Summary - Post-Place Power Opt Design report_timing_summary max_paths = 10; report_unconstrained = true;
Post-Place Phys Opt Design (phys_opt_design)
Timing Summary - Post-Place Phys Opt Design report_timing_summary max_paths = 10; report_unconstrained = true;
Type here to search
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3/12/2025


Heart_Rate_FPGA - [C:/Users/Student/Desktop/Bab_Vivado/Heart_Rate_FPGA/Heart_Rate_FPGA.xpr] - Vivado 2024.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Implementation Complete
Default Layout
Flow Navigator
IMPLEMENTED DESIGN - xc7a100tcsg324-1
PROJECT MANAGER
Settings
Add Sources
Language Temp
IP Catalog
IP INTEGRATOR
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Run Simulation
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Run Linter
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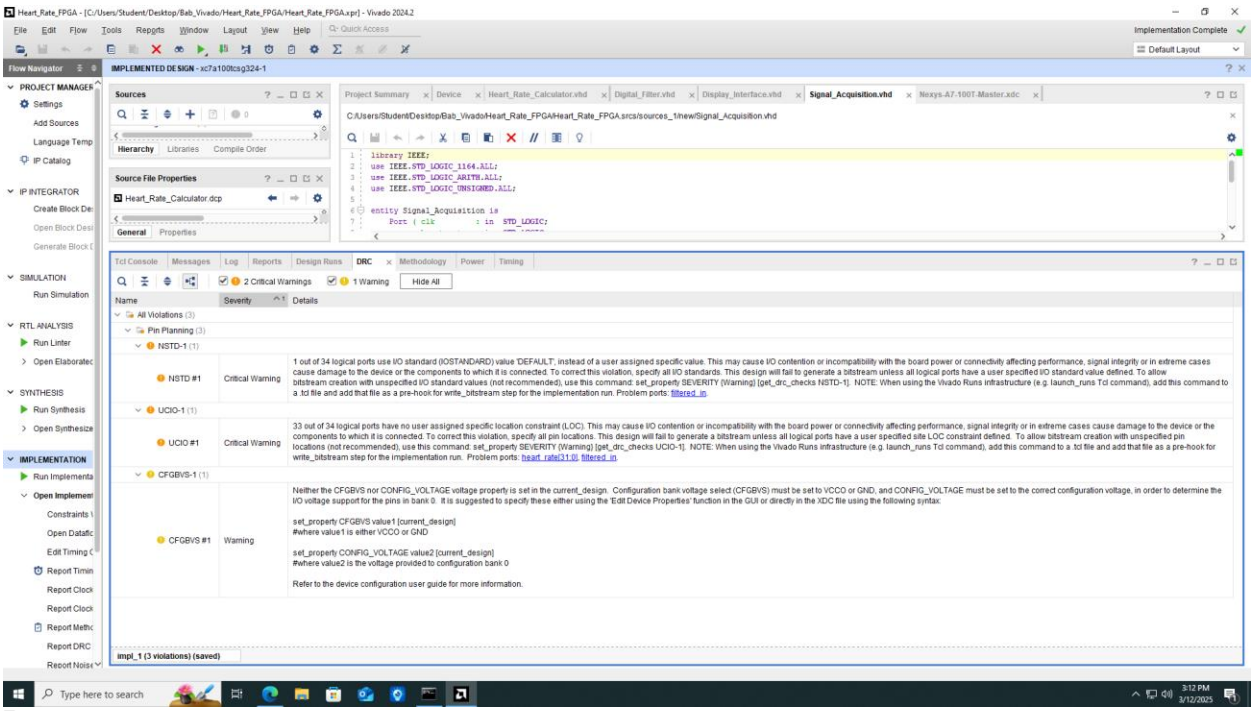
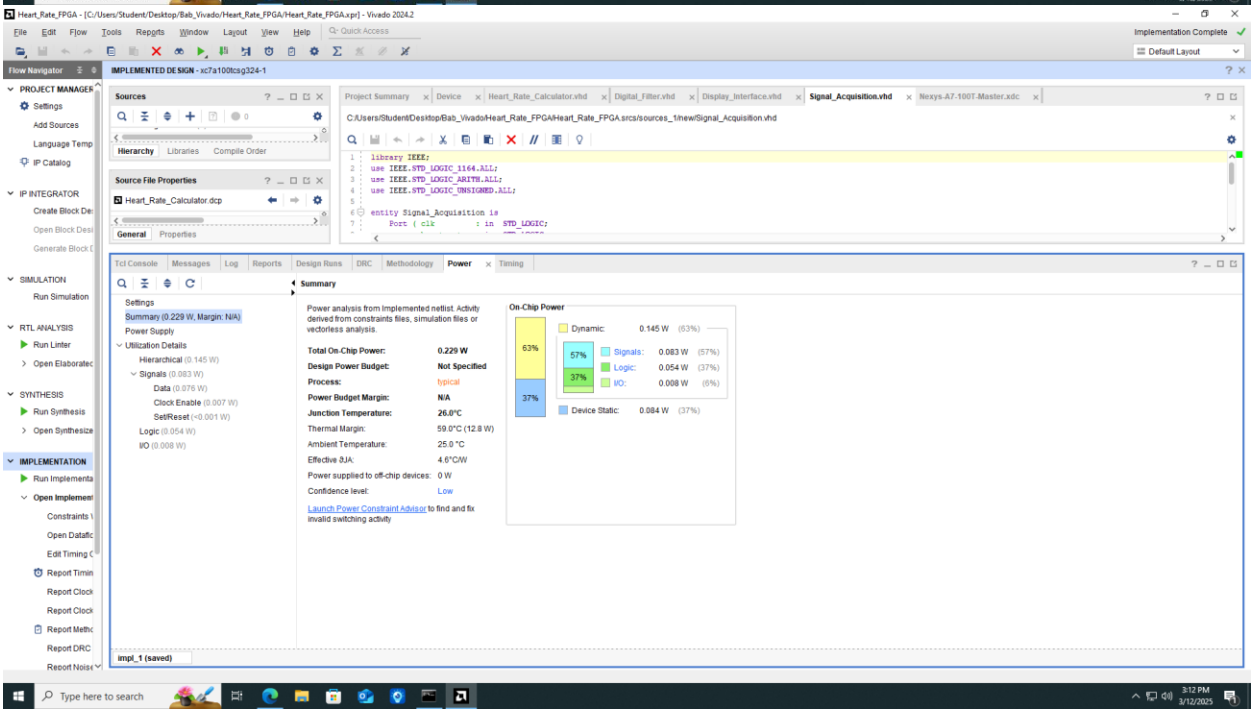
SYNTHESIS
Run Synthesis
Open Synthesize
IMPLEMENTATION
Run Implementa
Open Implemen
Constraints
Open Datafic
Edit Timing
Report Timin
Report Clock
Report Clock
Report Metho
Report DRC
Report Noise
Sources
Hierarchy Libraries Compile Order
Source File Properties
Heart_Rate_Calculator.dcp
General Properties
Project Summary
Device
Heart_Rate_Calculator.vhd
Digital_Filter.vhd
Display_Interface.vhd
Signal_Acquisition.vhd
Nexys-A7-100T-Master.xdc
C:/Users/Student/Desktop/Bab_Vivado/Heart_Rate_FPGA/Heart_Rate_FPGA.srcs/sources_1/new/Signal_Acquisition.vhd
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity Signal_Acquisition is
Port ( clk : in STD_LOGIC;
Tcl Console Messages Log Reports Design Runs DRC Methodology Power Timing
Report Type Options Modified Size
Utilization - Place Design report_utilization 3/12/25, 3:07 PM 10.4 KB
Control Sets - Place Design report_control_sets verbose = true; 3/12/25, 3:07 PM 4.0 KB
Incremental Reuse - Place Design report_incremental_reuse
Incremental Reuse - Place Design report_incremental_reuse
Timing Summary - Place Design report_timing_summary max_paths = 10; report_unconstrained = true;
Post-Place Power Opt Design (post_place_power_opt_design)
Timing Summary - Post-Place Power Opt Design report_timing_summary max_paths = 10; report_unconstrained = true;
Post-Place Phys Opt Design (phys_opt_design)
Timing Summary - Post-Place Phys Opt Design report_timing_summary max_paths = 10; report_unconstrained = true;
Route Design (route_design)
DRC - Route Design report_drc 3/12/25, 3:07 PM 4.6 KB
Methodology - Route Design report_methodology 3/12/25, 3:07 PM 7.2 KB
Power - Route Design report_power 3/12/25, 3:07 PM 8.4 KB
Route Status - Route Design report_route_status 3/12/25, 3:07 PM 0.6 KB
Timing Summary - Route Design report_timing_summary max_paths = 10; report_unconstrained = true; 3/12/25, 3:07 PM 37.5 KB
Incremental Reuse - Route Design report_incremental_reuse
Clock Utilization - Route Design report_clock_utilization 3/12/25, 3:07 PM 12.8 KB
Bus Skew - Route Design report_bus_skew warn_on_violation = true; 3/12/25, 3:07 PM 1.1 KB
implementation_log 3/12/25, 3:07 PM 38.5 KB
Post-Route Phys Opt Design (post_route_phys_opt_design)
Timing Summary - Post-Route Phys Opt Design report_timing_summary max_paths = 10; report_unconstrained = true; warn_on_violation = true;
Bus Skew - Post-Route Phys Opt Design report_bus_skew warn_on_violation = true;
Write Bitstream (write_bitstream)
implementation_log
Type here to search
3:12 PM
3/12/2025


Heart_Rate_FPGA - [C:/Users/Student/Desktop/Bab_Vivado/Heart_Rate_FPGA/Heart_Rate_FPGA.xpr] - Vivado 2024.2
File Edit Flow Tools Reports Window Layout View Help
Implementation Complete
Default Layout
Flow Navigator
IMPLEMENTED DESIGN - xc7a100tcsg324-1
Sources
Hierarchy Libraries Compile Order
Source File Properties
Heart_Rate_Calculator.dcp
General Properties
Project Summary Device Heart_Rate_Calculator.vhd Digital_Filter.vhd Display_Interface.vhd Signal_Acquisition.vhd Nexys-A7-100T-Master.xdc
C:/Users/Student/Desktop/Bab_Vivado/Heart_Rate_FPGA/Heart_Rate_FPGA.srcs/sources_1/new/Signal_Acquisition.vhd
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity Signal_Acquisition is
Port ( clk : in STD_LOGIC;
Tcl Console Messages Log Reports Design Runs DRC Methodology Power Timing
2 Critical Warnings 1 Warning Hide All
Name Severity Details
All Violations (3)
Pin Planning (3)
NSTD-1 (1)
NSTD #1 Critical Warning
1 out of 34 logical ports use I/O standard (IOSTANDARD) value 'DEFAULT', instead of a user assigned specific value. This may cause I/O contention or incompatibility with the board power or connectivity affecting performance, signal integrity or in extreme cases cause damage to the device or the components to which it is connected. To correct this violation, specify all I/O standards. This design will fail to generate a bitstream unless all logical ports have a user specified I/O standard value defined. To allow bitstream creation with unspecified I/O standard values (not recommended), use this command: set_property SEVERITY {Warning} [get_drc_checks NSTD-1]. NOTE: When using the Vivado Runs infrastructure (e.g. launch_runs Tcl command), add this command to a .tcl file and add that file as a pre-hook for write_bitstream step for the implementation run. Problem ports: filtered_in
UCIO-1 (1)
UCIO #1 Critical Warning
33 out of 34 logical ports have no user assigned specific location constraint (LOC). This may cause I/O contention or incompatibility with the board power or connectivity affecting performance, signal integrity or in extreme cases cause damage to the device or the components to which it is connected. To correct this violation, specify all pin locations. This design will fail to generate a bitstream unless all logical ports have a user specified site LOC constraint defined. To allow bitstream creation with unspecified pin locations (not recommended), use this command: set_property SEVERITY {Warning} [get_drc_checks UCIO-1]. NOTE: When using the Vivado Runs infrastructure (e.g. launch_runs Tcl command), add this command to a .tcl file and add that file as a pre-hook for write_bitstream step for the implementation run. Problem ports: heart_rate[31:0], filtered_in
CFGBVS-1 (1)
CFGBVS #1 Warning
Neither the CFGBVS nor CONFIG_VOLTAGE voltage property is set in the current_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG_VOLTAGE must be set to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0. It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax:
set_property CFGBVS value1 [current_design]
#where value1 is either VCCO or GND
set_property CONFIG_VOLTAGE value2 [current_design]
#where value2 is the voltage provided to configuration bank 0
Refer to the device configuration user guide for more information.
impl_1 (3 violations) (saved)
Type here to search
3:12 PM 3/12/2025


Heart_Rate_FPGA - [C:/Users/Student/Desktop/Bab_Vivado/Heart_Rate_FPGA/Heart_Rate_FPGA.xpr] - Vivado 2024.2
File Edit Flow Tools Reports Window Layout View Help
Implementation Complete
Default Layout
Flow Navigator
IMPLEMENTED DESIGN - xc7a100tcsg324-1
Sources
Hierarchy Libraries Compile Order
Source File Properties
Heart_Rate_Calculator.dcp
General Properties
Project Summary Device Heart_Rate_Calculator.vhd Digital_Filter.vhd Display_Interface.vhd Signal_Acquisition.vhd Nexys-A7-100T-Master.xdc
C:/Users/Student/Desktop/Bab_Vivado/Heart_Rate_FPGA/Heart_Rate_FPGA.srcs/sources_1/new/Signal_Acquisition.vhd
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity Signal_Acquisition is
Port ( clk : in STD_LOGIC;
Tcl Console Messages Log Reports Design Runs DRC Methodology Power Timing
Summary
Settings
Summary (0.229 W, Margin: N/A)
Power Supply
Utilization Details
Hierarchical (0.145 W)
Signals (0.083 W)
Data (0.076 W)
Clock Enable (0.007 W)
Set/Reset (<0.001 W)
Logic (0.054 W)
I/O (0.008 W)
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.
Total On-Chip Power: 0.229 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 26.0°C
Thermal Margin: 59.0°C (12.8 W)
Ambient Temperature: 25.0 °C
Effective ΘJA: 4.6°C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Launch Power Constraint Advisor to find and fix invalid switching activity
On-Chip Power
63%
37%
Dynamic: 0.145 W (63%)
57%
37%
Signals: 0.083 W (57%)
Logic: 0.054 W (37%)
I/O: 0.008 W (6%)
Device Static: 0.084 W (37%)
impl_1 (saved)
Type here to search
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## Results

- The FPGA successfully processed heart rate signals in real-time.
- BPM calculations were accurately displayed on **7-segment display and LED indicators**.
- The system effectively filtered noise and detected heartbeats with minimal error.
- Testing verified **proper signal acquisition, processing, and display functionality**.

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## Conclusion

The objective of the project was successfully achieved. The FPGA-based heart rate monitoring system demonstrated **real-time processing, efficient signal filtering, and accurate BPM calculations**. Compared to software-based approaches, the **hardware implementation on FPGA** provided faster computation and real-time responsiveness.

## Future Improvements:

- **Advanced DSP Algorithms:** Improve filtering techniques for noise reduction.
- **Wireless Transmission:** Integrate Bluetooth/Wi-Fi for remote monitoring.
- **Graphical Display:** Use an **LCD screen** for better visualization of heart rate trends.

The project highlights the potential of FPGA-based solutions for **real-time biomedical applications**, making it a promising technology for healthcare monitoring systems.

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