Lab Report

Created By: Bab

Introduction

The goal of this first portion of the lab was to create a baseline design for your development kit of choice to create a bitfile, which will be used to program the Artix-7 FPGA on the development board with a block design as well as a “Hello World” program in Vitis IDE.

Equipment Used

Xilinix board (Nexys A7)

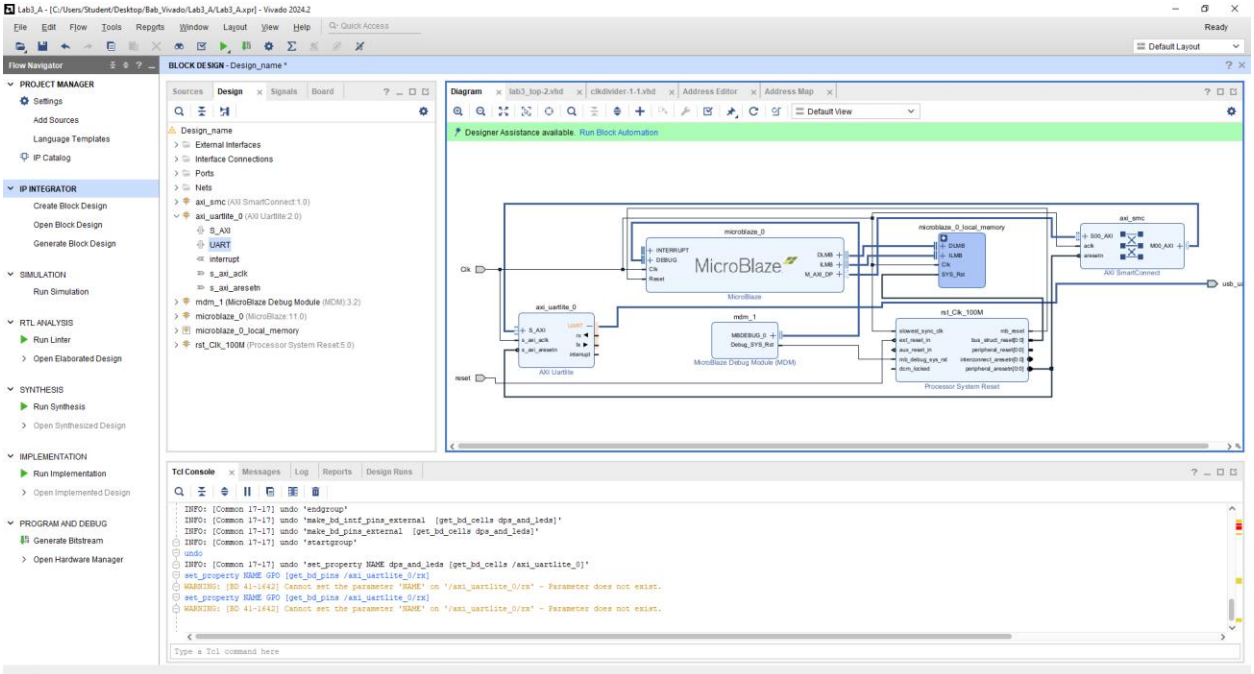
Procedure

1) Downloading Vivado
2) Downloading diligent Board files
3) Creating a Vivado Project
4) Adding two VHDL files
5) Vivado Design Flow
    a. Run Synthesis
    b. Run Implementation
    c. Generate Bitatream

6) Programing FPGA
7) Hardware Board Setup (Xilinix) and programing the device

Results

Here the results of the lab. Including the graphs or pictures or the like depicting or showcasing Lab’s results.


Lab3_A - [C:/Users/Student/Desktop/Bab_Vivado/Lab3_A/Lab3_A.xpr] - Vivado 2024.2
File Edit Flow Tools Reports Window Layout View Help
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Run Synthesis
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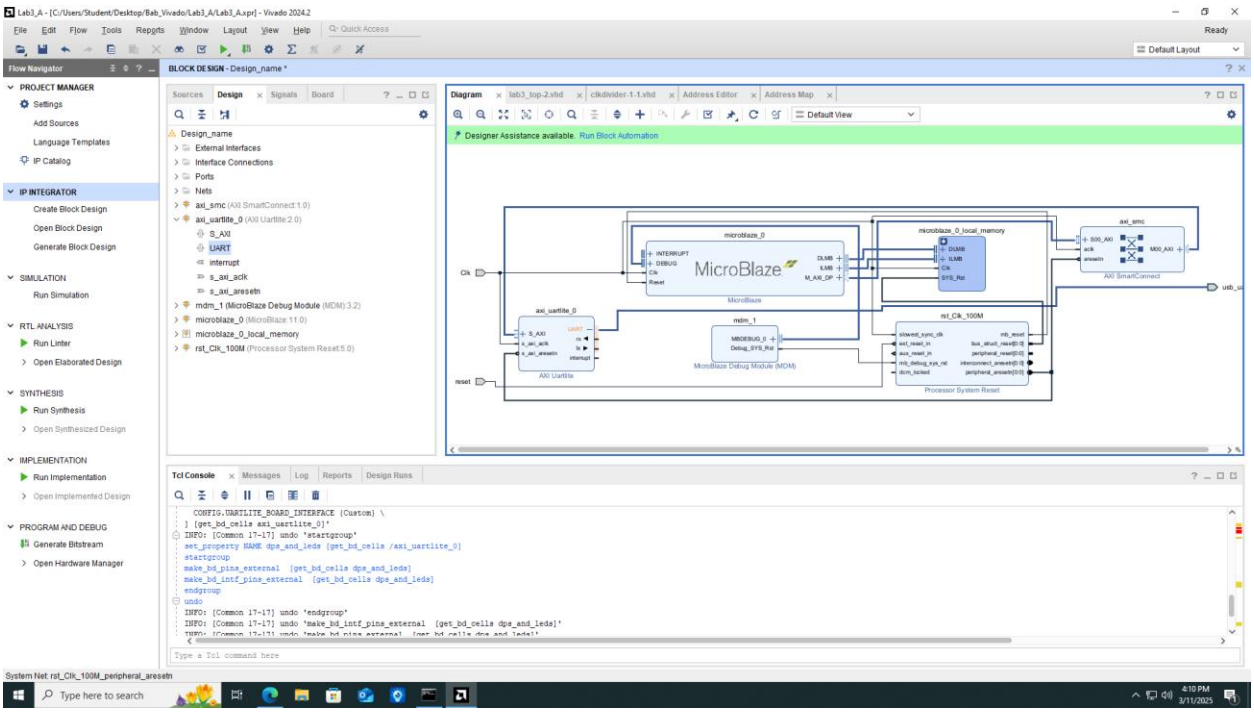
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
BLOCK DESIGN - Design_name *
Sources
Design
Signals
Board
Design_name
External Interfaces
Interface Connections
Ports
Nets
axi_smc (AXI SmartConnect:1.0)
axi_uartlite_0 (AXI Uartlite:2.0)
S_AXI
UART
interrupt
s_axi_aclk
s_axi_aresetn
mdm_1 (MicroBlaze Debug Module (MDM):3.2)
microblaze_0 (MicroBlaze:11.0)
microblaze_0_local_memory
rst_Clk_100M (Processor System Reset:5.0)
Diagram
lab3_top-2.vhd
clkdivider-1-1.vhd
Address Editor
Address Map
Default View
Designer Assistance available. Run Block Automation
MicroBlaze
Clk
reset
usb_uart
Tcl Console
Messages
Log
Reports
Design Runs
INFO: [Common 17-17] undo 'endgroup'
INFO: [Common 17-17] undo 'make_bd_intf_pins_external [get_bd_cells dps_and_leds]'
INFO: [Common 17-17] undo 'make_bd_pins_external [get_bd_cells dps_and_leds]'
INFO: [Common 17-17] undo 'startgroup'
undo
INFO: [Common 17-17] undo 'set_property NAME dps_and_leds [get_bd_cells /axi_uartlite_0]'
set_property NAME GPO [get_bd_pins /axi_uartlite_0/rx]
WARNING: [BD 41-1642] Cannot set the parameter 'NAME' on '/axi_uartlite_0/rx' - Parameter does not exist.
set_property NAME GPO [get_bd_pins /axi_uartlite_0/rx]
WARNING: [BD 41-1642] Cannot set the parameter 'NAME' on '/axi_uartlite_0/rx' - Parameter does not exist.
Type a Tcl command here
Type here to search
4:10 PM
3/11/2025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BLOCK DESIGN - Design_name *
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Design
Signals
Board
Design_name
External Interfaces
Interface Connections
Ports
Nets
axi_smc (AXI SmartConnect:1.0)
axi_uartlite_0 (AXI Uartlite:2.0)
S_AXI
UART
interrupt
s_axi_aclk
s_axi_aresetn
mdm_1 (MicroBlaze Debug Module (MDM):3.2)
microblaze_0 (MicroBlaze:11.0)
microblaze_0_local_memory
rst_Clk_100M (Processor System Reset:5.0)
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clkdivider-1-1.vhd
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usb_uart
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Design Runs
CONFIG.UARTLITE_BOARD_INTERFACE {Custom} \
] [get_bd_cells axi_uartlite_0]'
INFO: [Common 17-17] undo 'startgroup'
set_property NAME dps_and_leds [get_bd_cells /axi_uartlite_0]
startgroup
make_bd_pins_external [get_bd_cells dps_and_leds]
make_bd_intf_pins_external [get_bd_cells dps_and_leds]
endgroup
undo
INFO: [Common 17-17] undo 'endgroup'
INFO: [Common 17-17] undo 'make_bd_intf_pins_external [get_bd_cells dps_and_leds]'
Type a Tcl command here
System Net: rst_Clk_100M_peripheral_aresetn
Type here to search
4:10 PM
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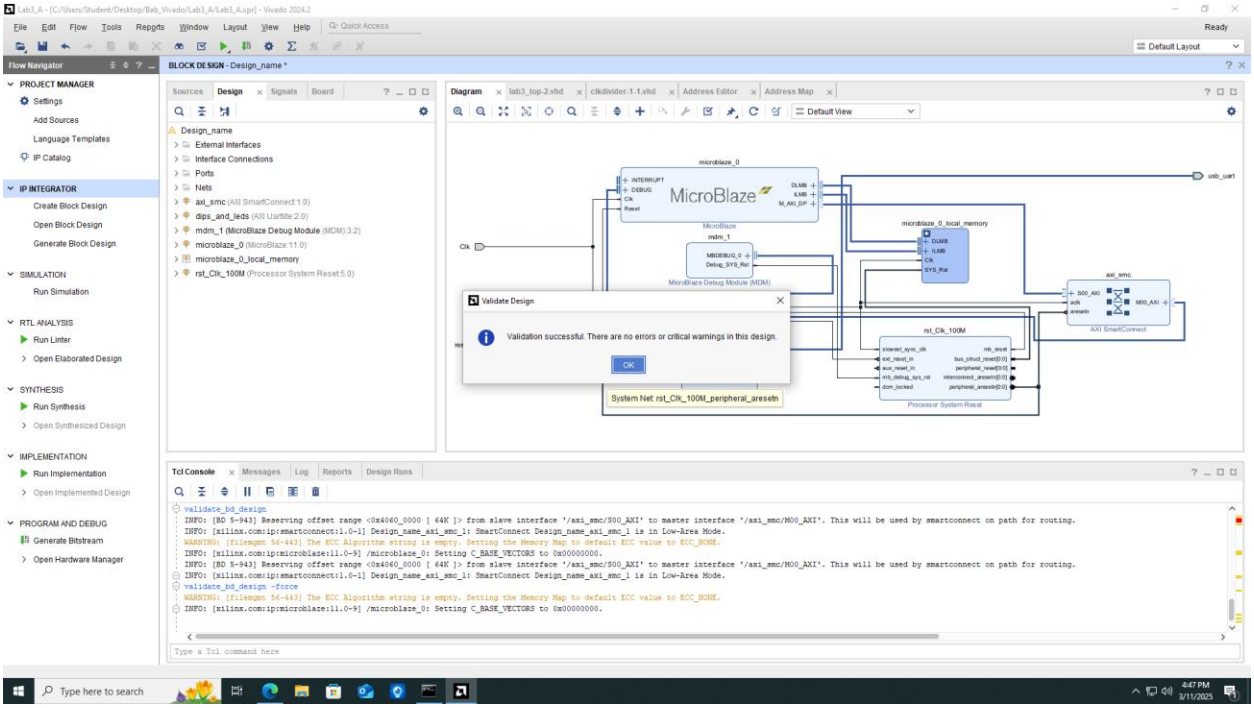
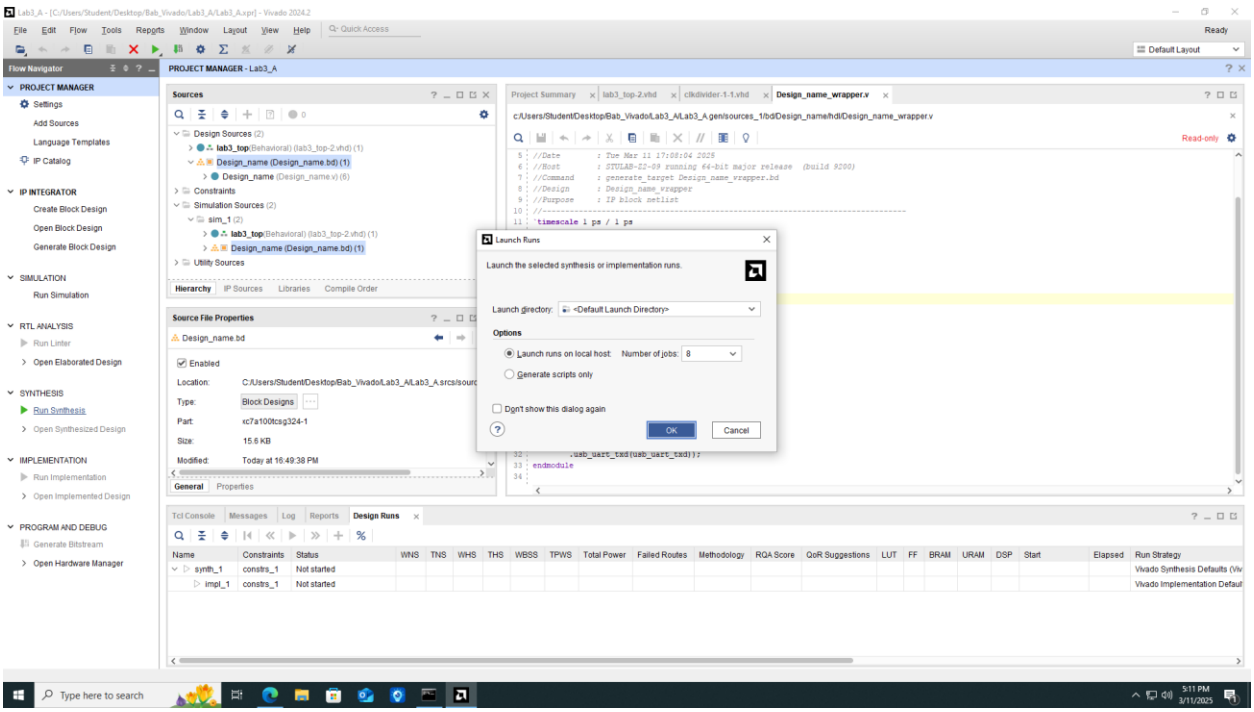
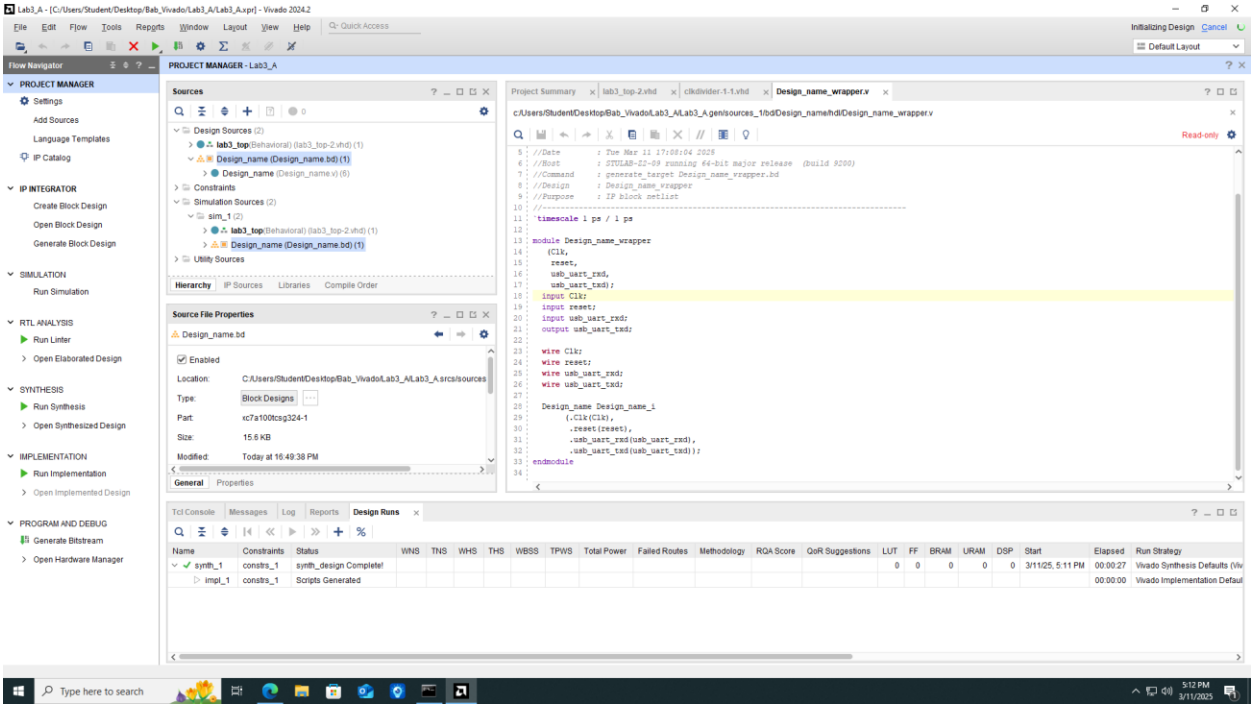

Validate Design
Validation successful. There are no errors or critical warnings in this design.
OK
Tcl Console
validate_bd_design
validate_bd_design -force


Launch Runs
Launch the selected synthesis or implementation runs.
Launch directory: <Default Launch Directory>
Launch runs on local host: Number of jobs: 8
Generate scripts only
Don't show this dialog again
OK
Cancel
Design Runs


Lab3_A - [C:/Users/Student/Desktop/Bab_Vivado/Lab3_A/Lab3_A.xpr] - Vivado 2024.2
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Initializing Design Cancel
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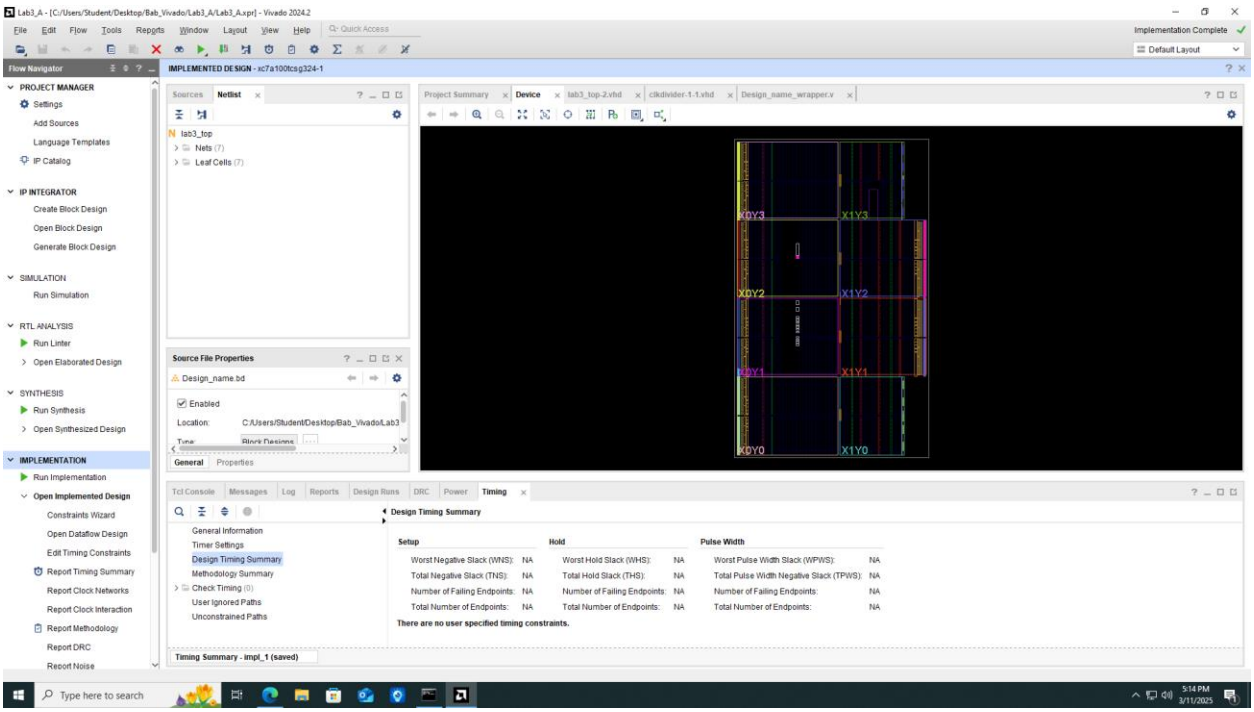
Sources
Design Sources (2)
lab3_top(Behavioral) (lab3_top-2.vhd) (1)
Design_name (Design_name.bd) (1)
Design_name (Design_name.v) (6)
Constraints
Simulation Sources (2)
sim_1 (2)
lab3_top(Behavioral) (lab3_top-2.vhd) (1)
Design_name (Design_name.bd) (1)
Utility Sources
Hierarchy IP Sources Libraries Compile Order
Source File Properties
Design_name.bd
Enabled
Location: C:/Users/Student/Desktop/Bab_Vivado/Lab3_A/Lab3_A.srcs/sources
Type: Block Designs
Part: xc7a100tcsg324-1
Size: 15.6 KB
Modified: Today at 16:49:38 PM
General Properties
Project Summary
lab3_top-2.vhd
clkdivider-1-1.vhd
Design_name_wrapper.v
c:/Users/Student/Desktop/Bab_Vivado/Lab3_A/Lab3_A.gen/sources_1/bd/Design_name/hdl/Design_name_wrapper.v
Read-only
//Date : Tue Mar 11 17:08:04 2025
//Host : STULAB-Z2-09 running 64-bit major release (build 9200)
//Command : generate_target Design_name_wrapper.bd
//Design : Design_name_wrapper
//Purpose : IP block netlist
`timescale 1 ps / 1 ps
module Design_name_wrapper
(Clk,
reset,
usb_uart_rxd,
usb_uart_txd);
input Clk;
input reset;
input usb_uart_rxd;
output usb_uart_txd;
wire Clk;
wire reset;
wire usb_uart_rxd;
wire usb_uart_txd;
Design_name Design_name_i
(.Clk(Clk),
.reset(reset),
.usb_uart_rxd(usb_uart_rxd),
.usb_uart_txd(usb_uart_txd));
endmodule
Tcl Console Messages Log Reports Design Runs
Name Constraints Status WNS TNS WHS THS WBSS TPWS Total Power Failed Routes Methodology RQA Score QoR Suggestions LUT FF BRAM URAM DSP Start Elapsed Run Strategy
synth_1 constrs_1 synth_design Complete! 0 0 0 0 0 3/11/25, 5:11 PM 00:00:27 Vivado Synthesis Defaults (Viv
impl_1 constrs_1 Scripts Generated 00:00:00 Vivado Implementation Defaul
Type here to search
5:12 PM
3/11/2025


Lab3_A - [C:/Users/Student/Desktop/Bab_Vivado/Lab3_A/Lab3_A.xpr] - Vivado 2024.2
File Edit Flow Tools Reports Window Layout View Help
Implementation Complete
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Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Sources Netlist
lab3_top
Nets (7)
Leaf Cells (7)
Source File Properties
Design_name.bd
Enabled
Location: C:/Users/Student/Desktop/Bab_Vivado/Lab3
General Properties
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Device
lab3_top-2.vhd
clkdivider-1-1.vhd
Design_name_wrapper.v
X0Y3
X1Y3
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Tcl Console Messages Log Reports Design Runs DRC Power Timing
General Information
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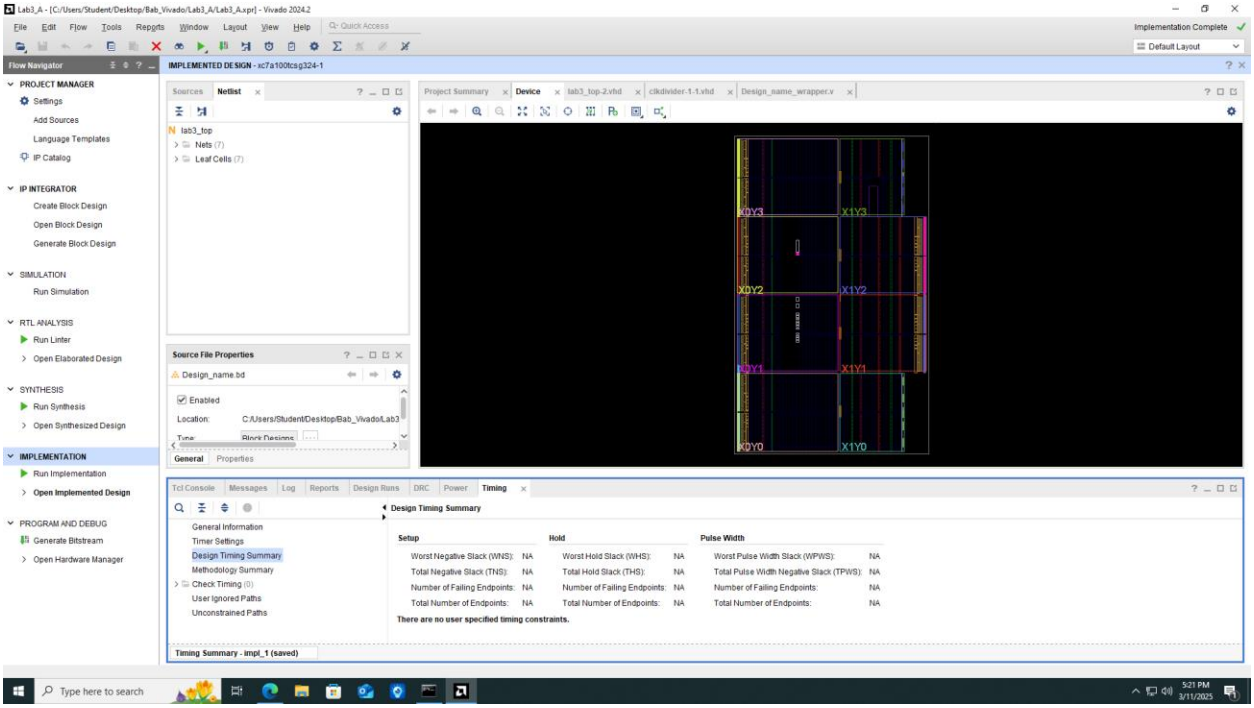
Design Timing Summary
Methodology Summary
Check Timing (0)
User Ignored Paths
Unconstrained Paths
Design Timing Summary
Setup
Worst Negative Slack (WNS): NA
Total Negative Slack (TNS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Hold
Worst Hold Slack (WHS): NA
Total Hold Slack (THS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Pulse Width
Worst Pulse Width Slack (WPWS): NA
Total Pulse Width Negative Slack (TPWS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
There are no user specified timing constraints.
Timing Summary - impl_1 (saved)
Type here to search
5:14 PM
3/11/2025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Source File Properties
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C:/Users/Student/Desktop/Bab_Vivado/Lab3
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clkdivider-1.1.vhd
Design_name_wrapper.v
X0Y3
X1Y3
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
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Pulse Width
Worst Negative Slack (WNS): NA
Worst Hold Slack (WHS): NA
Worst Pulse Width Slack (WPWS): NA
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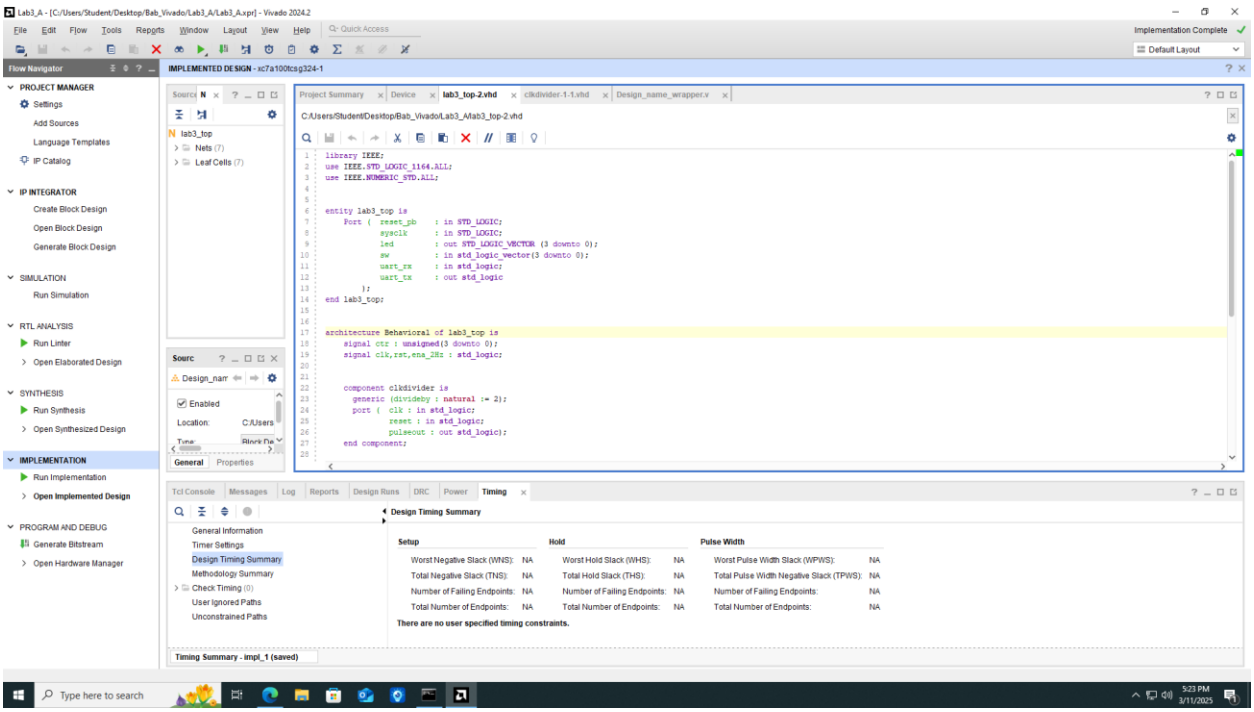
Total Hold Slack (THS): NA
Total Pulse Width Negative Slack (TPWS): NA
Number of Failing Endpoints: NA
Number of Failing Endpoints: NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Total Number of Endpoints: NA
Total Number of Endpoints: NA
There are no user specified timing constraints.
Timing Summary - impl_1 (saved)
Type here to search
5:21 PM
3/11/2025


Lab3_A - [C:/Users/Student/Desktop/Bab_Vivado/Lab3_A/Lab3_A.xpr] - Vivado 2024.2
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lab3_top
Nets (7)
Leaf Cells (7)
Source File Properties
Enabled
Location:
C:/Users
General
Properties
Project Summary
Device
lab3_top-2.vhd
clkdivider-1.1.vhd
Design_name_wrapper.v
C:/Users/Student/Desktop/Bab_Vivado/Lab3_A/lab3_top-2.vhd
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3 use IEEE.NUMERIC_STD.ALL;
4
5
6 entity lab3_top is
7 Port (reset_pb : in STD_LOGIC;
8 sysclk : in STD_LOGIC;
9 led : out STD_LOGIC_VECTOR (3 downto 0);
10 sw : in std_logic_vector(3 downto 0);
11 uart_rx : in std_logic;
12 uart_tx : out std_logic
13);
14 end lab3_top;
15
16
17 architecture Behavioral of lab3_top is
18 signal ctr : unsigned(3 downto 0);
19 signal clk,rst,ena_2Hz : std_logic;
20
21
22 component clkdivider is
23 generic (divideby : natural := 2);
24 port (clk : in std_logic;
25 reset : in std_logic;
26 pulseout : out std_logic);
27 end component;
28
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Design Timing Summary
Methodology Summary
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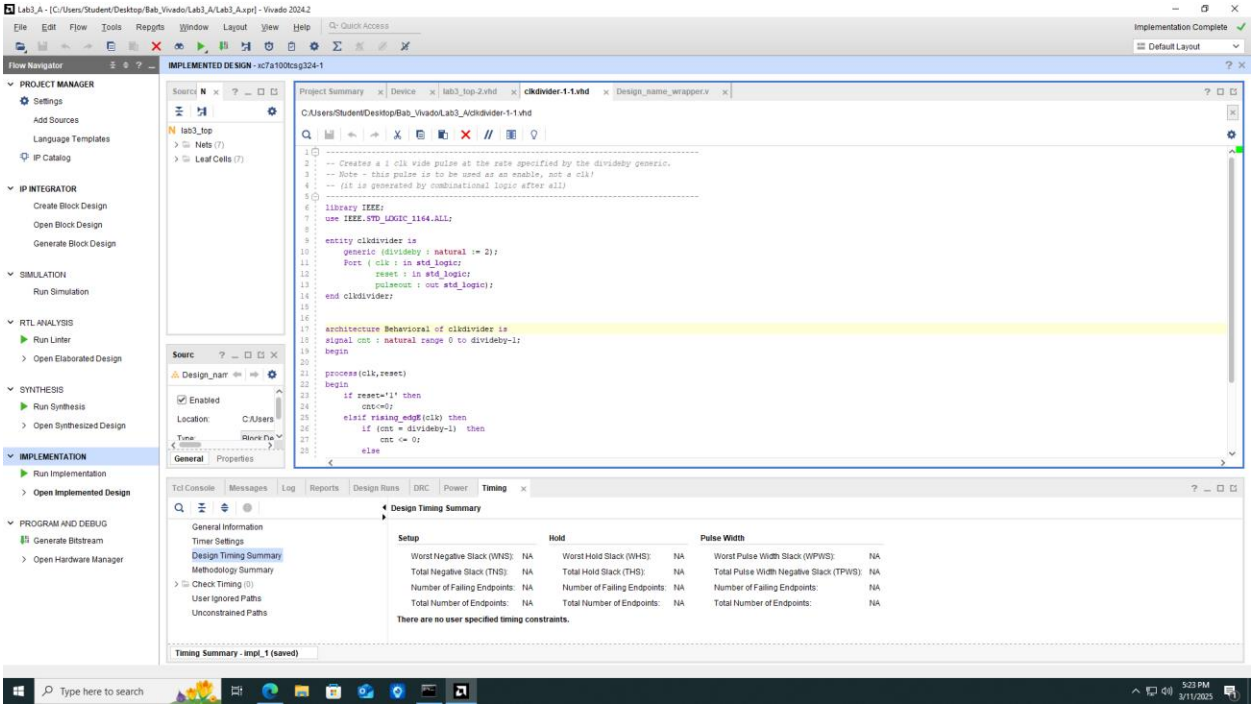
Unconstrained Paths
Setup
Hold
Pulse Width
Worst Negative Slack (WNS): NA
Worst Hold Slack (WHS): NA
Worst Pulse Width Slack (WPWS): NA
Total Negative Slack (TNS): NA
Total Hold Slack (THS): NA
Total Pulse Width Negative Slack (TPWS): NA
Number of Failing Endpoints: NA
Number of Failing Endpoints: NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Total Number of Endpoints: NA
Total Number of Endpoints: NA
There are no user specified timing constraints.
Timing Summary - impl_1 (saved)
Type here to search
5:23 PM
3/11/2025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clkdivider-1-1.vhd
Design_name_wrapper.v
C:/Users/Student/Desktop/Bab_Vivado/Lab3_A/clkdivider-1-1.vhd
-- Creates a 1 clk vide pulse at the rate specified by the dividedby generic.
-- Note - this pulse is to be used as an enable, not a clk!
-- (it is generated by combinational logic after all)
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity clkdivider is
generic (dividedby : natural := 2);
Port (clk : in std_logic;
reset : in std_logic;
pulseout : out std_logic);
end clkdivider;
architecture Behavioral of clkdivider is
signal cnt : natural range 0 to dividedby-1;
begin
process(clk,reset)
begin
if reset='1' then
cnt<=0;
elsif rising_edge(clk) then
if (cnt = dividedby-1) then
cnt <= 0;
else
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Total Pulse Width Negative Slack (TPWS): NA
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Number of Failing Endpoints: NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
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Total Number of Endpoints: NA
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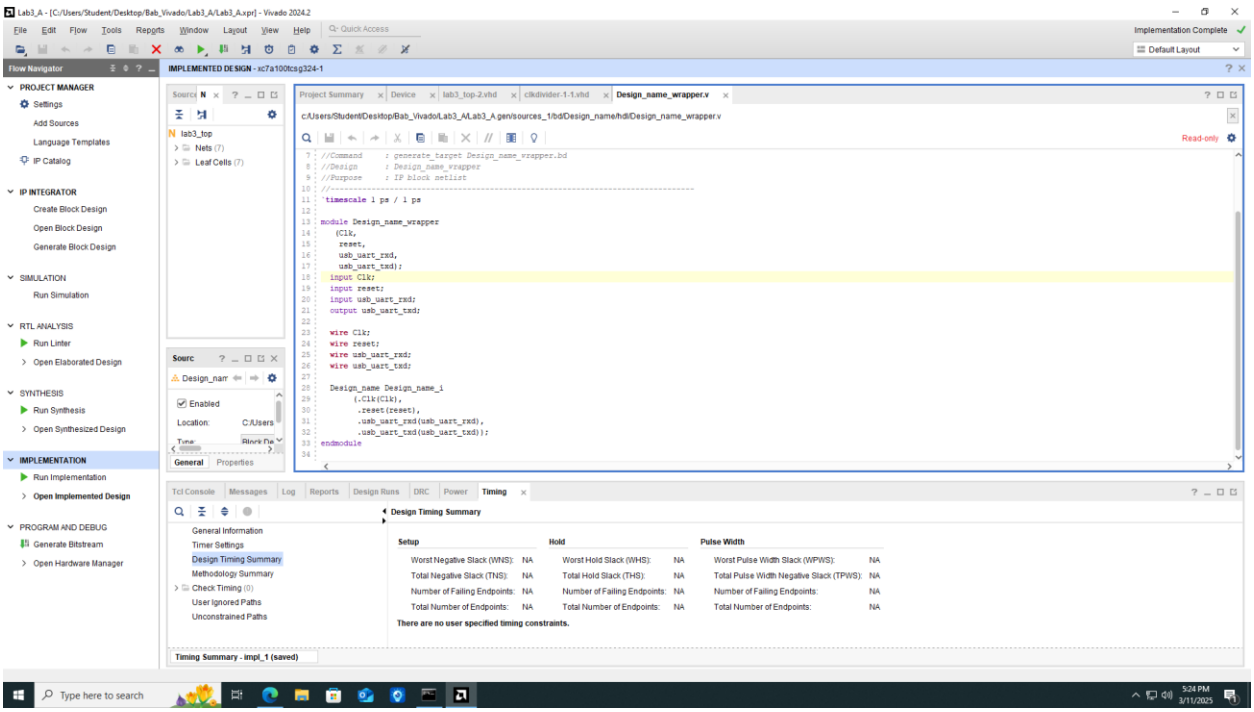
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Leaf Cells (7)
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clkdivider-1-1.vhd
Design_name_wrapper.v
c:/Users/Student/Desktop/Bab_Vivado/Lab3_A/Lab3_A.gen/sources_1/bd/Design_name/hdl/Design_name_wrapper.v
Read-only
//Command : generate_target Design_name_wrapper.bd
//Design : Design_name_wrapper
//Purpose : IP block netlist
`timescale 1 ps / 1 ps
module Design_name_wrapper
(Clk,
reset,
usb_uart_rxd,
usb_uart_txd);
input Clk;
input reset;
input usb_uart_rxd;
output usb_uart_txd;
wire Clk;
wire reset;
wire usb_uart_rxd;
wire usb_uart_txd;
Design_name Design_name_i
(.Clk(Clk),
.reset(reset),
.usb_uart_rxd(usb_uart_rxd),
.usb_uart_txd(usb_uart_txd));
endmodule
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Number of Failing Endpoints: NA
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Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Total Number of Endpoints: NA
Total Number of Endpoints: NA
There are no user specified timing constraints.
Timing Summary - impl_1 (saved)
Type here to search
5:24 PM
3/11/2025

Conclusion

The Objective of the Lab was met the program was run on hardware as well with the successful out put.