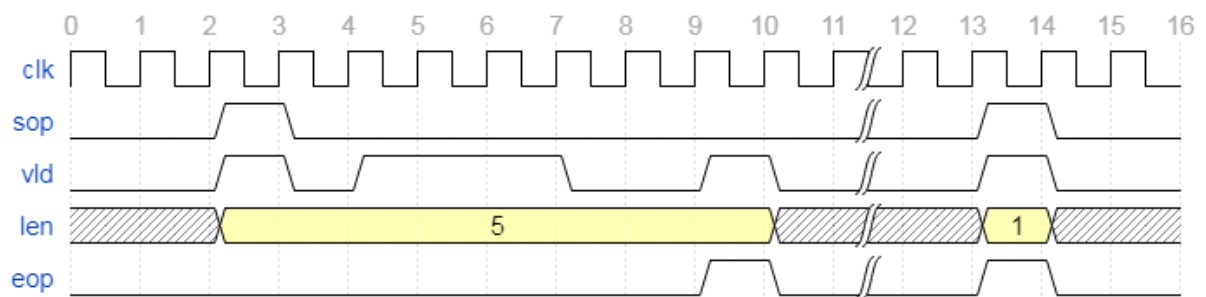


HW1

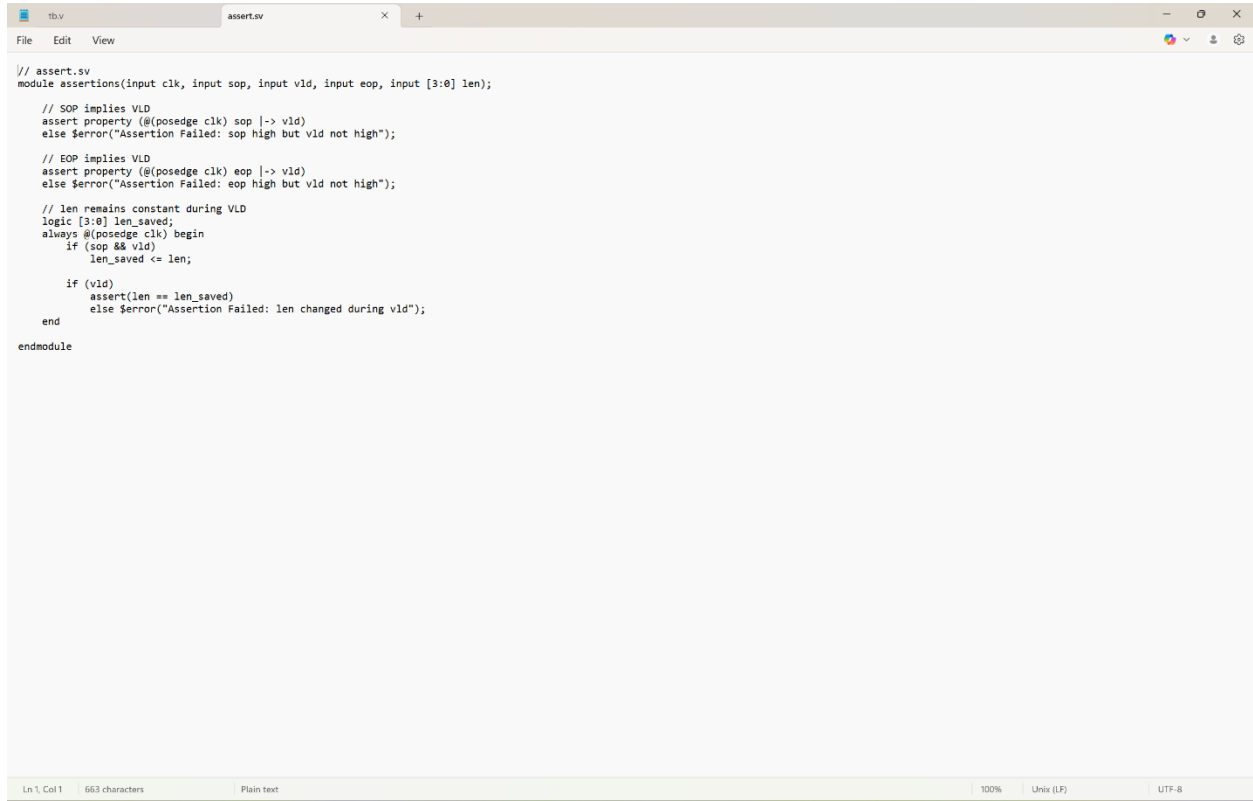
Submitted by: Bab Jan

Class: VLSIX.411

Study the attached [protocol.png](#) and write assertion test plan



Kindly see the below screen shots;



The screenshot shows a text editor window with a single tab titled 'assert.v'. The editor contains Verilog code for an assertions module. The code defines inputs for clock (clk), start of packet (sop), valid data (vld), end of packet (eop), and a 4-bit length (len). It includes two assertions: one for SOP implies VLD and another for EOP implies VLD. Additionally, it ensures the length remains constant during valid data by comparing the current length with a saved value. The status bar at the bottom indicates the cursor is at line 1, column 1, the file is 663 characters long, and it is using UTF-8 encoding.

```
// assert.v
module assertions(input clk, input sop, input vld, input eop, input [3:0] len);

    // SOP implies VLD
    assert property (@(posedge clk) sop |-> vld)
    else $error("Assertion Failed: sop high but vld not high");

    // EOP implies VLD
    assert property (@(posedge clk) eop |-> vld)
    else $error("Assertion Failed: eop high but vld not high");

    // len remains constant during VLD
    logic [3:0] len_saved;
    always @(posedge clk) begin
        if (sop && vld)
            len_saved <= len;

        if (vld)
            assert(len == len_saved)
            else $error("Assertion Failed: len changed during vld");
    end
endmodule
```

Ln 1, Col 1 | 663 characters | Plain text | 100% | Unix (LF) | UTF-8

```
tb.v x assert.v File.vlist Protocol.v run_vcs +
File Edit View

// tb.v
`timescale 1ns/1ps

module tb;

reg clk = 0;
always #5 clk = ~clk; // 10ns clock period

wire sop, vld, eop;
wire [3:0] len;

protocol dut (
    .clk(clk),
    .sop(sop),
    .vld(vld),
    .eop(eop),
    .len(len)
);

assertions a (
    .clk(clk),
    .sop(sop),
    .vld(vld),
    .eop(eop),
    .len(len)
);

initial begin
    $vcdplusfile("vcdplus.vpd");
    $vcdpluson(0, tb);
    #200 $finish;
end

endmodule
```

```
Ln 35, Col 1 423 characters Plain text 100% Unix (LF) UTF-8

tb.v assert.v File.vlist Protocol.v x +
File Edit View

// protocol.v
module protocol (
    input wire clk,
    output reg sop, vld, eop,
    output reg [3:0] len
);

reg [3:0] counter = 0;

always @(posedge clk) begin
    case ($time)
        20: begin // cycle 2
            sop <= 1;
            vld <= 1;
            len <= 5;
            counter <= 5;
            eop <= 0;
        end
        30,40,50: begin
            sop <= 0;
            vld <= 1;
            counter <= counter - 1;
            eop <= 0;
        end
        60: begin
            sop <= 0;
            vld <= 1;
            counter <= 0;
            eop <= 1;
        end
        130: begin // cycle 13
            sop <= 1;
            vld <= 1;
            len <= 1;
            counter <= 1;
            eop <= 0;
        end
        140: begin
            sop <= 0;
            vld <= 1;
            counter <= 0;
            eop <= 1;
        end
        default: begin
            sop <= 0;
            vld <= 0;
            len <= 0;
            eop <= 0;
        end
    endcase
end

endmodule

Ln 1, Col 1 1,026 characters Plain text 100% Unix (LF) UTF-8
```

tb.vassert.svFile.vlist

FileEditView

```
protocol.v
tb.v
assert.sv
```

Ln 4, Col 126 charactersPlain text100%Unix (LF)UTF-8

tb.vassert.svFile.vlistProtocol.vrun_vcs

FileEditView

H1B I A

Ln 1, Col 1153 charactersPlain text100%Unix (LF)UTF-8

```
#!/bin/bash
vcs -l compile.log -sverilog -lca -debug_all -full64 -timescale=1ns/1ps -f File.vlist
./simv -l sim.log +vcs+lic+wait
dve -vpd vcdplus.vpd &
```

HW1

OneDriveBab - PersonalDesktopSystem Verilog Assertion and Formal VerificationLinux FilesHW1Search HW1

NewSortViewDetails

Name	Status	Date modified	Type	Size
asset.sv	✓	7/28/2025 2:20 PM	SV File	1 KB
File.vlist	✓	7/28/2025 2:23 PM	VLIST File	1 KB
hw1	✓	7/25/2025 12:04 AM	PNG File	15 KB
Protocol.v	✓	7/28/2025 2:19 PM	V File	2 KB
run_vcs	✓	7/28/2025 2:23 PM	File	1 KB
tb.v	✓	7/28/2025 2:21 PM	V File	1 KB

6 items1 item selected663 bytesAvailable on this device