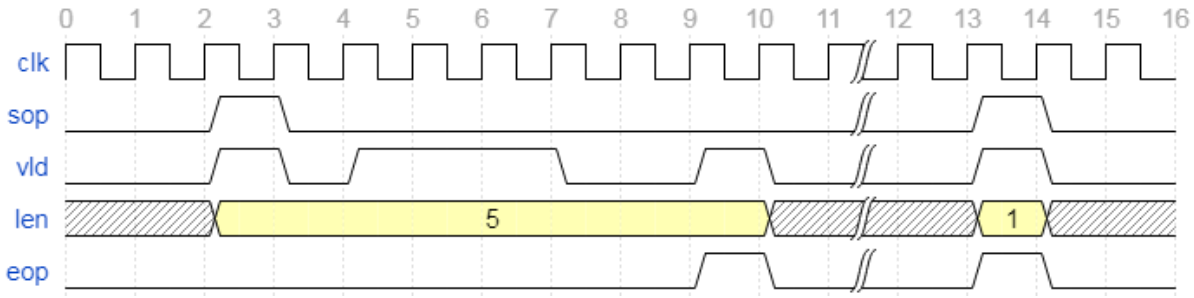
HW1

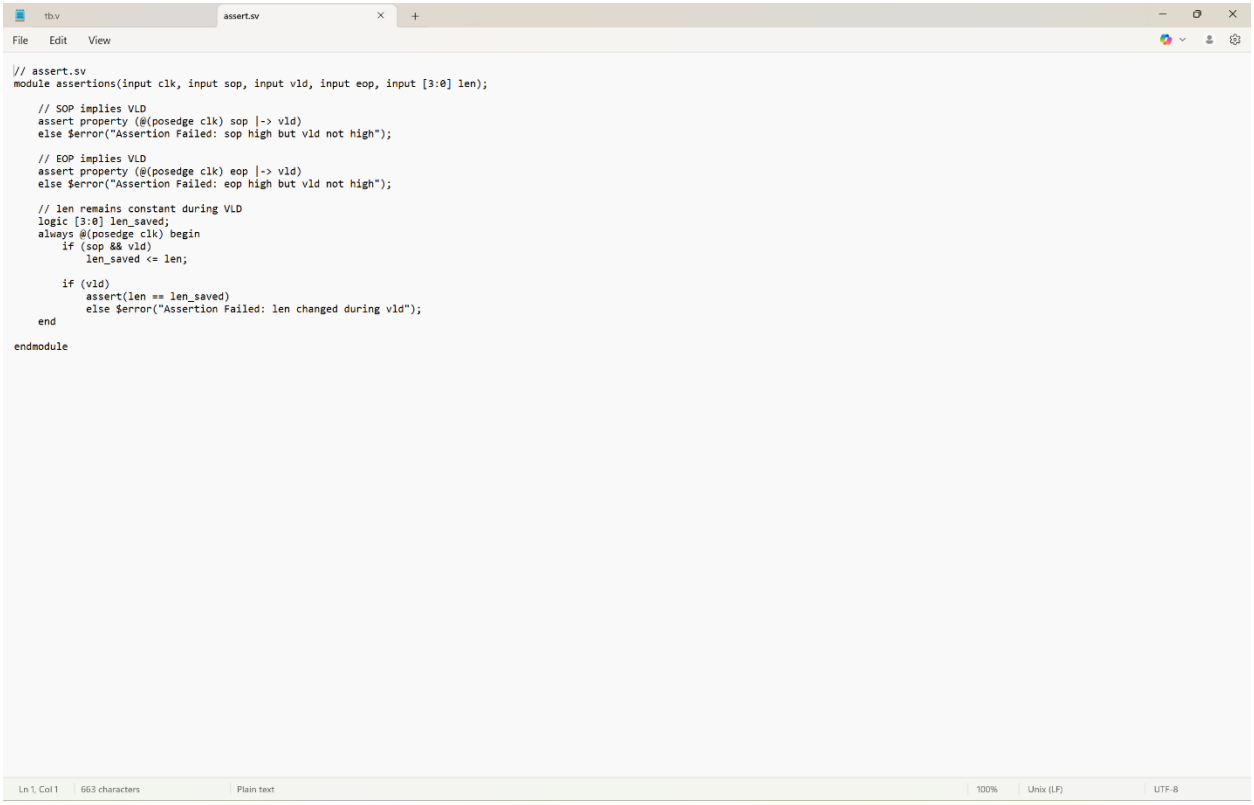
Submitted by: Bab Jan

Class: VLSIX.411

Study the attached protocol.png and write assertion test plan



Kindly see the below screen shots;



tb.v | assert.sv | File.vlist | Protocol.v | run_vcs

File Edit View

```
// tb.v
`timescale 1ns/1ps

module tb;

reg clk = 0;
always #5 clk = ~clk; // 10ns clock period

wire sop, vld, eop;
wire [3:0] len;

protocol dut (
    .clk(clk),
    .sop(sop),
    .vld(vld),
    .eop(eop),
    .len(len)
);

assertions a (
    .clk(clk),
    .sop(sop),
    .vld(vld),
    .eop(eop),
    .len(len)
);

initial begin
    $vcdplusfile("vcdplus.vpd");
    $vcdpluson(0, tb);
    #200 $finish;
end

endmodule
```

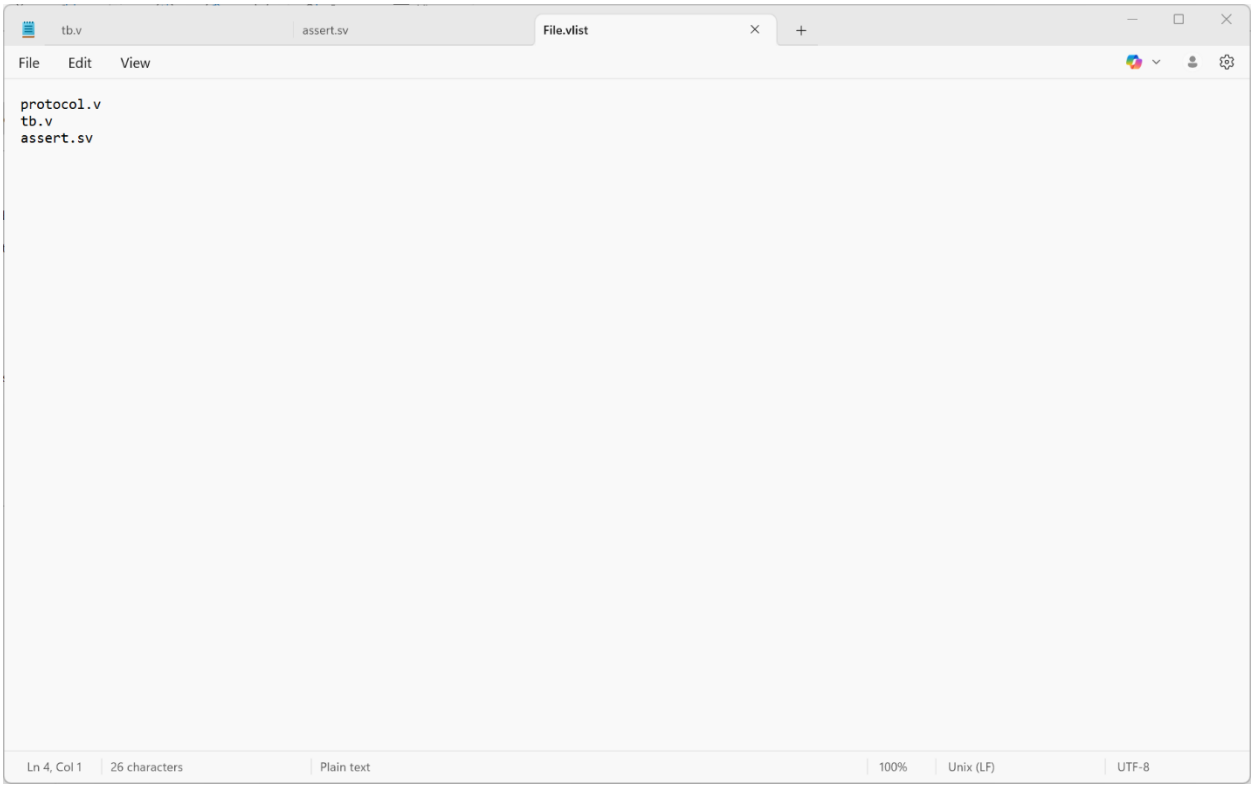
Ln 35, Col 1 | 423 characters | Plain text | 100% | Unix (LF) | UTF-8

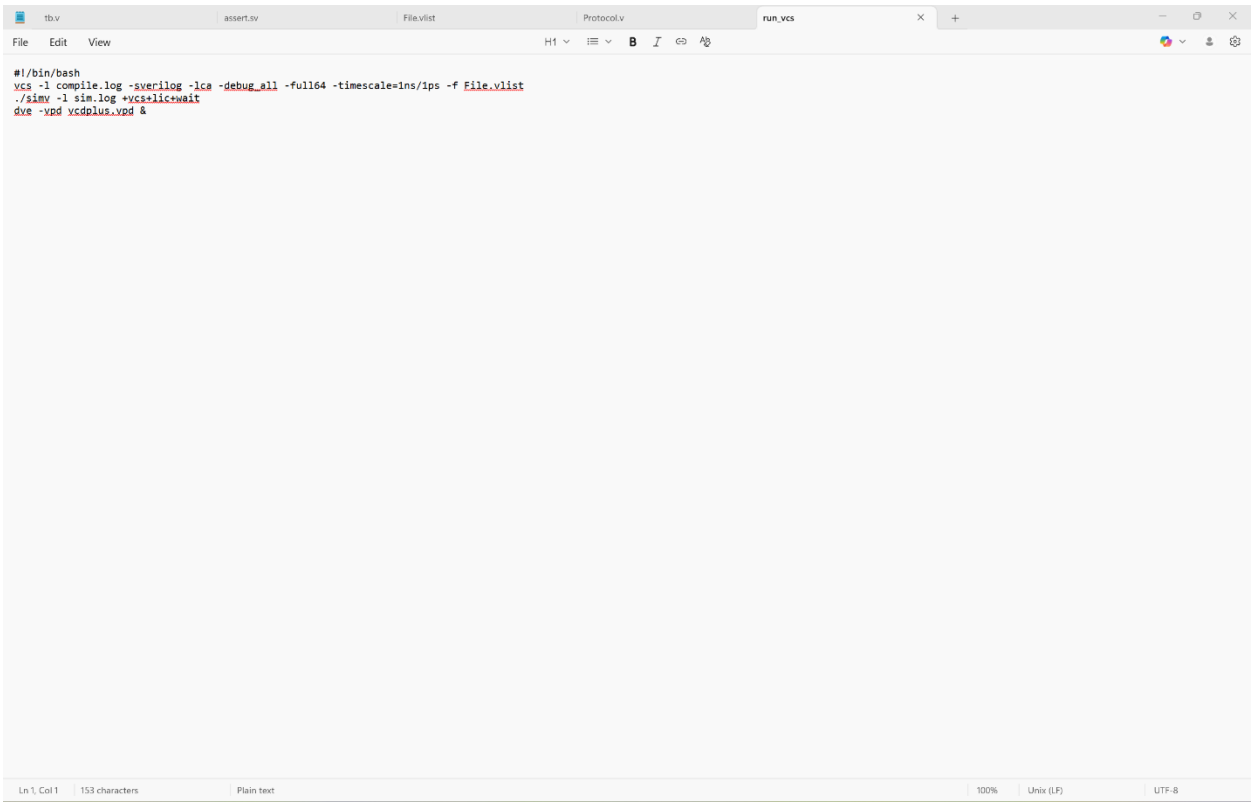
tb.v | assert.sv | File.vlist | Protocol.v

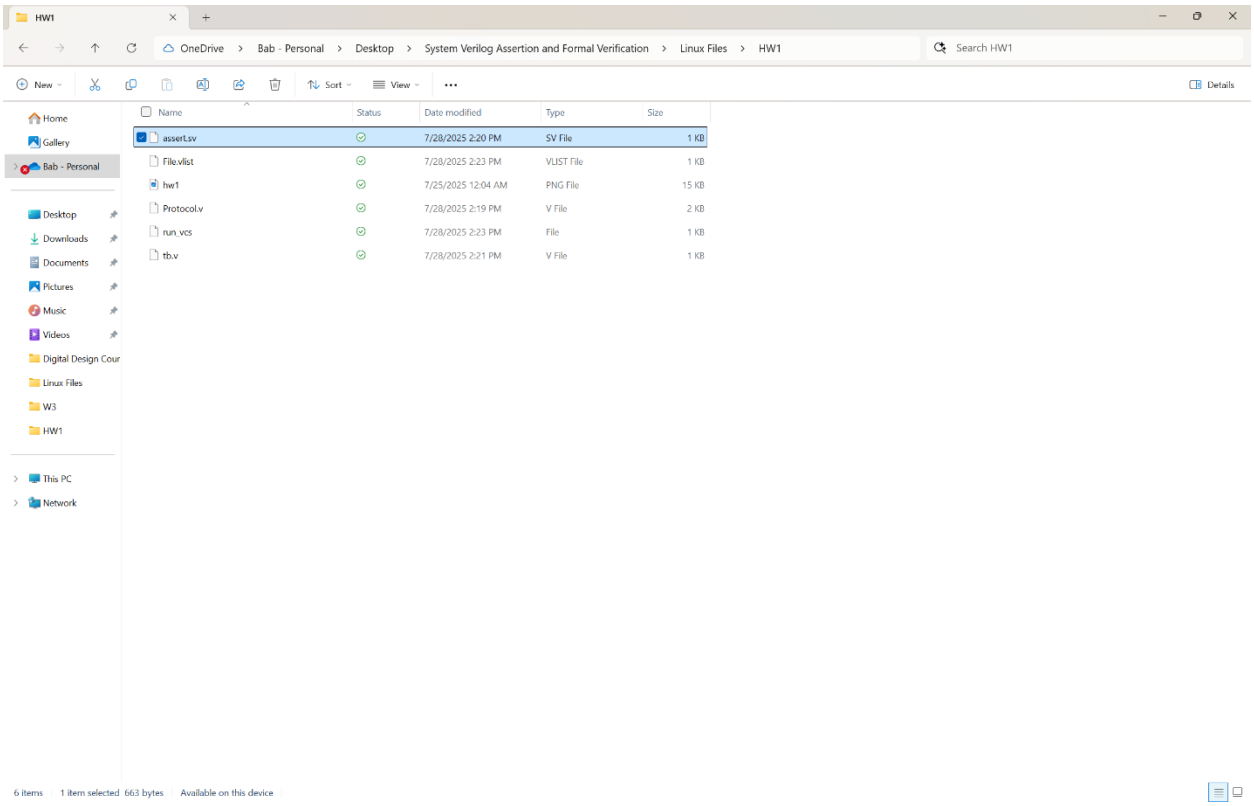
File Edit View

```
// protocol.v
module protocol (
    input wire clk,
    output reg sop, vld, eop,
    output reg [3:0] len
);

reg [3:0] counter = 0;

always @(posedge clk) begin
    case ($time)
        20: begin  // cycle 2
            sop <= 1;
            vld <= 1;
            len <= 5;
            counter <= 5;
            eop <= 0;
        end
        30,40,50: begin
            sop <= 0;
            vld <= 1;
            counter <= counter - 1;
            eop <= 0;
        end
        60: begin
            sop <= 0;
            vld <= 1;
            counter <= 0;
            eop <= 1;
        end
        130: begin // cycle 13
            sop <= 1;
            vld <= 1;
            len <= 1;
            counter <= 1;
            eop <= 0;
        end
        140: begin
            sop <= 0;
            vld <= 1;
            counter <= 0;
            eop <= 1;
        end
        default: begin
            sop <= 0;
            vld <= 0;
            len <= 0;
            eop <= 0;
        end
    endcase
end

endmodule
```

Ln 1, Col 1 | 1,026 characters | Plain text | 100% | Unix (LF) | UTF-8


tb.v
assert.sv
File.vlist
File
Edit
View
protocol.v
tb.v
assert.sv
Ln 4, Col 1
26 characters
Plain text
100%
Unix (LF)
UTF-8


tb.v
assert.sv
File.vlist
Protocol.v
run_vcs
File Edit View
#!/bin/bash
vcs -l compile.log -sverilog -lca -debug_all -full64 -timescale=1ns/1ps -f File.vlist
./simv -l sim.log +vcs+lic+wait
dve -vpd vcdplus.vpd &
Ln 1, Col 1
153 characters
Plain text
100%
Unix (LF)
UTF-8


HW1
OneDrive › Bab - Personal › Desktop › System Verilog Assertion and Formal Verification › Linux Files › HW1
Search HW1
New
Sort
View
Details
Home
Gallery
Bab - Personal
Desktop
Downloads
Documents
Pictures
Music
Videos
Digital Design Cour
Linux Files
W3
HW1
This PC
Network
Name
Status
Date modified
Type
Size
assert.sv 7/28/2025 2:20 PM SV File 1 KB
File.vlist 7/28/2025 2:23 PM VLIST File 1 KB
hw1 7/25/2025 12:04 AM PNG File 15 KB
Protocol.v 7/28/2025 2:19 PM V File 2 KB
run_vcs 7/28/2025 2:23 PM File 1 KB
tb.v 7/28/2025 2:21 PM V File 1 KB
6 items
1 item selected 663 bytes
Available on this device