XQuartz Applications Edit Window Help Fri Dec 6 10:33 AM

X2GO-tc14154-62-1727925143_stDMATE_dp32

Applications Places System Fri Dec 6, 10:33

verilog7.v (~/Desktop/exam/question7) - Pluma

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verilog7.v

```verilog
module traffic_light_fsm (
    input clk,
    input reset_n, // Asynchronous active low reset
    output reg ns_green, ns_yellow, ns_red,
    output reg ew_green, ew_yellow, ew_red
);

    // State encoding
    parameter STATE_NS_GREEN  = 2'b00;
    parameter STATE_NS_YELLOW = 2'b01;
    parameter STATE_EW_GREEN  = 2'b10;
    parameter STATE_EW_YELLOW = 2'b11;

    reg [1:0] current_state, next_state; // Current and next states
    reg [6:0] timer; // Timer for counting clock cycles (0-127)

    // State transition and timer logic
    always @(posedge clk or negedge reset_n) begin
        if (!reset_n) begin
            current_state <= STATE_NS_GREEN;
            timer <= 7'd0;
        end else begin
            current_state <= next_state;
            timer <= (timer == 7'd63 || timer == 7'd3) ? 7'd0 : timer + 1;
        end
    end

    // Next state logic
    always @(*) begin
        case (current_state)
            STATE_NS_GREEN:
                next_state = (timer == 7'd63) ? STATE_NS_YELLOW : STATE_NS_GREEN;
            STATE_NS_YELLOW:
                next_state = (timer == 7'd3) ? STATE_EW_GREEN : STATE_NS_YELLOW;
            STATE_EW_GREEN:
                next_state = (timer == 7'd63) ? STATE_EW_YELLOW : STATE_EW_GREEN;
            STATE_EW_YELLOW:
                next_state = (timer == 7'd3) ? STATE_NS_GREEN : STATE_EW_YELLOW;
            default:
                next_state = STATE_NS_GREEN;
        endcase
    end

    // Output logic
    always @(*) begin
        // Default all outputs to off
        ns_green = 0; ns_yellow = 0; ns_red = 0;
        ew_green = 0; ew_yellow = 0; ew_red = 0;

        case (current_state)
            STATE_NS_GREEN: begin
                ns_green = 1;
                ns_red = 0;
                ew_red = 1;
            end
            STATE_NS_YELLOW: begin
                ns_yellow = 1;
                ns_red = 0;
                ew_red = 1;
            end
```

Verilog Tab Width: 4 Ln 1, Col 1 INS

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```
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Warning-[LCA_FEATURES_ENABLED] Usage warning
  LCA features enabled by '-lca' argument on the command line.  For more
  information regarding list of LCA features please refer to Chapter "LCA
  features" in the VCS Release Notes


Warning-[DEBUG_DEP] Option will be deprecated
  The option '-debug_all' will be deprecated in a future release.  Please use
  '-debug_acc+all -debug_region+cell+encrypt' instead.

Parsing design file 'verilog7.v'
Parsing design file 'testbench7.v'
Top Level Modules:
       traffic_light_fsm_tb
TimeScale is 1 ns / 1 ps
Starting vcs inline pass...

1 module and 0 UDP read.
recompiling module traffic_light_fsm_tb
rm -f _cuarc*.so _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
if [ -x ../simv ]; then chmod a-x ../simv; fi
g++  -o ../simv      -rdynamic  -Wl,-rpath='$ORIGIN'/simv.daidir -Wl,-rpath=./simv.daidir -Wl,-rpath=/usr/synopsys
/vcs/U-2023.03-SP2/linux64/lib -L/usr/synopsys/vcs/U-2023.03-SP2/linux64/lib  -Wl,-rpath-link=./  /usr/lib64/libnu
ma.so.1   objs/amcQw_d.o   _28731_archive_1.so  -SIM_l,o      rmapats_mop.o rmapats.o rmar.o rmar_nd.o  rmar_llvm_
0_1.o rmar_llvm_0_0.o          -lvirsim -lerrorinf -lsnpsmalloc -lvfs    -lvcsnew -lsimprofile -luclinative /usr
/synopsys/vcs/U-2023.03-SP2/linux64/lib/vcs_tls.o   -Wl,-whole-archive  -lvcsucli    -Wl,-no-whole-archive
  /usr/synopsys/vcs/U-2023.03-SP2/linux64/lib/vcs_save_restore_new.o -ldl  -lc -lm -lpthread -ldl
../simv up to date
CPU time: .282 seconds to compile + .372 seconds to elab + .209 seconds to link
Info: [VCS_SAVE_RESTORE_INFO] ASLR (Address Space Layout Randomization) is detected on the machine. To enable $sav
e functionality, ASLR will be switched off and simv re-executed.
Please use '-no_save' simv switch to avoid re-execution or '-suppress=ASLR_DETECTED_INFO' to suppress this message

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VCD+ Writer U-2023.03-SP2_Full64 Copyright (c) 1991-2023 by Synopsys Inc.
Time=0 | NS: Green=1, Yellow=0, Red=0 | EW: Green=0, Yellow=0, Red=1
$finish called from file "testbench7.v", line 38.
$finish at simulation time                 515000
           V C S   S i m u l a t i o n   R e p o r t
Time: 515000 ps
CPU Time:      0.390 seconds;       Data structure size:   0.0Mb
Fri Dec  6 10:32:15 2024
[tc14154@VLSI03 question7]$
```

Mate Terminal question7 verilog7.v (~/Desktop...

XQuartz Applications Edit Window Help Fri Dec 6 10:33 AM

X2GO-tc14154-62-1727925143_stDMATE_dp32

Applications Places System Fri Dec 6, 10:33

verilog7.v (~/Desktop/exam/question7) - Pluma

File Edit View Search Tools Documents Help

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verilog7.v

```verilog
    // State transition and timer logic
    always @(posedge clk or negedge reset_n) begin
        if (!reset_n) begin
            current_state <= STATE_NS_GREEN;
            timer <= 7'd0;
        end else begin
            current_state <= next_state;
            timer <= (timer == 7'd63 || timer == 7'd3) ? 7'd0 : timer + 1;
        end
    end

    // Next state logic
    always @(*) begin
        case (current_state)
            STATE_NS_GREEN:
                next_state = (timer == 7'd63) ? STATE_NS_YELLOW : STATE_NS_GREEN;
            STATE_NS_YELLOW:
                next_state = (timer == 7'd3) ? STATE_EW_GREEN : STATE_NS_YELLOW;
            STATE_EW_GREEN:
                next_state = (timer == 7'd63) ? STATE_EW_YELLOW : STATE_EW_GREEN;
            STATE_EW_YELLOW:
                next_state = (timer == 7'd3) ? STATE_NS_GREEN : STATE_EW_YELLOW;
            default:
                next_state = STATE_NS_GREEN;
        endcase
    end

    // Output logic
    always @(*) begin
        // Default all outputs to off
        ns_green = 0; ns_yellow = 0; ns_red = 0;
        ew_green = 0; ew_yellow = 0; ew_red = 0;

        case (current_state)
            STATE_NS_GREEN: begin
                ns_green = 1;
                ns_red = 0;
                ew_red = 1;
            end
            STATE_NS_YELLOW: begin
                ns_yellow = 1;
                ns_red = 0;
                ew_red = 1;
            end
            STATE_EW_GREEN: begin
                ns_red = 1;
                ew_green = 1;
                ew_red = 0;
            end
            STATE_EW_YELLOW: begin
                ns_red = 1;
                ew_yellow = 1;
                ew_red = 0;
            end
        endcase
    end

endmodule
```

Verilog Tab Width: 4 Ln 1, Col 1 INS

Mate Terminal

File Edit View Search Terminal Help

```
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Parsing design file 'verilog7.v'
Parsing design file 'testbench7.v'
Top Level Modules:
       traffic_light_fsm_tb
TimeScale is 1 ns / 1 ps
Starting vcs inline pass...

1 module and 0 UDP read.
recompiling module traffic_light_fsm_tb
rm -f _cuarc*.so _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
if [ -x ../simv ]; then chmod a-x ../simv; fi
g++  -o ../simv      -rdynamic  -Wl,-rpath='$ORIGIN'/simv.daidir -Wl,-rpath=./simv.daidir -Wl,-rpath=/usr/synopsys
/vcs/U-2023.03-SP2/linux64/lib -L/usr/synopsys/vcs/U-2023.03-SP2/linux64/lib  -Wl,-rpath-link=./  /usr/lib64/libnu
ma.so.1   objs/amcQw_d.o   _28731_archive_1.so  -SIM_l,o      rmapats_mop.o rmapats.o rmar.o rmar_nd.o  rmar_llvm_
0_1.o rmar_llvm_0_0.o          -lvirsim -lerrorinf -lsnpsmalloc -lvfs    -lvcsnew -lsimprofile -luclinative /usr
/synopsys/vcs/U-2023.03-SP2/linux64/lib/vcs_tls.o   -Wl,-whole-archive  -lvcsucli    -Wl,-no-whole-archive
  /usr/synopsys/vcs/U-2023.03-SP2/linux64/lib/vcs_save_restore_new.o -ldl  -lc -lm -lpthread -ldl
../simv up to date
CPU time: .282 seconds to compile + .372 seconds to elab + .209 seconds to link
Info: [VCS_SAVE_RESTORE_INFO] ASLR (Address Space Layout Randomization) is detected on the machine. To enable $sav
e functionality, ASLR will be switched off and simv re-executed.
Please use '-no_save' simv switch to avoid re-execution or '-suppress=ASLR_DETECTED_INFO' to suppress this message

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VCD+ Writer U-2023.03-SP2_Full64 Copyright (c) 1991-2023 by Synopsys Inc.
Time=0 | NS: Green=1, Yellow=0, Red=0 | EW: Green=0, Yellow=0, Red=1
$finish called from file "testbench7.v", line 38.
$finish at simulation time                 515000
           V C S   S i m u l a t i o n   R e p o r t
Time: 515000 ps
CPU Time:      0.390 seconds;       Data structure size:   0.0Mb
Fri Dec  6 10:32:15 2024
[tc14154@VLSI03 question7]$
```
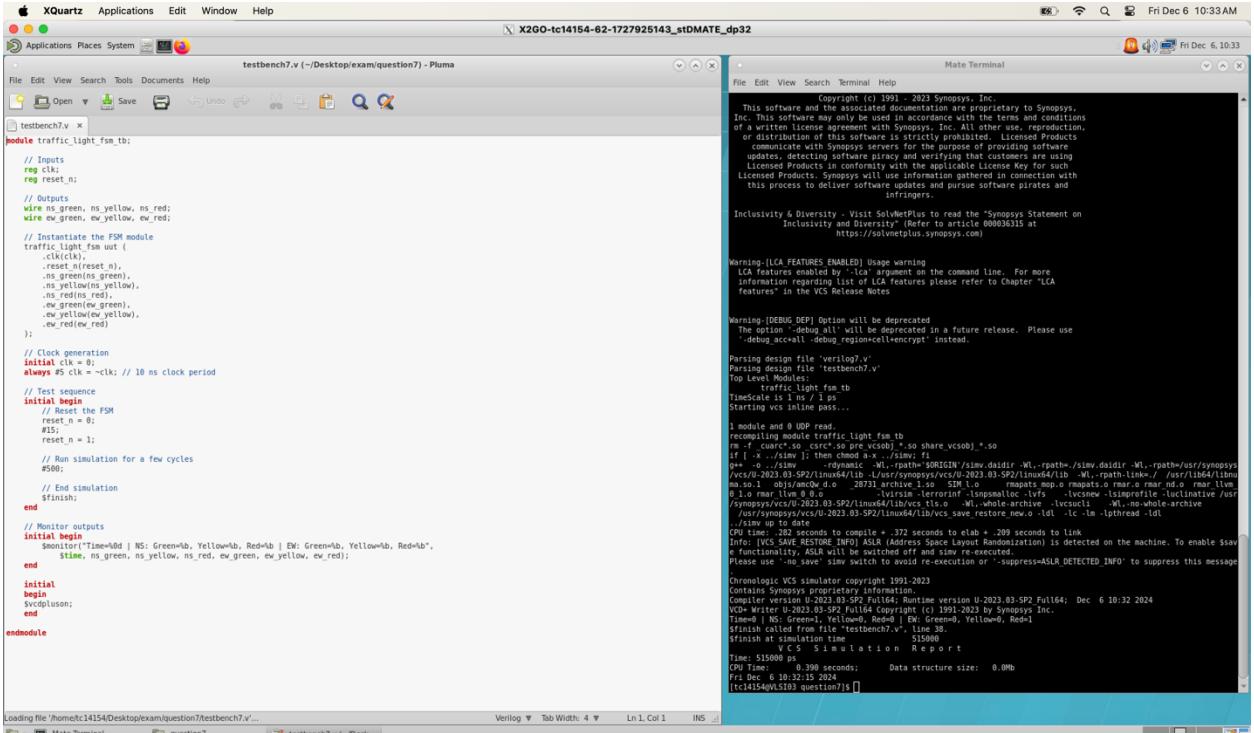

Mate Terminal question7 verilog7.v (~/Desktop...


XQuartz Applications Edit Window Help
Fri Dec 6 10:33 AM
X2GO-tc14154-62-1727925143_stDMATE_dp32
testbench7.v (~/Desktop/exam/question7) - Pluma
File Edit View Search Tools Documents Help
Open Save Undo
testbench7.v
module traffic_light_fsm_tb;
// Inputs
reg clk;
reg reset_n;
// Outputs
wire ns_green, ns_yellow, ns_red;
wire ew_green, ew_yellow, ew_red;
// Instantiate the FSM module
traffic_light_fsm uut (
.clk(clk),
.reset_n(reset_n),
.ns_green(ns_green),
.ns_yellow(ns_yellow),
.ns_red(ns_red),
.ew_green(ew_green),
.ew_yellow(ew_yellow),
.ew_red(ew_red)
);
// Clock generation
initial clk = 0;
always #5 clk = ~clk; // 10 ns clock period
// Test sequence
initial begin
// Reset the FSM
reset_n = 0;
#15;
reset_n = 1;
// Run simulation for a few cycles
#500;
// End simulation
$finish;
end
// Monitor outputs
initial begin
$monitor("Time=%0d | NS: Green=%b, Yellow=%b, Red=%b | EW: Green=%b, Yellow=%b, Red=%b",
$time, ns_green, ns_yellow, ns_red, ew_green, ew_yellow, ew_red);
end
initial
begin
$vcdpluson;
end
endmodule
Loading file '/home/tc14154/Desktop/exam/question7/testbench7.v'...
Verilog Tab Width: 4 Ln 1, Col 1 INS
Mate Terminal
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The option '-debug_all' will be deprecated in a future release. Please use '-debug_acc+all -debug_region+cell+encrypt' instead.
Parsing design file 'verilog7.v'
Parsing design file 'testbench7.v'
Top Level Modules:
traffic_light_fsm_tb
TimeScale is 1 ns / 1 ps
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module traffic_light_fsm_tb
rm -f _cuarc*.so _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
if [-x ../simv]; then chmod a-x ../simv; fi
g++ -o ../simv -rdynamic -Wl,-rpath='$ORIGIN'/simv.daidir -Wl,-rpath=./simv.daidir -Wl,-rpath=/usr/synopsys/vcs/U-2023.03-SP2/linux64/lib -L/usr/synopsys/vcs/U-2023.03-SP2/linux64/lib -Wl,-rpath-link=./ /usr/lib64/libnuma.so.1 objs/amcQw_d.o _28731_archive_1.so SIM_l.o rmapats.mop.o rmapats.o rmar.o rmar_nd.o rmar_llvm_0_1.o rmar_llvm_0_0.o -lvirsim -lerrorinf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -luclinative /usr/synopsys/vcs/U-2023.03-SP2/linux64/lib/vcs_tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive /usr/synopsys/vcs/U-2023.03-SP2/linux64/lib/vcs_save_restore_new.o -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .282 seconds to compile + .372 seconds to elab + .209 seconds to link
Info: [VCS_SAVE_RESTORE_INFO] ASLR (Address Space Layout Randomization) is detected on the machine. To enable $save functionality, ASLR will be switched off and simv re-executed.
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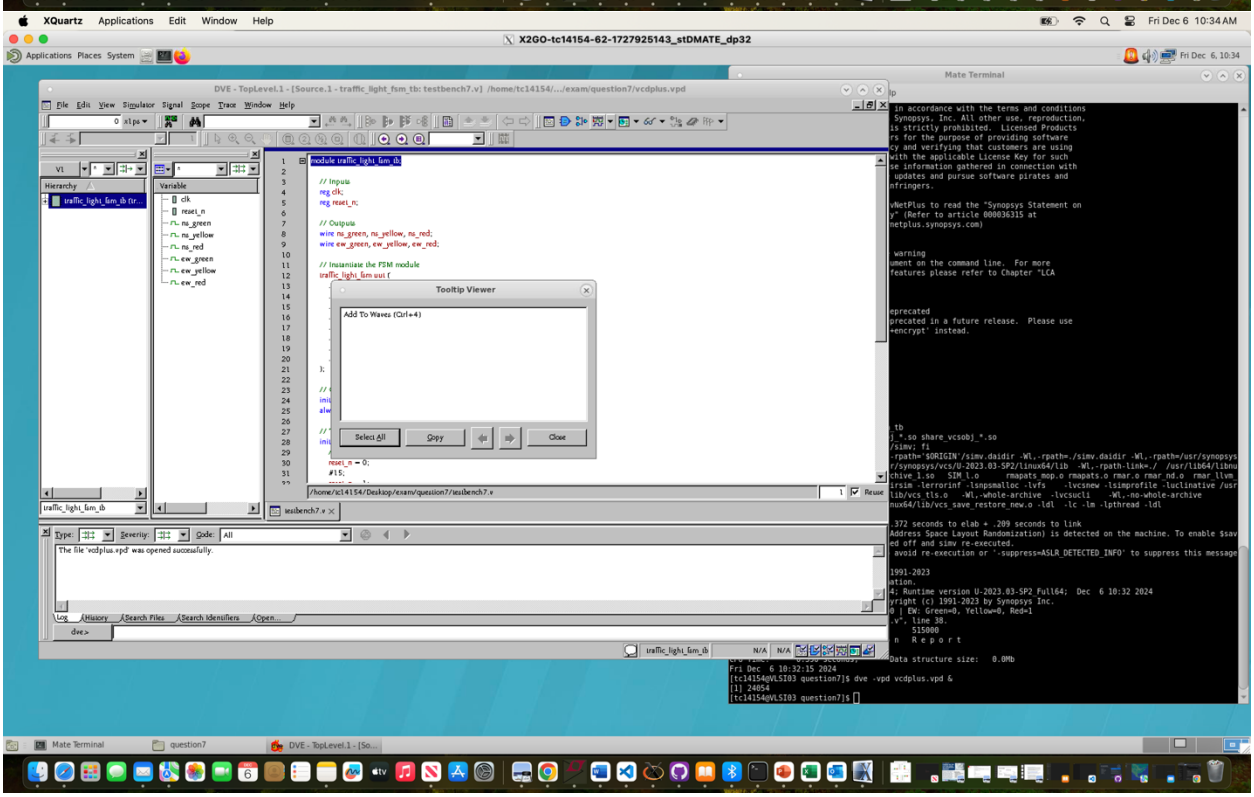
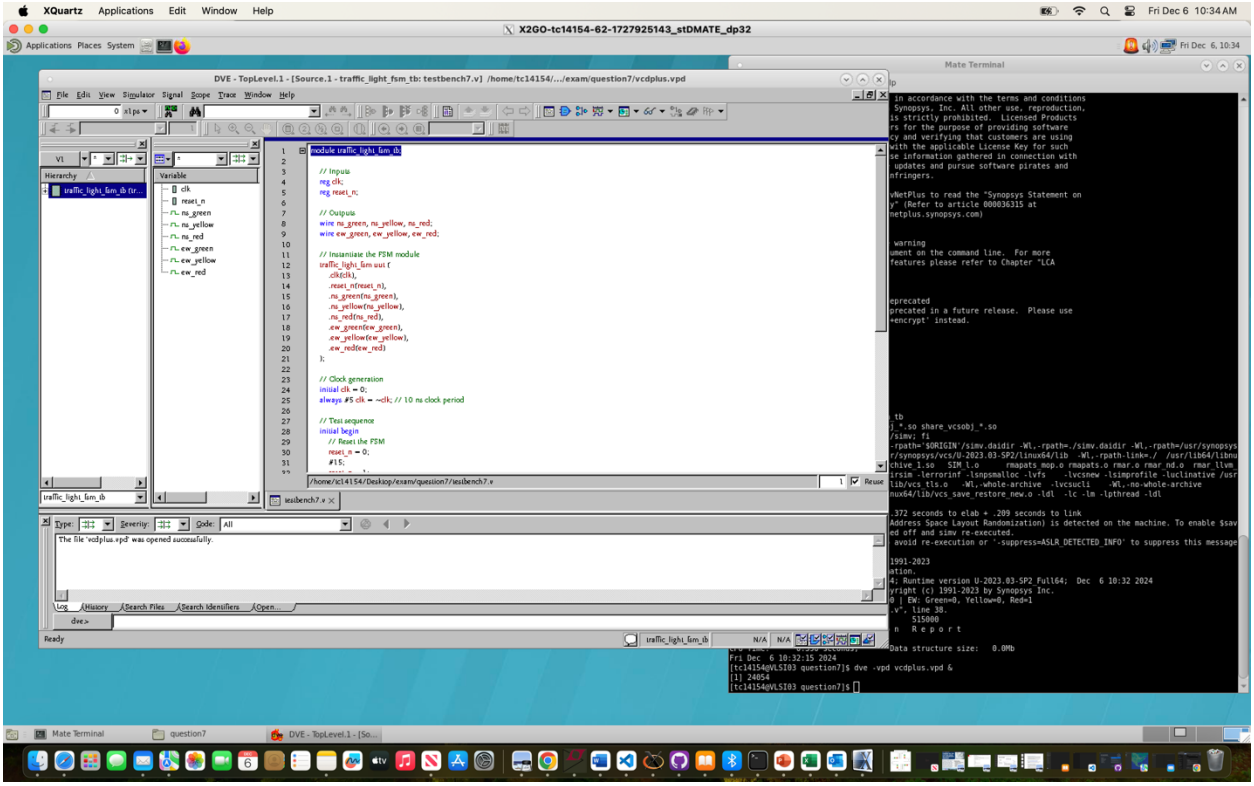
Time=0 | NS: Green=1, Yellow=0, Red=0 | EW: Green=0, Yellow=0, Red=1
$finish called from file "testbench7.v", line 38.
$finish at simulation time 515000
V C S S i m u l a t i o n R e p o r t
Time: 515000 ps
CPU Time: 0.390 seconds; Data structure size: 0.0Mb
Fri Dec 6 10:32:15 2024
[tc14154@VLSI03 question7]$


XQuartz Applications Edit Window Help
Fri Dec 6 10:34 AM
X2GO-tc14154-62-1727925143_stDMATE_dp32
DVE - TopLevel.1 - [Source.1 - traffic_light_fsm_tb: testbench7.v] /home/tc14154/.../exam/question7/vcdplus.vpd
File Edit View Simulator Signal Scope Trace Window Help
Hierarchy
traffic_light_fsm_tb tbr...
Variable
clk
reset_n
ns_green
ns_yellow
ns_red
ew_green
ew_yellow
ew_red
module traffic_light_fsm_tb;
// Inputs
reg clk;
reg reset_n;
// Outputs
wire ns_green, ns_yellow, ns_red;
wire ew_green, ew_yellow, ew_red;
// Instantiate the FSM module
traffic_light_fsm uut (
Tooltip Viewer
Add To Waves (Ctrl+4)
Select All
Copy
Close
/home/tc14154/Desktop/exam/question7/testbench7.v
testbench7.v
Type: Severity: Code: All
The file 'vcdplus.vpd' was opened successfully.
Log History Search Files Search Identifiers Open...
dve>
Mate Terminal
Fri Dec 6 10:32:15 2024
[tc14154@VLSI03 question7]$ dve -vpd vcdplus.vpd &
[1] 24054
[tc14154@VLSI03 question7]$


XQuartz Applications Edit Window Help
Fri Dec 6 10:34 AM
X2GO-tc14154-62-1727925143_stDMATE_dp32
DVE - TopLevel.1 - [Source.1 - traffic_light_fsm_tb: testbench7.v] /home/tc14154/.../exam/question7/vcdplus.vpd
File Edit View Simulator Signal Scope Trace Window Help
Hierarchy
traffic_light_fsm_tb (tr...
Variable
clk
reset_n
ns_green
ns_yellow
ns_red
ew_green
ew_yellow
ew_red
module traffic_light_fsm_tb;
// Inputs
reg clk;
reg reset_n;
// Outputs
wire ns_green, ns_yellow, ns_red;
wire ew_green, ew_yellow, ew_red;
// Instantiate the FSM module
traffic_light_fsm uut (
.clk(clk),
.reset_n(reset_n),
.ns_green(ns_green),
.ns_yellow(ns_yellow),
.ns_red(ns_red),
.ew_green(ew_green),
.ew_yellow(ew_yellow),
.ew_red(ew_red)
);
// Clock generation
initial clk = 0;
always #5 clk = ~clk; // 10 ns clock period
// Test sequence
initial begin
// Reset the FSM
reset_n = 0;
#15;
/home/tc14154/Desktop/exam/question7/testbench7.v
testbench7.v
Type: Severity: Code: All
The file 'vcdplus.vpd' was opened successfully.
Log History Search Files Search Identifiers Open...
dve>
Ready
traffic_light_fsm_tb
N/A
Mate Terminal
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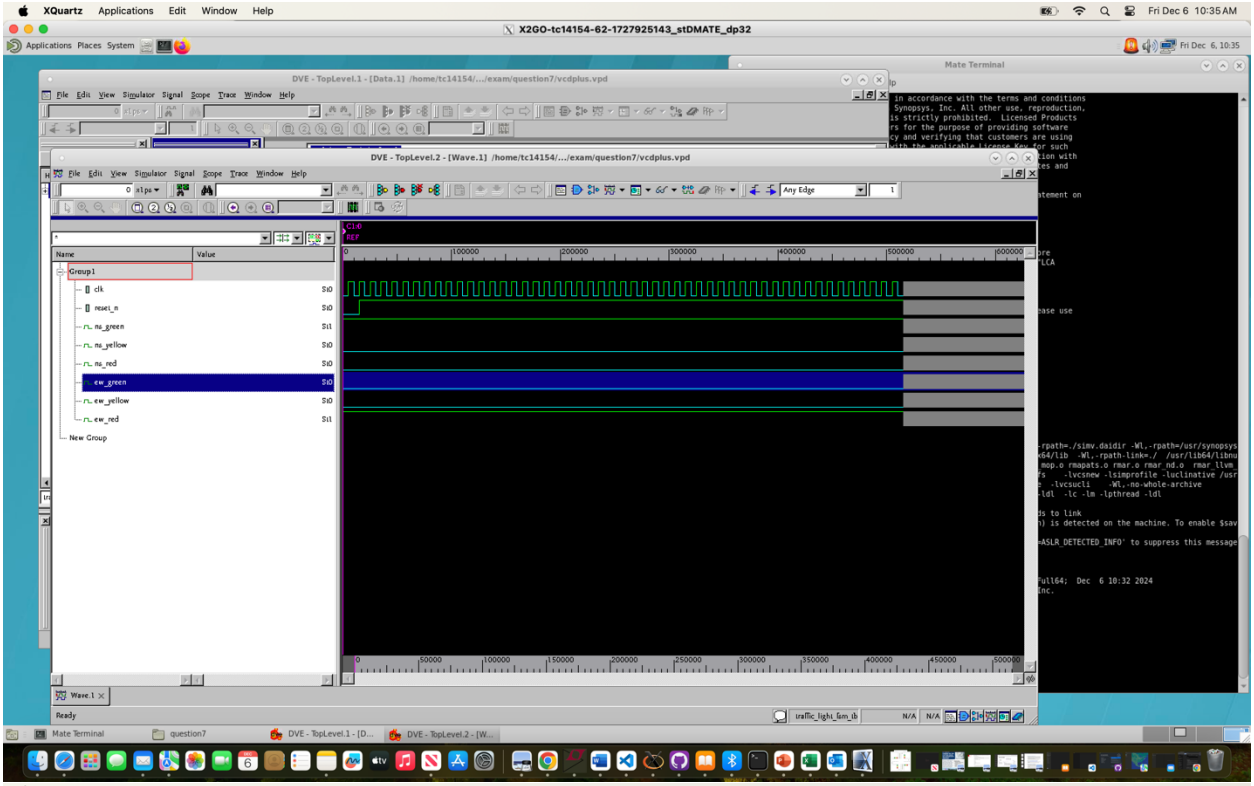
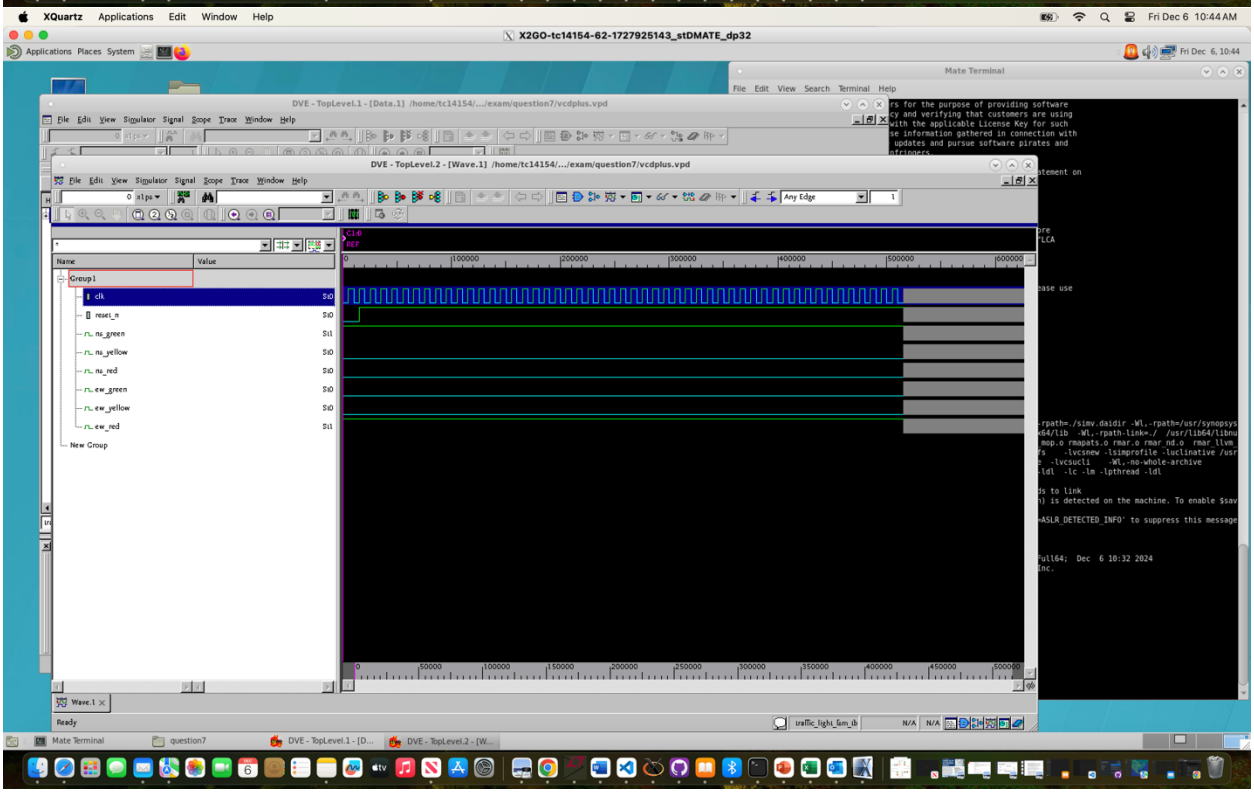
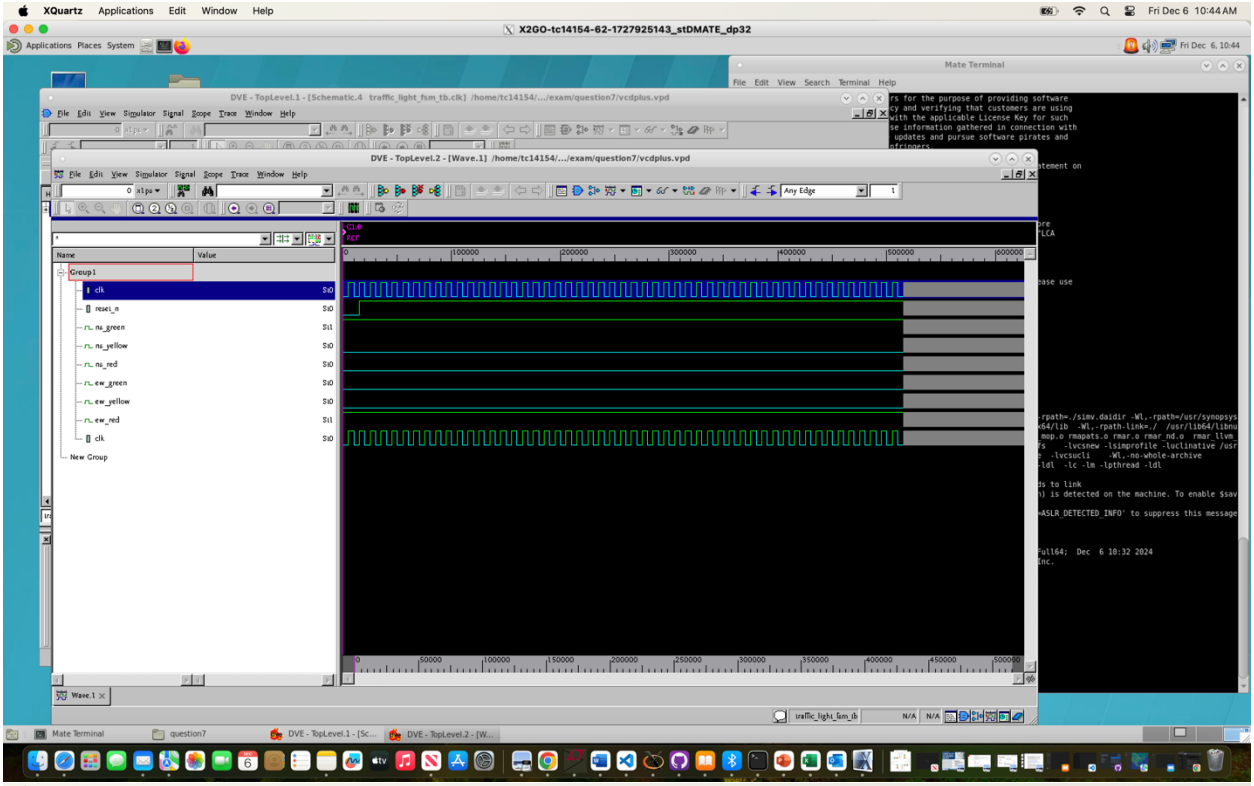
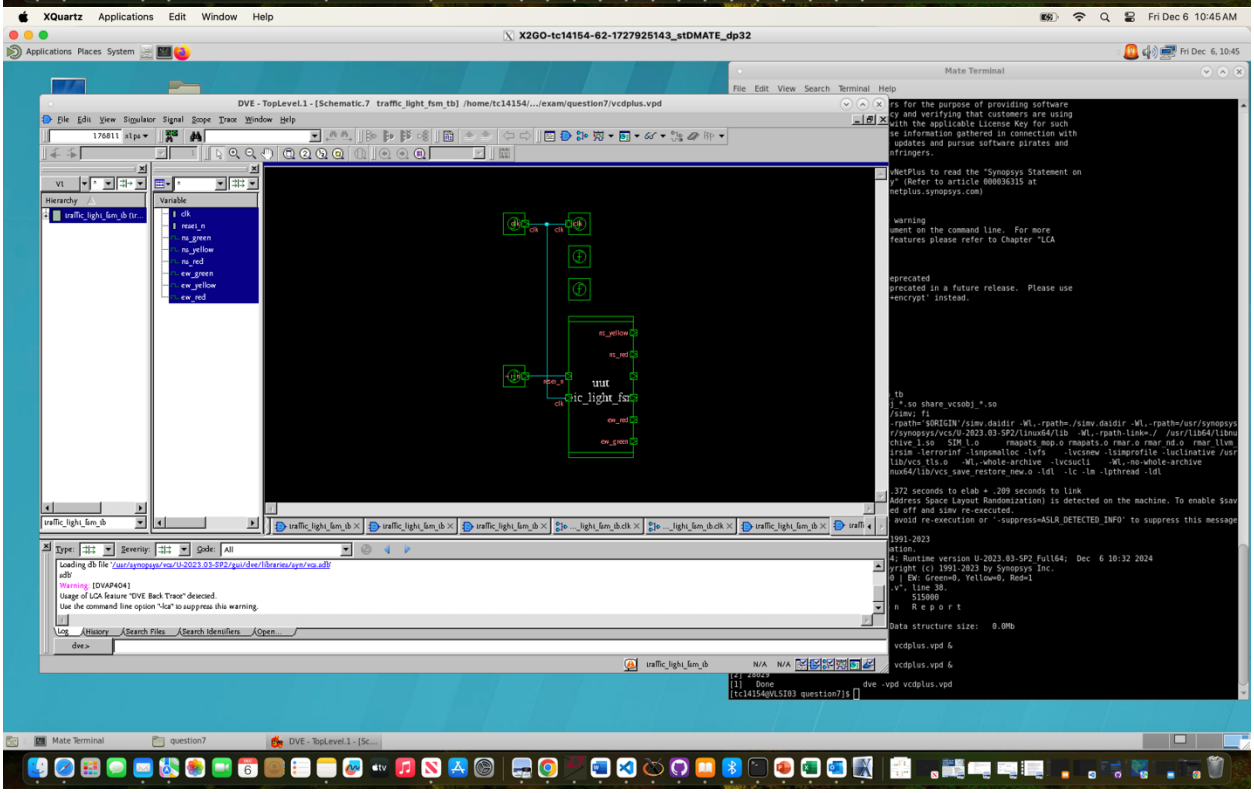
vNetPlus to read the "Synopsys Statement on
y" (Refer to article 000036315 at
netplus.synopsys.com)
warning
ument on the command line. For more
features please refer to Chapter "LCA
eprecated
precated in a future release. Please use
+encrypt' instead.
Data structure size: 0.0Mb
Fri Dec 6 10:32:15 2024
[tc14154@VLSI03 question7]$ dve -vpd vcdplus.vpd &
[1] 24054
[tc14154@VLSI03 question7]$
Mate Terminal
question7
DVE - TopLevel.1 - [So...


XQuartz Applications Edit Window Help
Fri Dec 6 10:35 AM
X2GO-tc14154-62-1727925143_stDMATE_dp32
DVE - TopLevel.1 - [Data.1] /home/tc14154/.../exam/question7/vcdplus.vpd
DVE - TopLevel.2 - [Wave.1] /home/tc14154/.../exam/question7/vcdplus.vpd
Mate Terminal
Group1
clk
reset_n
ns_green
ns_yellow
ns_red
ew_green
ew_yellow
ew_red
New Group


XQuartz Applications Edit Window Help
Fri Dec 6 10:44 AM
X2GO-tc14154-62-1727925143_stDMATE_dp32
DVE - TopLevel.1 - [Data.1] /home/tc14154/.../exam/question7/vcdplus.vpd
DVE - TopLevel.2 - [Wave.1] /home/tc14154/.../exam/question7/vcdplus.vpd
Mate Terminal
Group1
clk
reset_n
ns_green
ns_yellow
ns_red
ew_green
ew_yellow
ew_red
New Group


XQuartz Applications Edit Window Help
Fri Dec 6 10:44 AM
X2GO-tc14154-62-1727925143_stDMATE_dp32
Mate Terminal
DVE - TopLevel.1 - [Schematic.4 traffic_light_fsm_tb.clk] /home/tc14154/.../exam/question7/vcdplus.vpd
DVE - TopLevel.2 - [Wave.1] /home/tc14154/.../exam/question7/vcdplus.vpd
Group1
clk
reset_n
ns_green
ns_yellow
ns_red
ew_green
ew_yellow
ew_red
clk
New Group
Wave.1


XQuartz Applications Edit Window Help
Fri Dec 6 10:45 AM
X2GO-tc14154-62-1727925143_stDMATE_dp32
Mate Terminal
DVE - TopLevel.1 - [Schematic.7 traffic_light_fsm_tb] /home/tc14154/.../exam/question7/vcdplus.vpd
Hierarchy
Variable
clk
reset_n
ns_green
ns_yellow
ns_red
ew_green
ew_yellow
ew_red
uut
traffic_light_fsm_tb
Loading db file '/usr/synopsys/vcs/U-2023.03-SP2/gui/dve/libraries/syn/vcs.adb'
adb/
Warning- [DVAP404]
Usage of LCA feature "DVE Back Trace" detected.
Use the command line option "-lca" to suppress this warning.