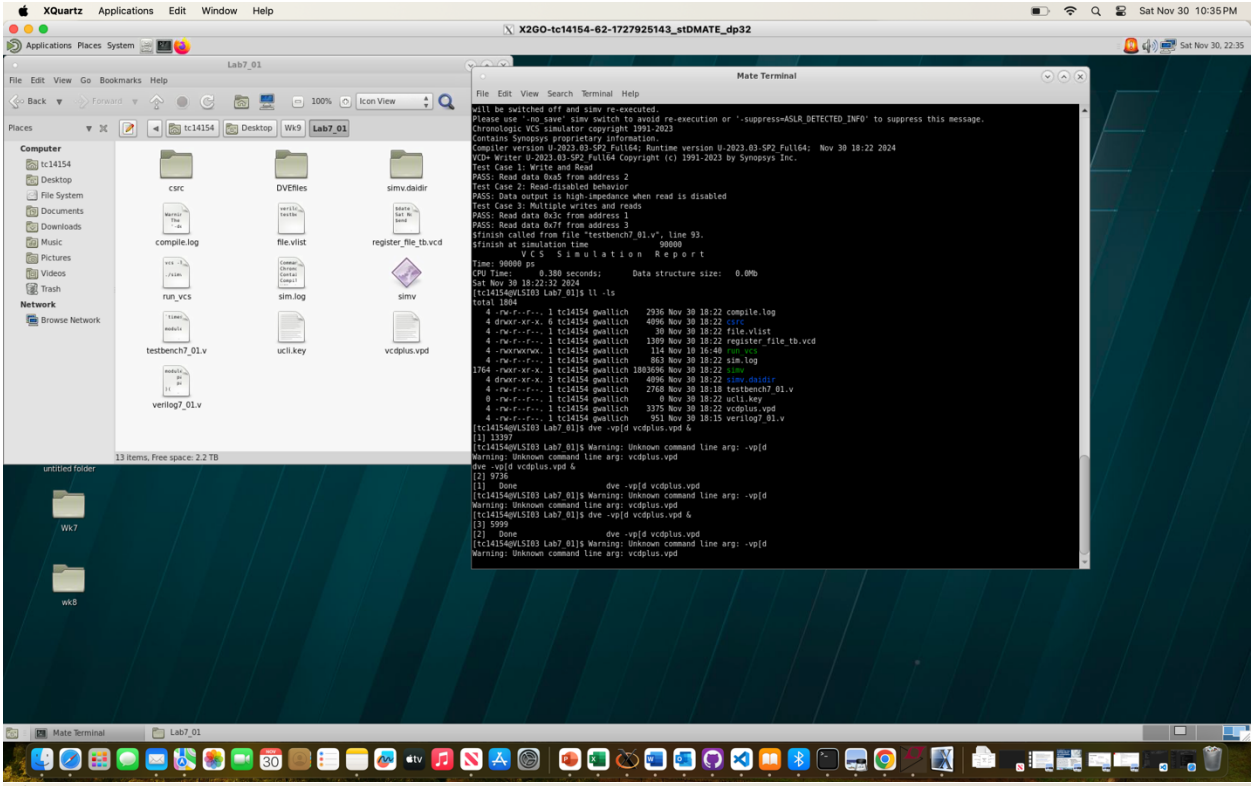
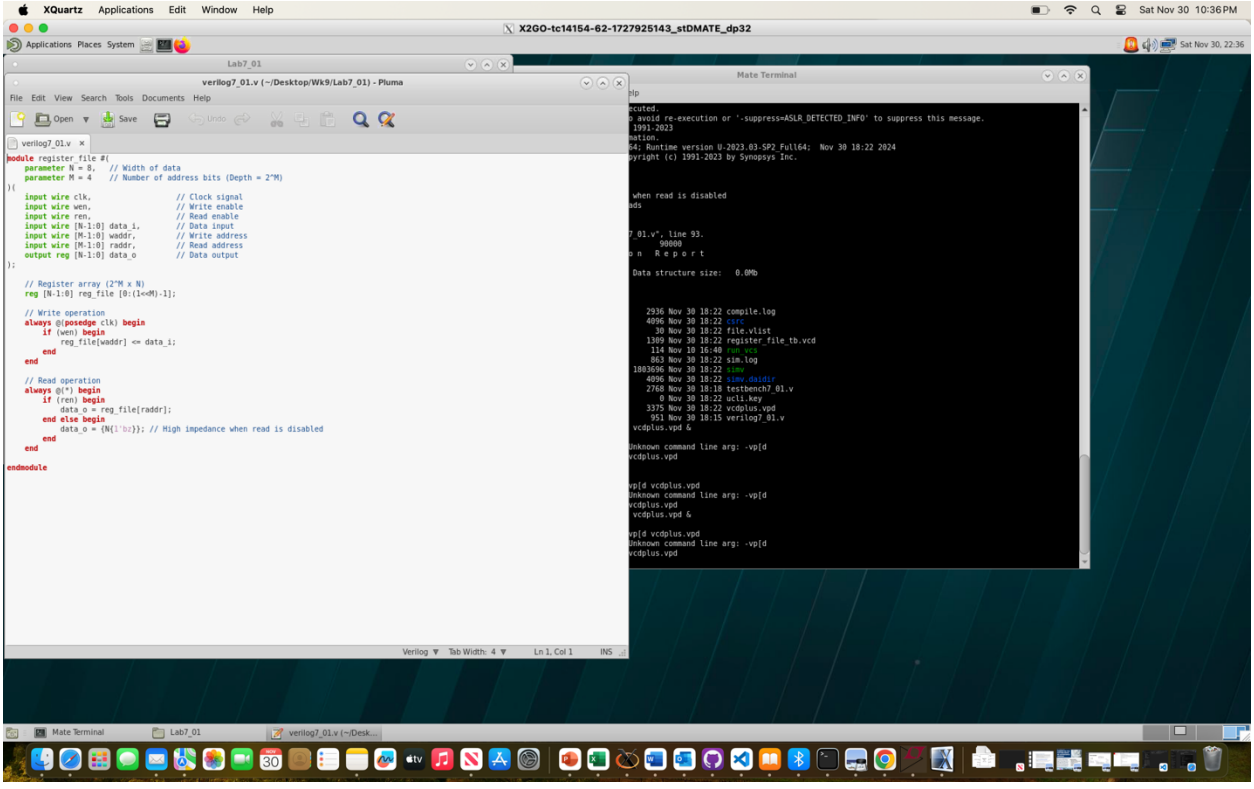
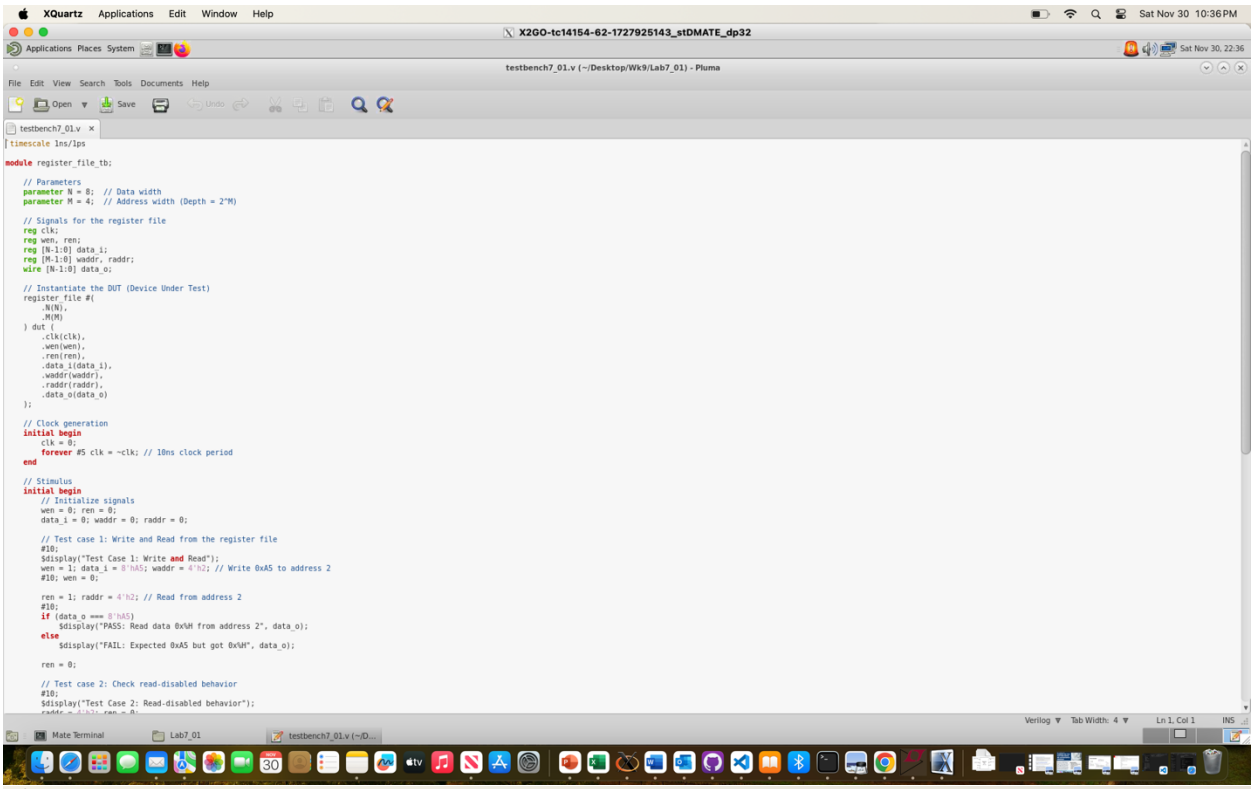
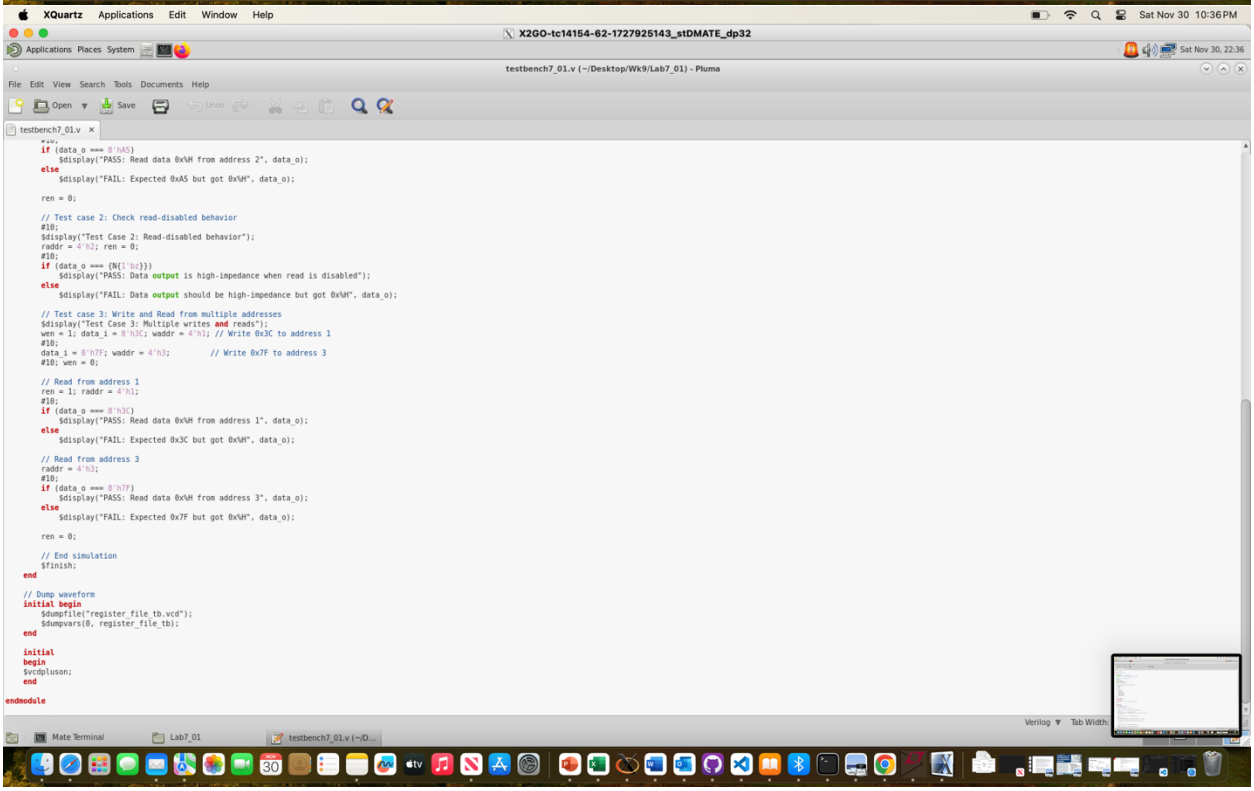
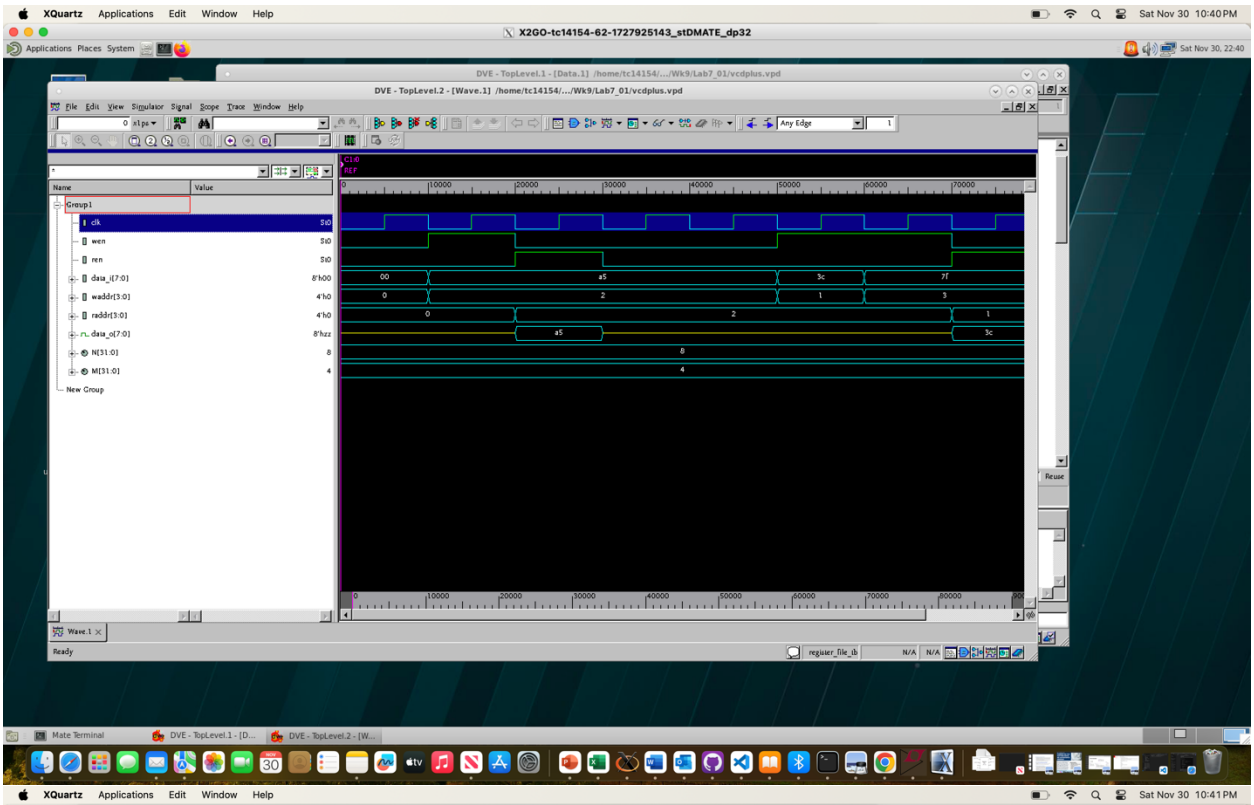
Lab07_01 a and b:

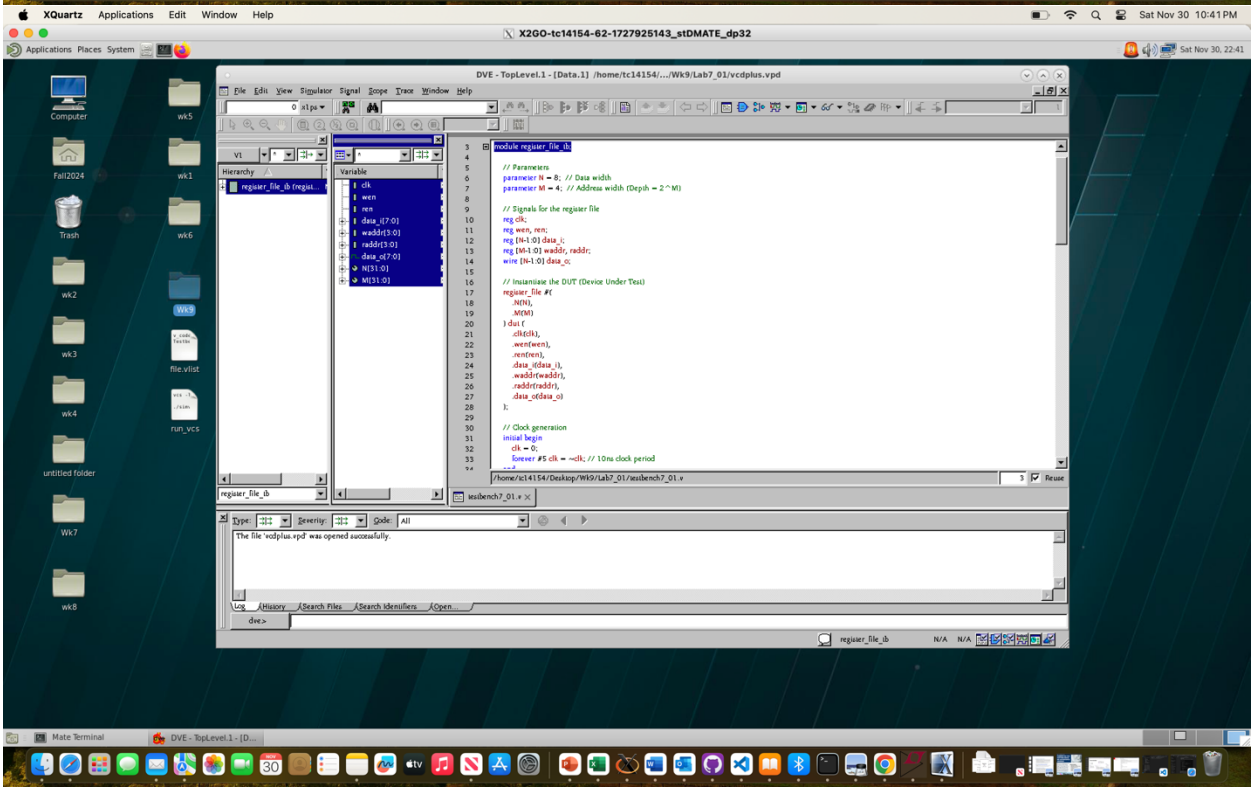

XQuartz Applications Edit Window Help
Sat Nov 30 10:35 PM
X2GO-tc14154-62-1727925143_stDMATE_dp32
Applications Places System
Sat Nov 30, 22:35
Lab7_01
File Edit View Go Bookmarks Help
Places
tc14154 Desktop Wk9 Lab7_01
Computer
tc14154
Desktop
File System
Documents
Downloads
Music
Pictures
Videos
Trash
Network
Browse Network
csrc
DVEfiles
simv.daidir
compile.log
file.vlist
register_file_tb.vcd
run_vcs
sim.log
simv
testbench7_01.v
ucli.key
vcdplus.vpd
verilog7_01.v
13 items, Free space: 2.2 TB
Mate Terminal
File Edit View Search Terminal Help
will be switched off and simv re-executed.
Please use '-no_save' simv switch to avoid re-execution or '-suppress=ASLR_DETECTED_INFO' to suppress this message.
Chronologic VCS simulator copyright 1991-2023
Contains Synopsys proprietary information.
Compiler version U-2023.03-SP2_Full64; Runtime version U-2023.03-SP2_Full64; Nov 30 18:22 2024
VCD+ Writer U-2023.03-SP2_Full64 Copyright (c) 1991-2023 by Synopsys Inc.
Test Case 1: Write and Read
PASS: Read data 0xa5 from address 2
Test Case 2: Read-disabled behavior
PASS: Data output is high-impedance when read is disabled
Test Case 3: Multiple writes and reads
PASS: Read data 0x3c from address 1
PASS: Read data 0x7f from address 3
$finish called from file "testbench7_01.v", line 93.
$finish at simulation time 90000
V C S S i m u l a t i o n R e p o r t
Time: 90000 ps
CPU Time: 0.380 seconds; Data structure size: 0.0Mb
Sat Nov 30 18:22:32 2024
[tc14154@VLSI03 Lab7_01]$ ll -ls
total 1804
4 -rw-r--r--. 1 tc14154 gwallich 2936 Nov 30 18:22 compile.log
4 drwxr-xr-x. 6 tc14154 gwallich 4096 Nov 30 18:22 csrc
4 -rw-r--r--. 1 tc14154 gwallich 30 Nov 30 18:22 file.vlist
4 -rw-r--r--. 1 tc14154 gwallich 1309 Nov 30 18:22 register_file_tb.vcd
4 -rwxrwxrwx. 1 tc14154 gwallich 114 Nov 10 16:40 run_vcs
4 -rw-r--r--. 1 tc14154 gwallich 863 Nov 30 18:22 sim.log
1764 -rwxr-xr-x. 1 tc14154 gwallich 1803696 Nov 30 18:22 simv
4 drwxr-xr-x. 3 tc14154 gwallich 4096 Nov 30 18:22 simv.daidir
4 -rw-r--r--. 1 tc14154 gwallich 2768 Nov 30 18:18 testbench7_01.v
0 -rw-r--r--. 1 tc14154 gwallich 0 Nov 30 18:22 ucli.key
4 -rw-r--r--. 1 tc14154 gwallich 3375 Nov 30 18:22 vcdplus.vpd
4 -rw-r--r--. 1 tc14154 gwallich 951 Nov 30 18:15 verilog7_01.v
[tc14154@VLSI03 Lab7_01]$ dve -vpd vcdplus.vpd &
[1] 13397
[tc14154@VLSI03 Lab7_01]$ Warning: Unknown command line arg: -vpd
Warning: Unknown command line arg: vcdplus.vpd
dve -vpd vcdplus.vpd &
[2] 9736
[1] Done dve -vpd vcdplus.vpd
[tc14154@VLSI03 Lab7_01]$ Warning: Unknown command line arg: -vpd
Warning: Unknown command line arg: vcdplus.vpd
[tc14154@VLSI03 Lab7_01]$ dve -vpd vcdplus.vpd &
[3] 5999
[2] Done dve -vpd vcdplus.vpd
[tc14154@VLSI03 Lab7_01]$ Warning: Unknown command line arg: -vpd
Warning: Unknown command line arg: vcdplus.vpd
untitled folder
Wk7
wk8
Mate Terminal
Lab7_01


XQuartz Applications Edit Window Help
Sat Nov 30 10:36 PM
X2GO-tc14154-62-1727925143_stDMATE_dp32
Applications Places System
Sat Nov 30, 22:36
Lab7_01
verilog7_01.v (~/Desktop/Wk9/Lab7_01) - Pluma
File Edit View Search Tools Documents Help
Open Save Undo
verilog7_01.v
module register_file #(
parameter N = 8, // Width of data
parameter M = 4 // Number of address bits (Depth = 2^M)
)(
input wire clk, // Clock signal
input wire wen, // Write enable
input wire ren, // Read enable
input wire [N-1:0] data_i, // Data input
input wire [M-1:0] waddr, // Write address
input wire [M-1:0] raddr, // Read address
output reg [N-1:0] data_o // Data output
);
// Register array (2^M x N)
reg [N-1:0] reg_file [0:(1<<M)-1];
// Write operation
always @(posedge clk) begin
if (wen) begin
reg_file[waddr] <= data_i;
end
end
// Read operation
always @(*) begin
if (ren) begin
data_o = reg_file[raddr];
end else begin
data_o = {N{1'bz}}; // High impedance when read is disabled
end
end
endmodule
Verilog Tab Width: 4 Ln 1, Col 1 INS
Mate Terminal
Lab7_01
verilog7_01.v (~/Desk...

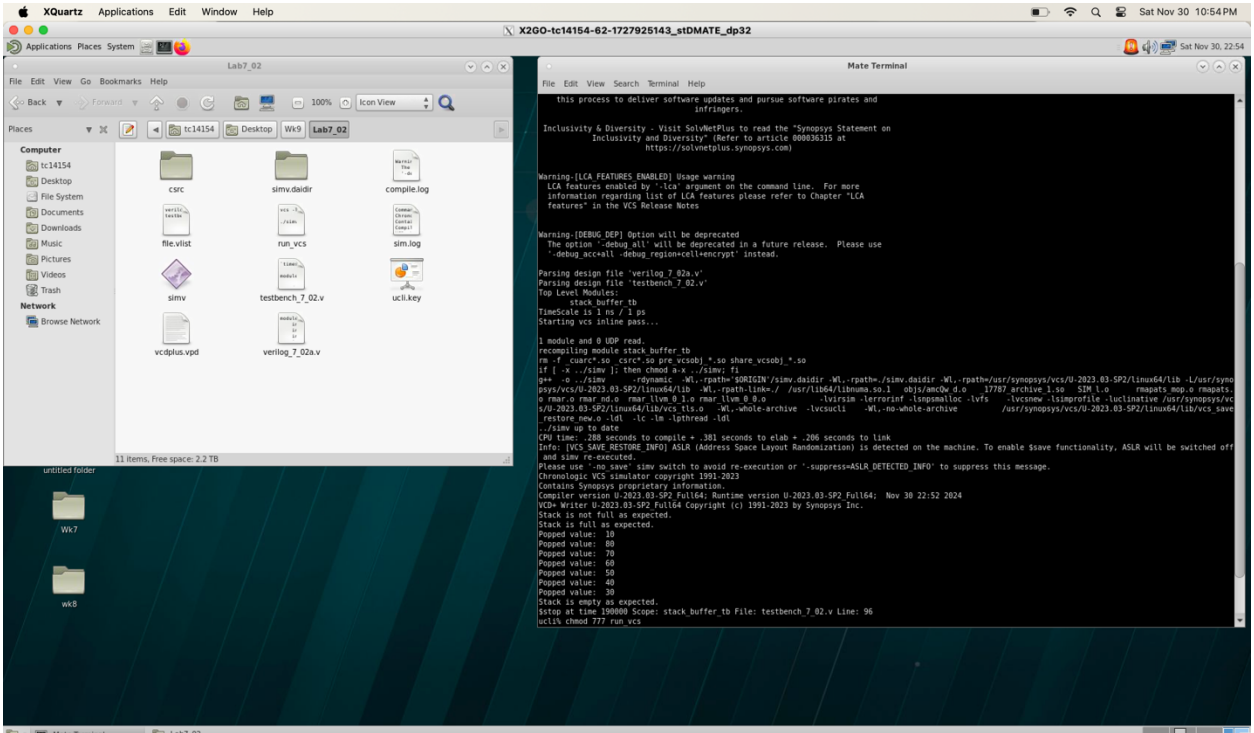

XQuartz Applications Edit Window Help
Sat Nov 30 10:36 PM
X2GO-tc14154-62-1727925143_stDMATE_dp32
Applications Places System
Sat Nov 30, 22:36
testbench7_01.v (~/Desktop/Wk9/Lab7_01) - Pluma
File Edit View Search Tools Documents Help
Open Save Undo
testbench7_01.v
`timescale 1ns/1ps
module register_file_tb;
// Parameters
parameter N = 8; // Data width
parameter M = 4; // Address width (Depth = 2^M)
// Signals for the register file
reg clk;
reg wen, ren;
reg [N-1:0] data_i;
reg [M-1:0] waddr, raddr;
wire [N-1:0] data_o;
// Instantiate the DUT (Device Under Test)
register_file #(
.N(N),
.M(M)
) dut (
.clk(clk),
.wen(wen),
.ren(ren),
.data_i(data_i),
.waddr(waddr),
.raddr(raddr),
.data_o(data_o)
);
// Clock generation
initial begin
clk = 0;
forever #5 clk = ~clk; // 10ns clock period
end
// Stimulus
initial begin
// Initialize signals
wen = 0; ren = 0;
data_i = 0; waddr = 0; raddr = 0;
// Test case 1: Write and Read from the register file
#10;
$display("Test Case 1: Write and Read");
wen = 1; data_i = 8'hA5; waddr = 4'h2; // Write 0xA5 to address 2
#10; wen = 0;
ren = 1; raddr = 4'h2; // Read from address 2
#10;
if (data_o === 8'hA5)
$display("PASS: Read data 0x%H from address 2", data_o);
else
$display("FAIL: Expected 0xA5 but got 0x%H", data_o);
ren = 0;
// Test case 2: Check read-disabled behavior
#10;
$display("Test Case 2: Read-disabled behavior");
Verilog Tab Width: 4 Ln 1, Col 1 INS
Mate Terminal
Lab7_01
testbench7_01.v (~/D...

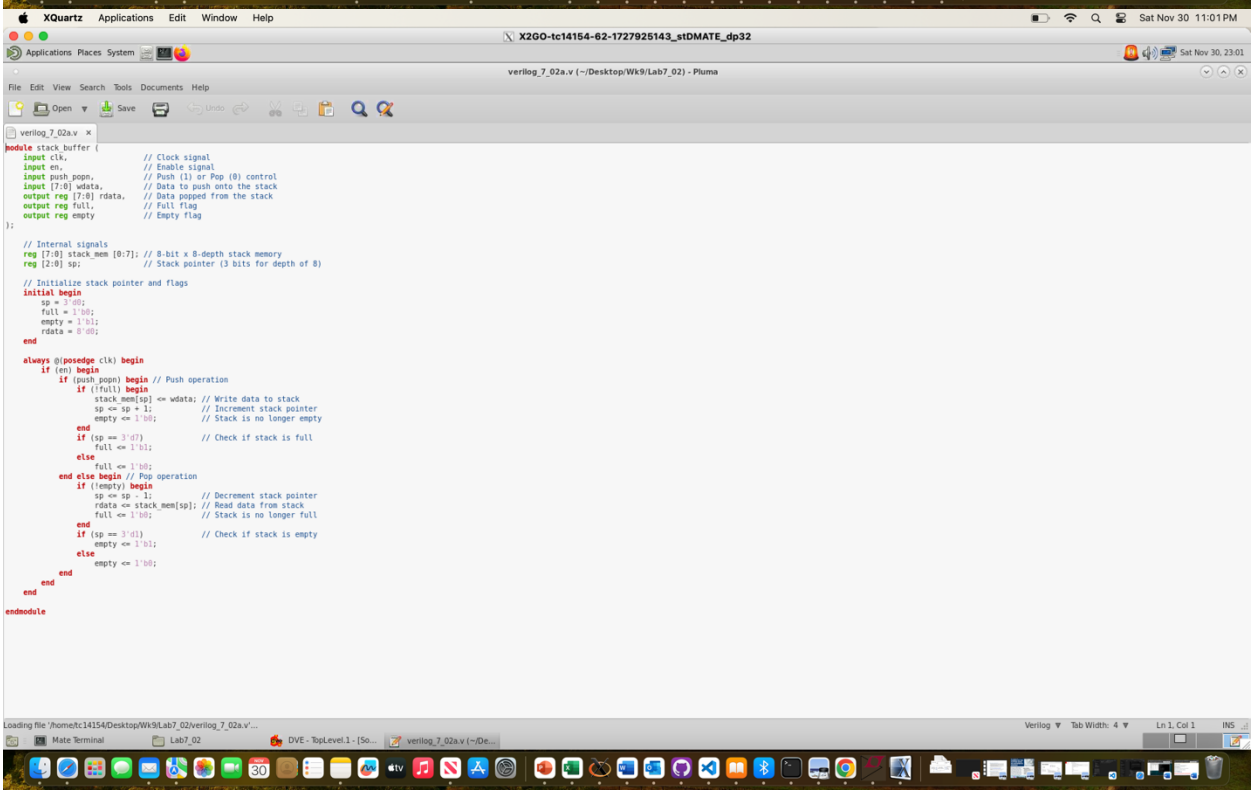

XQuartz Applications Edit Window Help
Sat Nov 30 10:36 PM
X2GO-tc14154-62-1727925143_stDMATE_dp32
Applications Places System
Sat Nov 30, 22:36
testbench7_01.v (~/Desktop/Wk9/Lab7_01) - Pluma
File Edit View Search Tools Documents Help
Open Save Undo
testbench7_01.v
if (data_o === 8'hA5)
$display("PASS: Read data 0x%H from address 2", data_o);
else
$display("FAIL: Expected 0xA5 but got 0x%H", data_o);
ren = 0;
// Test case 2: Check read-disabled behavior
#10;
$display("Test Case 2: Read-disabled behavior");
raddr = 4'h2; ren = 0;
#10;
if (data_o === {N{1'bz}})
$display("PASS: Data output is high-impedance when read is disabled");
else
$display("FAIL: Data output should be high-impedance but got 0x%H", data_o);
// Test case 3: Write and Read from multiple addresses
$display("Test Case 3: Multiple writes and reads");
wen = 1; data_i = 8'h3C; waddr = 4'h1; // Write 0x3C to address 1
#10;
data_i = 8'h7F; waddr = 4'h3; // Write 0x7F to address 3
#10; wen = 0;
// Read from address 1
ren = 1; raddr = 4'h1;
#10;
if (data_o === 8'h3C)
$display("PASS: Read data 0x%H from address 1", data_o);
else
$display("FAIL: Expected 0x3C but got 0x%H", data_o);
// Read from address 3
raddr = 4'h3;
#10;
if (data_o === 8'h7F)
$display("PASS: Read data 0x%H from address 3", data_o);
else
$display("FAIL: Expected 0x7F but got 0x%H", data_o);
ren = 0;
// End simulation
$finish;
end
// Dump waveform
initial begin
$dumpfile("register_file_tb.vcd");
$dumpvars(0, register_file_tb);
end
initial
begin
$vcdpluson;
end
endmodule
Verilog Tab Width:
Mate Terminal
Lab7_01
testbench7_01.v (~/D...

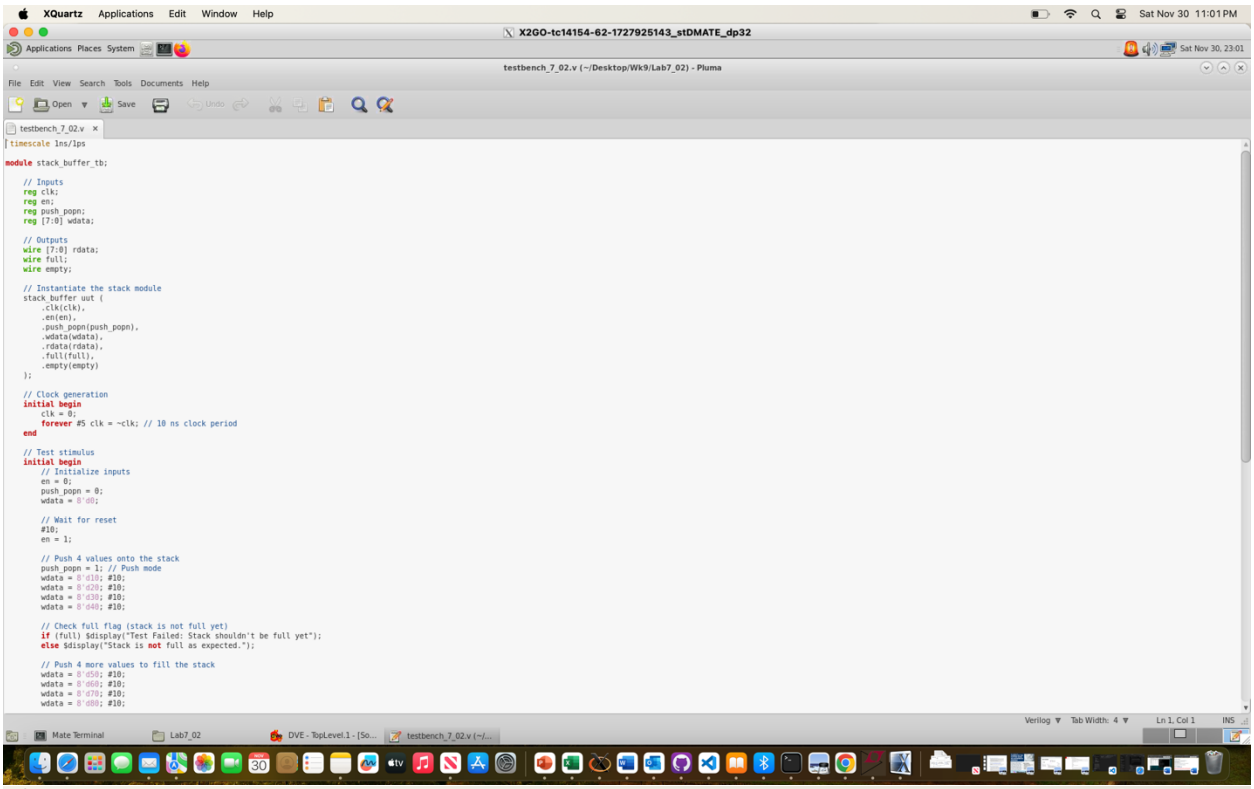

XQuartz Applications Edit Window Help
Sat Nov 30 10:40 PM
X2GO-tc14154-62-1727925143_stDMATE_dp32
DVE - TopLevel.2 - [Wave.1] /home/tc14154/.../Wk9/Lab7_01/vcdplus.vpd
Group1
clk
wen
ren
data_i[7:0]
waddr[3:0]
raddr[3:0]
data_o[7:0]
N[31:0]
M[31:0]
New Group

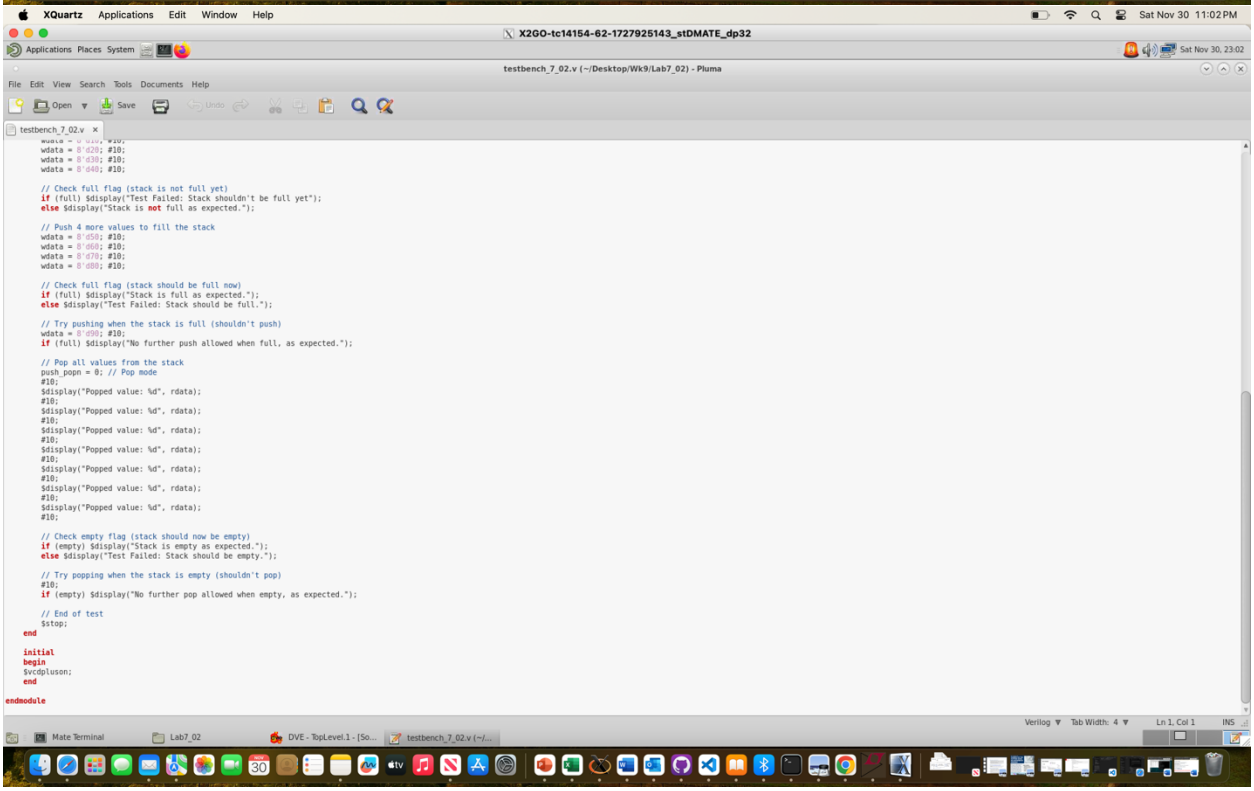

XQuartz Applications Edit Window Help
Sat Nov 30 10:41 PM
X2GO-tc14154-62-1727925143_stDMATE_dp32
DVE - TopLevel.1 - [Data.1] /home/tc14154/.../Wk9/Lab7_01/vcdplus.vpd
module register_file_tb
// Parameters
parameter N = 8; // Data width
parameter M = 4; // Address width (Depth = 2^M)
// Signals for the register file
reg clk;
reg wen, ren;
reg [N-1:0] data_i;
reg [M-1:0] waddr, raddr;
wire [N-1:0] data_o;
// Instantiate the DUT (Device Under Test)
register_file #(
.N(N),
.M(M)
) dut (
.clk(clk),
.wen(wen),
.ren(ren),
.data_i(data_i),
.waddr(waddr),
.raddr(raddr),
.data_o(data_o)
);
// Clock generation
initial begin
clk = 0;
forever #5 clk = ~clk; // 10ns clock period
The file 'vcdplus.vpd' was opened successfully.

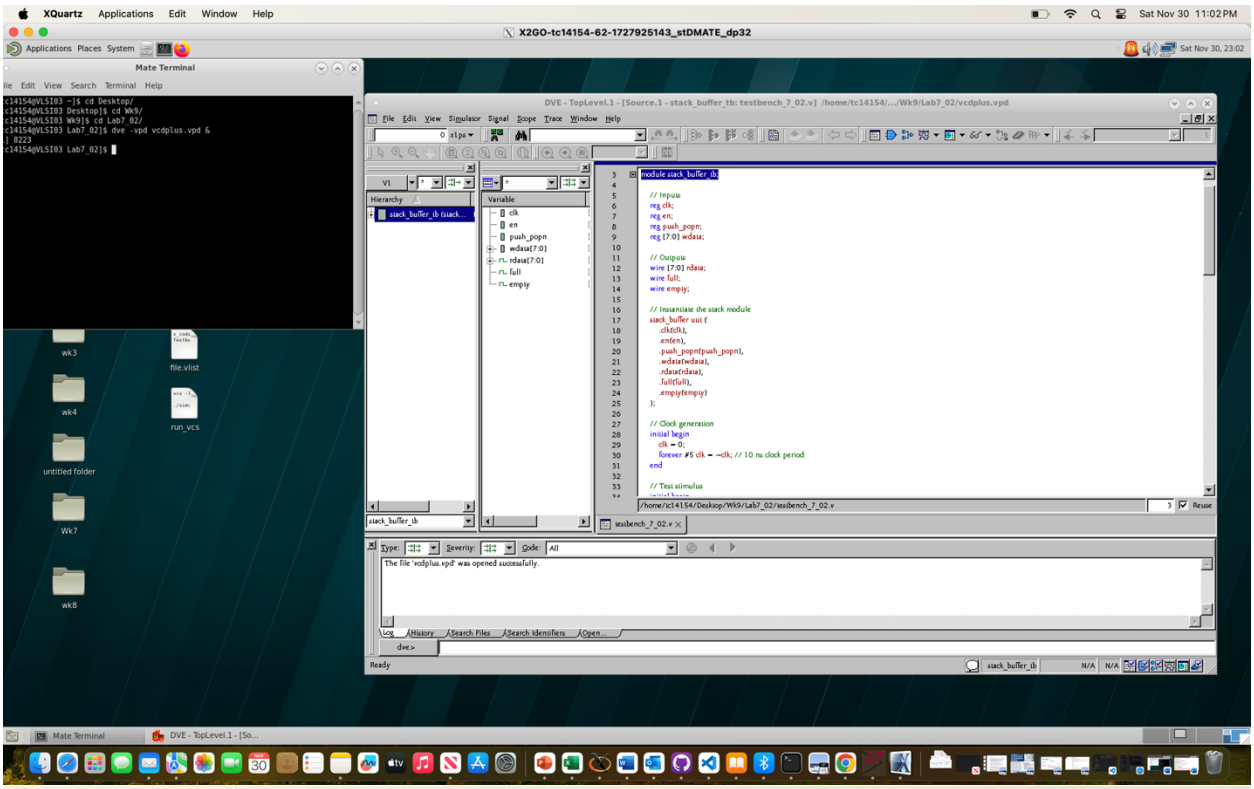
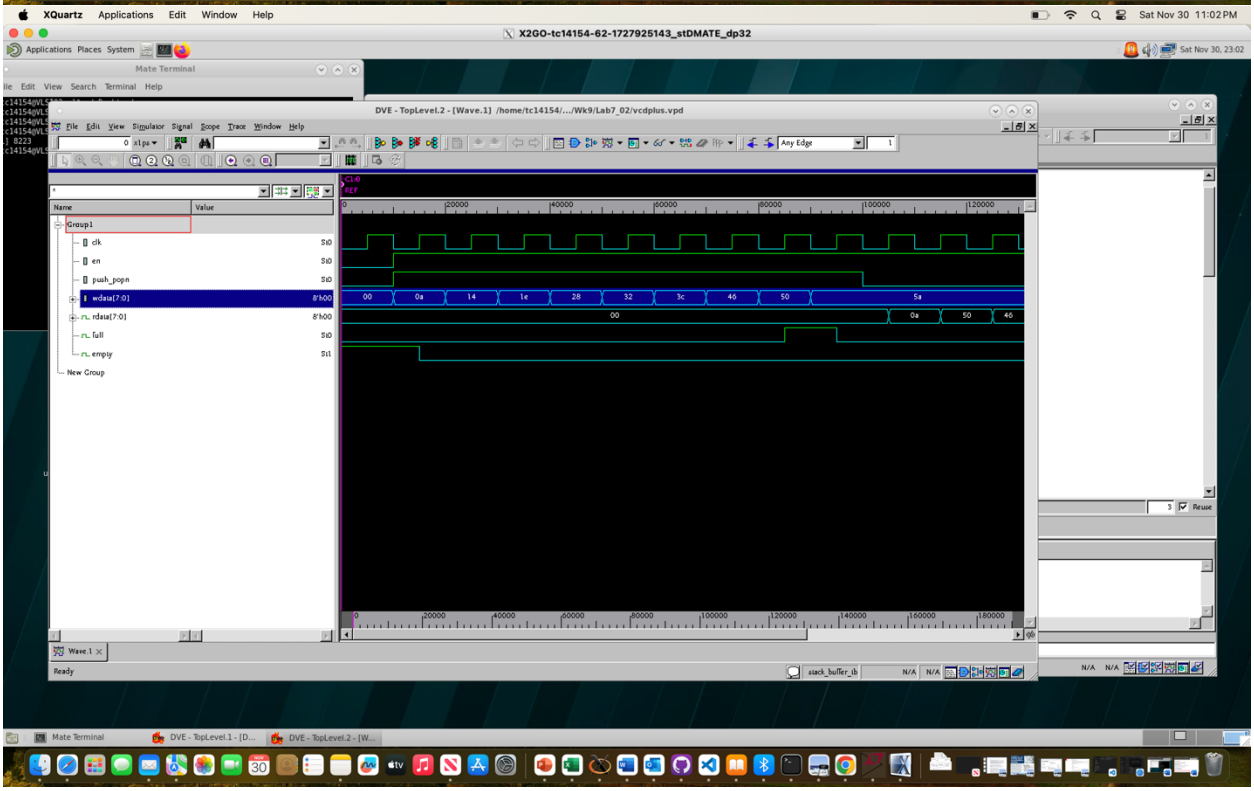
Lab07_02 a and b:



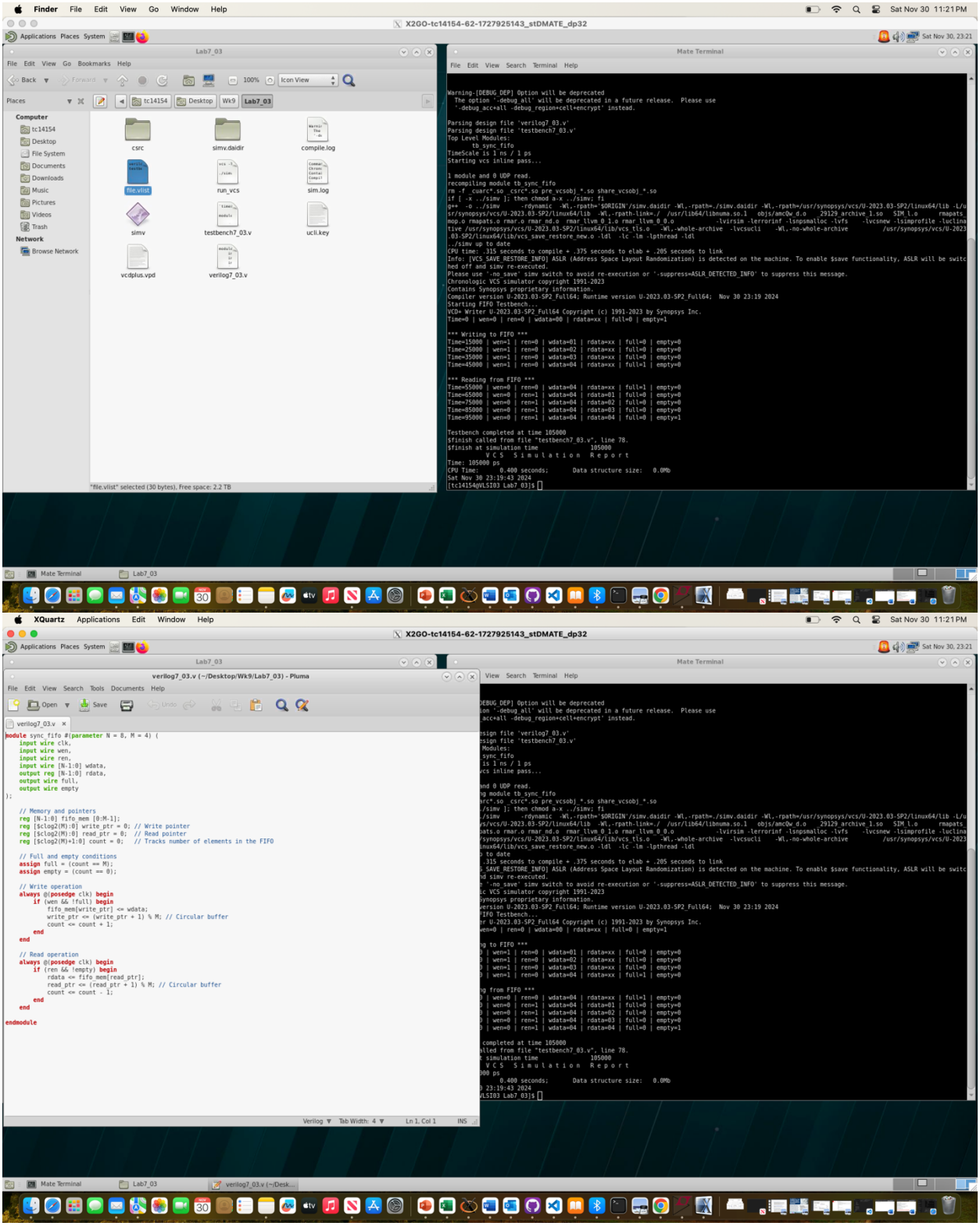


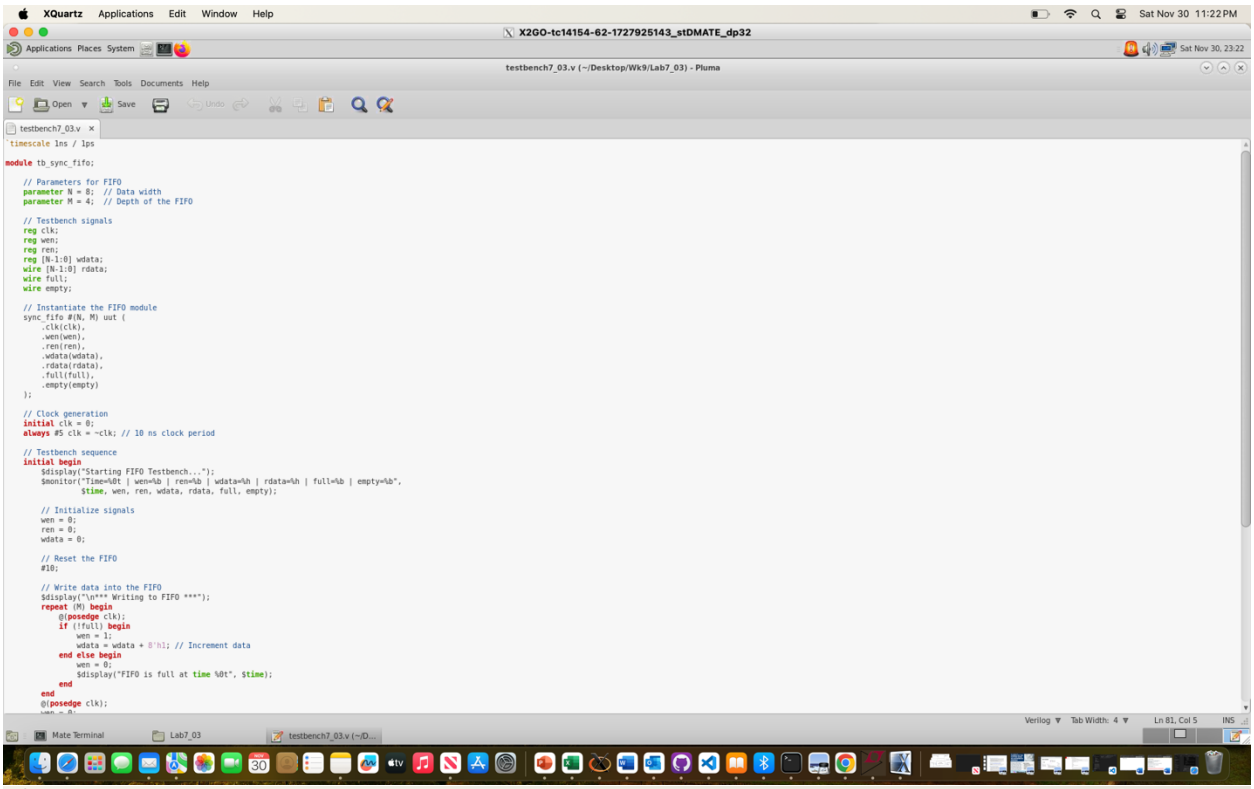

XQuartz Applications Edit Window Help
Sat Nov 30 11:01 PM
X2GO-tc14154-62-1727925143_stDMATE_dp32
Applications Places System
Sat Nov 30, 23:01
testbench_7_02.v (~/Desktop/Wk9/Lab7_02) - Pluma
File Edit View Search Tools Documents Help
Open Save Undo
testbench_7_02.v
`timescale 1ns/1ps
module stack_buffer_tb;
// Inputs
reg clk;
reg en;
reg push_popn;
reg [7:0] wdata;
// Outputs
wire [7:0] rdata;
wire full;
wire empty;
// Instantiate the stack module
stack_buffer uut (
.clk(clk),
.en(en),
.push_popn(push_popn),
.wdata(wdata),
.rdata(rdata),
.full(full),
.empty(empty)
);
// Clock generation
initial begin
clk = 0;
forever #5 clk = ~clk; // 10 ns clock period
end
// Test stimulus
initial begin
// Initialize inputs
en = 0;
push_popn = 0;
wdata = 8'd0;
// Wait for reset
#10;
en = 1;
// Push 4 values onto the stack
push_popn = 1; // Push mode
wdata = 8'd10; #10;
wdata = 8'd20; #10;
wdata = 8'd30; #10;
wdata = 8'd40; #10;
// Check full flag (stack is not full yet)
if (full) $display("Test Failed: Stack shouldn't be full yet");
else $display("Stack is not full as expected.");
// Push 4 more values to fill the stack
wdata = 8'd50; #10;
wdata = 8'd60; #10;
wdata = 8'd70; #10;
wdata = 8'd80; #10;
Verilog Tab Width: 4 Ln 1, Col 1 INS
Mate Terminal
Lab7_02
DVE - TopLevel.1 - [So...
testbench_7_02.v (~/...

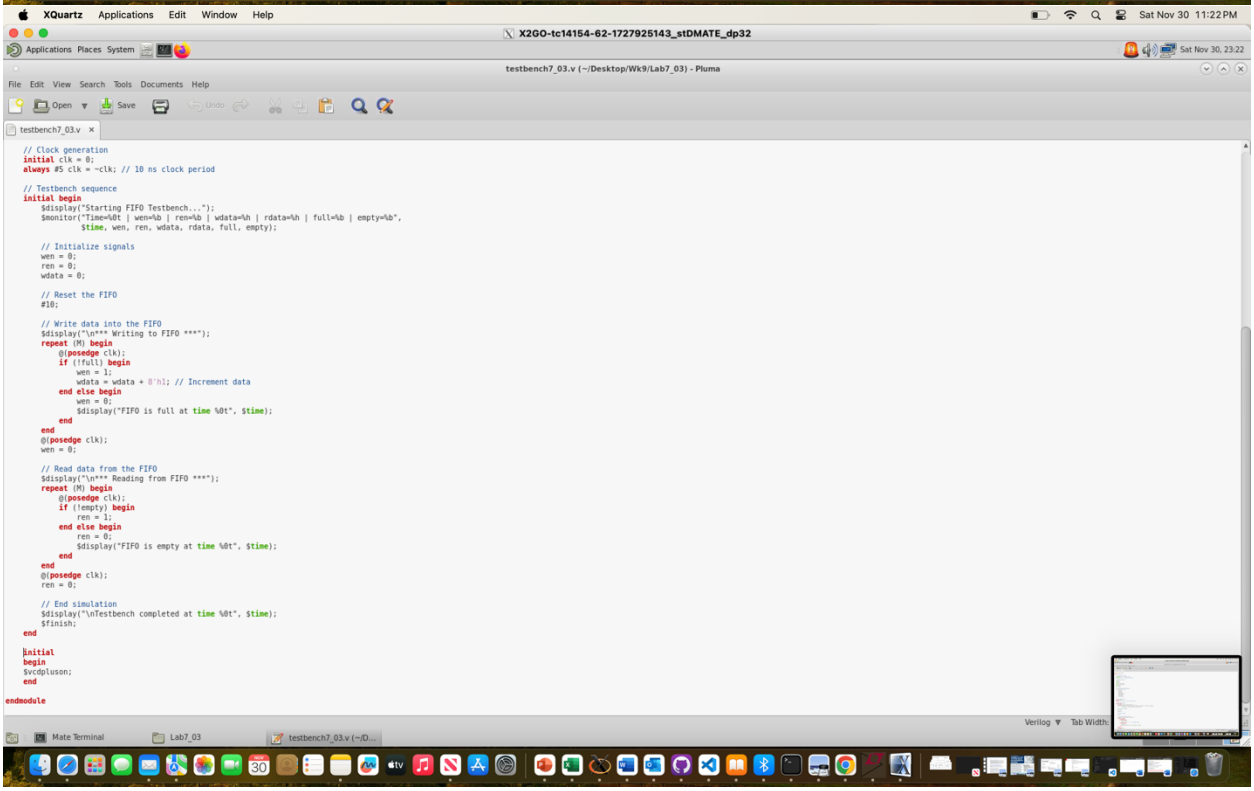

XQuartz Applications Edit Window Help
Sat Nov 30 11:02 PM
X2GO-tc14154-62-1727925143_stDMATE_dp32
Applications Places System
Sat Nov 30, 23:02
testbench_7_02.v (~/Desktop/Wk9/Lab7_02) - Pluma
File Edit View Search Tools Documents Help
Open Save Undo
testbench_7_02.v
wdata = 8'd20; #10;
wdata = 8'd30; #10;
wdata = 8'd40; #10;
// Check full flag (stack is not full yet)
if (full) $display("Test Failed: Stack shouldn't be full yet");
else $display("Stack is not full as expected.");
// Push 4 more values to fill the stack
wdata = 8'd50; #10;
wdata = 8'd60; #10;
wdata = 8'd70; #10;
wdata = 8'd80; #10;
// Check full flag (stack should be full now)
if (full) $display("Stack is full as expected.");
else $display("Test Failed: Stack should be full.");
// Try pushing when the stack is full (shouldn't push)
wdata = 8'd90; #10;
if (full) $display("No further push allowed when full, as expected.");
// Pop all values from the stack
push_popn = 0; // Pop mode
#10;
$display("Popped value: %d", rdata);
#10;
$display("Popped value: %d", rdata);
#10;
$display("Popped value: %d", rdata);
#10;
$display("Popped value: %d", rdata);
#10;
$display("Popped value: %d", rdata);
#10;
$display("Popped value: %d", rdata);
#10;
$display("Popped value: %d", rdata);
#10;
// Check empty flag (stack should now be empty)
if (empty) $display("Stack is empty as expected.");
else $display("Test Failed: Stack should be empty.");
// Try popping when the stack is empty (shouldn't pop)
#10;
if (empty) $display("No further pop allowed when empty, as expected.");
// End of test
$stop;
end
initial
begin
$vcdpluson;
end
endmodule
Verilog Tab Width: 4 Ln 1, Col 1 INS
Mate Terminal
Lab7_02
DVE - TopLevel.1 - [So...
testbench_7_02.v (~/...

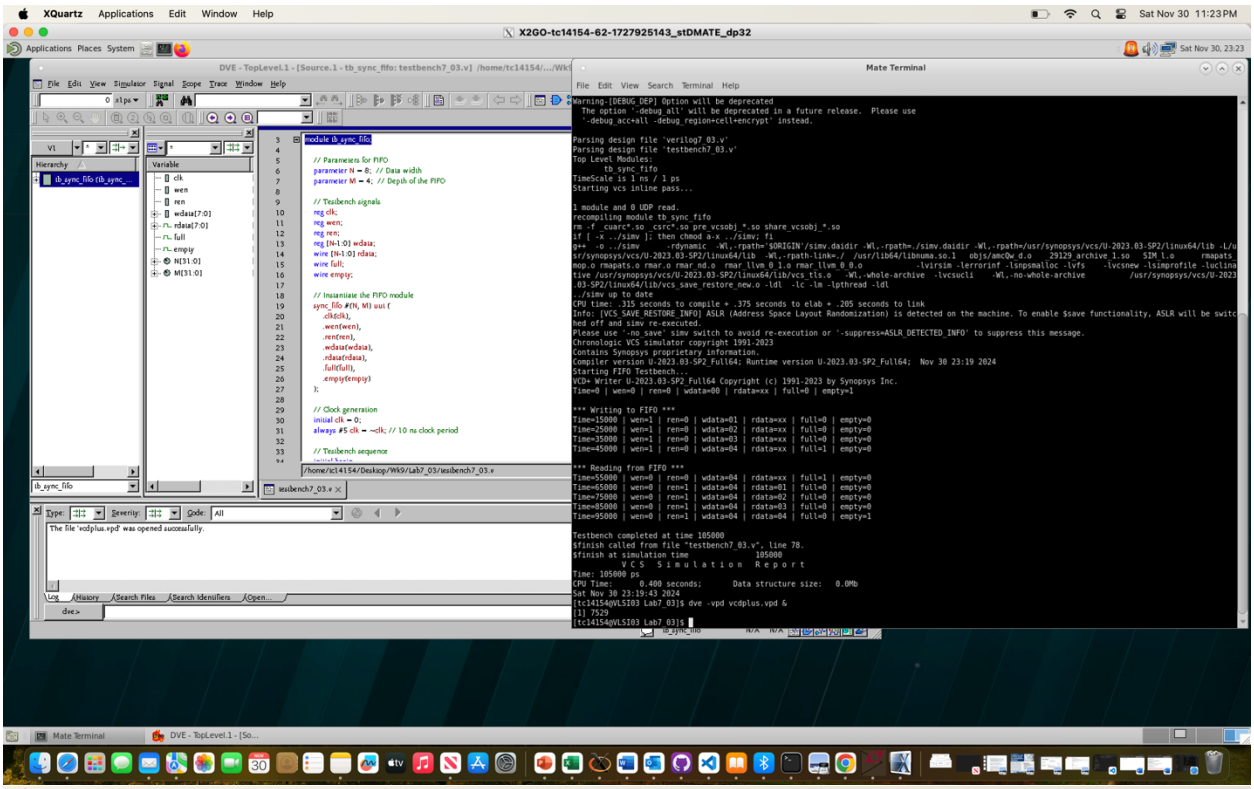

XQuartz Applications Edit Window Help
Sat Nov 30 11:02 PM
X2GO-tc14154-62-1727925143_stDMATE_dp32
Mate Terminal
DVE - TopLevel.1 - [Source.1 - stack_buffer_tb: testbench_7_02.v] /home/tc14154/.../Wk9/Lab7_02/vcdplus.vpd
module stack_buffer_tb;
// Inputs
reg clk;
reg en;
reg push_popn;
reg [7:0] wdata;
// Outputs
wire [7:0] rdata;
wire full;
wire empty;
// Instantiate the stack module
stack_buffer uut (
.clk(clk),
.en(en),
.push_popn(push_popn),
.wdata(wdata),
.rdata(rdata),
.full(full),
.empty(empty)
);
// Clock generation
initial begin
clk = 0;
forever #5 clk = ~clk; // 10 ns clock period
end
// Test stimulus
The file 'vcdplus.vpd' was opened successfully.

XQuartz Applications Edit Window Help
Sat Nov 30 11:02 PM
X2GO-tc14154-62-1727925143_stDMATE_dp32
DVE - TopLevel.2 - [Wave.1] /home/tc14154/.../Wk9/Lab7_02/vcdplus.vpd
Group1
clk
en
push_popn
wdata[7:0]
rdata[7:0]
full
empty
New Group
Wave.1
Ready

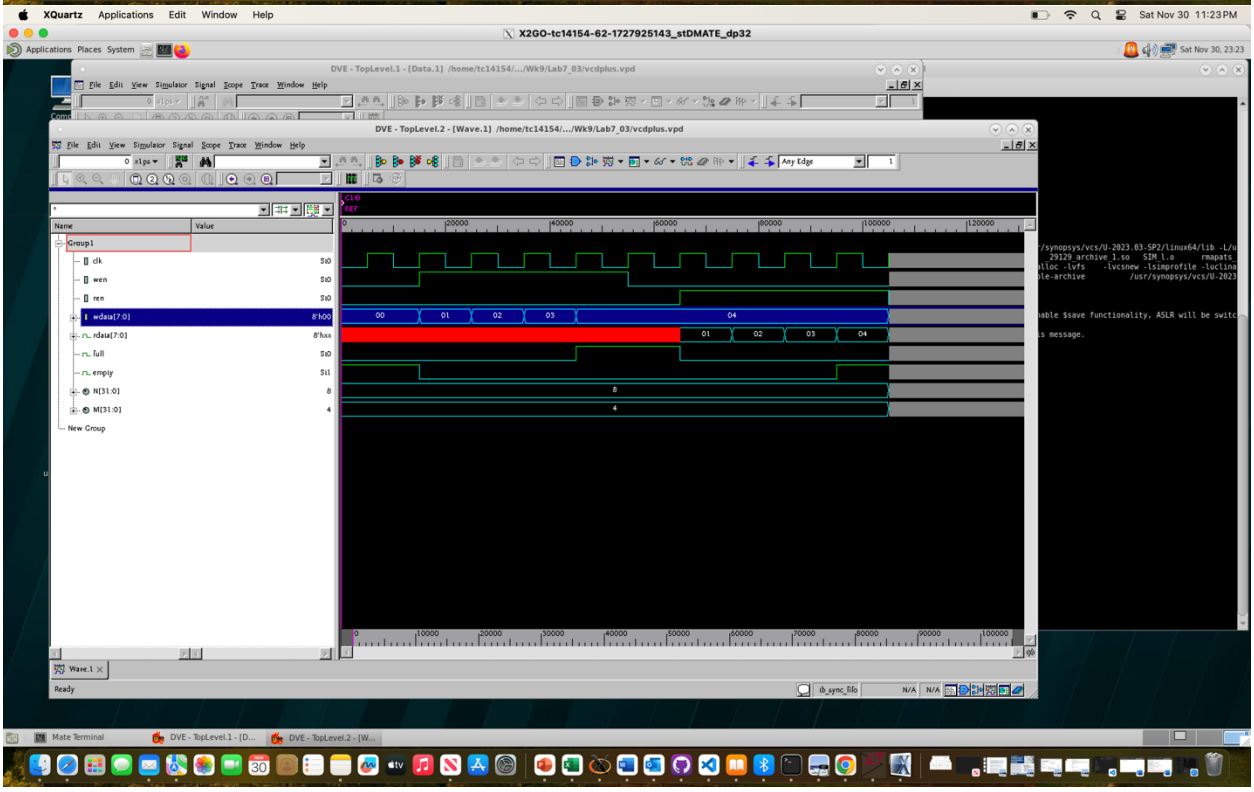
Lab07_03 a and b:




XQuartz Applications Edit Window Help
Sat Nov 30 11:22 PM
X2GO-tc14154-62-1727925143_stDMATE_dp32
Applications Places System
Sat Nov 30, 23:22
testbench7_03.v (~/Desktop/Wk9/Lab7_03) - Pluma
File Edit View Search Tools Documents Help
Open Save Undo
testbench7_03.v
`timescale 1ns / 1ps
module tb_sync_fifo;
// Parameters for FIFO
parameter N = 8; // Data width
parameter M = 4; // Depth of the FIFO
// Testbench signals
reg clk;
reg wen;
reg ren;
reg [N-1:0] wdata;
wire [N-1:0] rdata;
wire full;
wire empty;
// Instantiate the FIFO module
sync_fifo #(N, M) uut (
.clk(clk),
.wen(wen),
.ren(ren),
.wdata(wdata),
.rdata(rdata),
.full(full),
.empty(empty)
);
// Clock generation
initial clk = 0;
always #5 clk = ~clk; // 10 ns clock period
// Testbench sequence
initial begin
$display("Starting FIFO Testbench...");
$monitor("Time=%0t | wen=%b | ren=%b | wdata=%h | rdata=%h | full=%b | empty=%b",
$time, wen, ren, wdata, rdata, full, empty);
// Initialize signals
wen = 0;
ren = 0;
wdata = 0;
// Reset the FIFO
#10;
// Write data into the FIFO
$display("\n*** Writing to FIFO ***");
repeat (M) begin
@(posedge clk);
if (!full) begin
wen = 1;
wdata = wdata + 8'h1; // Increment data
end else begin
wen = 0;
$display("FIFO is full at time %0t", $time);
end
end
@(posedge clk);
Verilog Tab Width: 4 Ln 81, Col 5 INS
Mate Terminal
Lab7_03
testbench7_03.v (~/D...


XQuartz Applications Edit Window Help
Sat Nov 30 11:22 PM
X2GO-tc14154-62-1727925143_stDMATE_dp32
Applications Places System
Sat Nov 30, 23:22
testbench7_03.v (~/Desktop/Wk9/Lab7_03) - Pluma
File Edit View Search Tools Documents Help
Open Save Undo
testbench7_03.v
// Clock generation
initial clk = 0;
always #5 clk = ~clk; // 10 ns clock period
// Testbench sequence
initial begin
$display("Starting FIFO Testbench...");
$monitor("Time=%0t | wen=%b | ren=%b | wdata=%h | rdata=%h | full=%b | empty=%b",
$time, wen, ren, wdata, rdata, full, empty);
// Initialize signals
wen = 0;
ren = 0;
wdata = 0;
// Reset the FIFO
#10;
// Write data into the FIFO
$display("\n*** Writing to FIFO ***");
repeat (M) begin
@(posedge clk);
if (!full) begin
wen = 1;
wdata = wdata + 8'h1; // Increment data
end else begin
wen = 0;
$display("FIFO is full at time %0t", $time);
end
end
@(posedge clk);
wen = 0;
// Read data from the FIFO
$display("\n*** Reading from FIFO ***");
repeat (M) begin
@(posedge clk);
if (!empty) begin
ren = 1;
end else begin
ren = 0;
$display("FIFO is empty at time %0t", $time);
end
end
@(posedge clk);
ren = 0;
// End simulation
$display("\nTestbench completed at time %0t", $time);
$finish;
end
initial
begin
$vcdpluson;
end
endmodule
Verilog Tab Width:
Mate Terminal
Lab7_03
testbench7_03.v (~/D...


XQuartz Applications Edit Window Help
Sat Nov 30 11:23 PM
X2GO-tc14154-62-1727925143_stDMATE_dp32
Applications Places System
Sat Nov 30, 23:23
DVE - TopLevel.1 - [Source.1 - tb_sync_fifo: testbench7_03.v] /home/tc14154/.../Wk9/Lab7_03/testbench7_03.v
File Edit View Simulator Signal Scope Trace Window Help
Hierarchy
tb_sync_fifo (tb_sync_...
Variable
clk
wen
ren
wdata[7:0]
rdata[7:0]
full
empty
N[31:0]
M[31:0]
module tb_sync_fifo;
// Parameters for FIFO
parameter N = 8; // Data width
parameter M = 4; // Depth of the FIFO
// Testbench signals
reg clk;
reg wen;
reg ren;
reg [N-1:0] wdata;
wire [N-1:0] rdata;
wire full;
wire empty;
// Instantiate the FIFO module
sync_fifo #(N, M) uut (
.clk(clk),
.wen(wen),
.ren(ren),
.wdata(wdata),
.rdata(rdata),
.full(full),
.empty(empty)
);
// Clock generation
initial clk = 0;
always #5 clk = ~clk; // 10 ns clock period
// Testbench sequence
/home/tc14154/Desktop/Wk9/Lab7_03/testbench7_03.v
testbench7_03.v
Type: Severity: Code: All
'The file 'vcdplus.vpd' was opened successfully.
Log History Search Files Search Identifiers Open...
dve>
Mate Terminal
File Edit View Search Terminal Help
Warning-[DEBUG_DEP] Option will be deprecated
The option '-debug_all' will be deprecated in a future release. Please use
'-debug_acc+all -debug_region+cell+encrypt' instead.
Parsing design file 'verilog7_03.v'
Parsing design file 'testbench7_03.v'
Top Level Modules:
tb_sync_fifo
TimeScale is 1 ns / 1 ps
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb_sync_fifo
rm -f _cuarc*.so _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
if [-x ../simv]; then chmod a-x ../simv; fi
g++ -o ../simv -rdynamic -Wl,-rpath='$ORIGIN'/simv.daidir -Wl,-rpath=./simv.daidir -Wl,-rpath=/usr/synopsys/vcs/U-2023.03-SP2/linux64/lib -L/u
sr/synopsys/vcs/U-2023.03-SP2/linux64/lib -Wl,-rpath-link=./ /usr/lib64/libnuma.so.1 objs/amc0w_d.o 29129_archive_1.so SIM_l.o rmapats_
mop.o rmapats.o rmar.o rmar_nd.o rmar_llvm_0_1.o rmar_llvm_0_0.o -lvirsim -lerrorinf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -luclina
tive /usr/synopsys/vcs/U-2023.03-SP2/linux64/lib/vcs_tls.a -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive /usr/synopsys/vcs/U-2023
.03-SP2/linux64/lib/vcs_save_restore_new.o -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .315 seconds to compile + .375 seconds to elab + .205 seconds to link
Info: [VCS_SAVE_RESTORE_INFO] ASLR (Address Space Layout Randomization) is detected on the machine. To enable $save functionality, ASLR will be switc
hed off and simv re-executed.
Please use '-no_save' simv switch to avoid re-execution or '-suppress=ASLR_DETECTED_INFO' to suppress this message.
Chronologic VCS simulator copyright 1991-2023
Contains Synopsys proprietary information.
Compiler version U-2023.03-SP2_Full64; Runtime version U-2023.03-SP2_Full64; Nov 30 23:19 2024
Starting FIFO Testbench...
VCD+ Writer U-2023.03-SP2_Full64 Copyright (c) 1991-2023 by Synopsys Inc.
Time=0 | wen=0 | ren=0 | wdata=00 | rdata=xx | full=0 | empty=1
*** Writing to FIFO ***
Time=15000 | wen=1 | ren=0 | wdata=01 | rdata=xx | full=0 | empty=0
Time=25000 | wen=1 | ren=0 | wdata=02 | rdata=xx | full=0 | empty=0
Time=35000 | wen=1 | ren=0 | wdata=03 | rdata=xx | full=0 | empty=0
Time=45000 | wen=1 | ren=0 | wdata=04 | rdata=xx | full=1 | empty=0
*** Reading from FIFO ***
Time=55000 | wen=0 | ren=0 | wdata=04 | rdata=xx | full=1 | empty=0
Time=65000 | wen=0 | ren=1 | wdata=04 | rdata=01 | full=0 | empty=0
Time=75000 | wen=0 | ren=1 | wdata=04 | rdata=02 | full=0 | empty=0
Time=85000 | wen=0 | ren=1 | wdata=04 | rdata=03 | full=0 | empty=0
Time=95000 | wen=0 | ren=1 | wdata=04 | rdata=04 | full=0 | empty=1
Testbench completed at time 105000
$finish called from file "testbench7_03.v", line 78.
$finish at simulation time 105000
V C S S i m u l a t i o n R e p o r t
Time: 105000 ps
CPU Time: 0.400 seconds; Data structure size: 0.0Mb
Sat Nov 30 23:19:43 2024
[tc14154@VLSI03 Lab7_03]$ dve -vpd vcdplus.vpd &
[1] 7529
[tc14154@VLSI03 Lab7_03]$
tb_sync_fifo
N/A
N/A
Mate Terminal
DVE - TopLevel.1 - [So...


XQuartz Applications Edit Window Help
Sat Nov 30 11:23 PM
X2GO-tc14154-62-1727925143_stDMATE_dp32
Applications Places System
Sat Nov 30, 23:23
DVE - TopLevel.1 - [Data.1] /home/tc14154/.../Wk9/Lab7_03/vcdplus.vpd
DVE - TopLevel.2 - [Wave.1] /home/tc14154/.../Wk9/Lab7_03/vcdplus.vpd
File Edit View Simulator Signal Scope Trace Window Help
Any Edge
Name
Value
Group1
clk
wen
ren
wdata[7:0]
rdata[7:0]
full
empty
N[31:0]
M[31:0]
New Group
C1:0
REF
0
20000
40000
60000
80000
100000
120000
00
01
02
03
04
8
4
10000
30000
50000
70000
90000
Wave.1
Ready
tb_sync_fifo
N/A
N/A
Mate Terminal
DVE - TopLevel.1 - [D...
DVE - TopLevel.2 - [W...