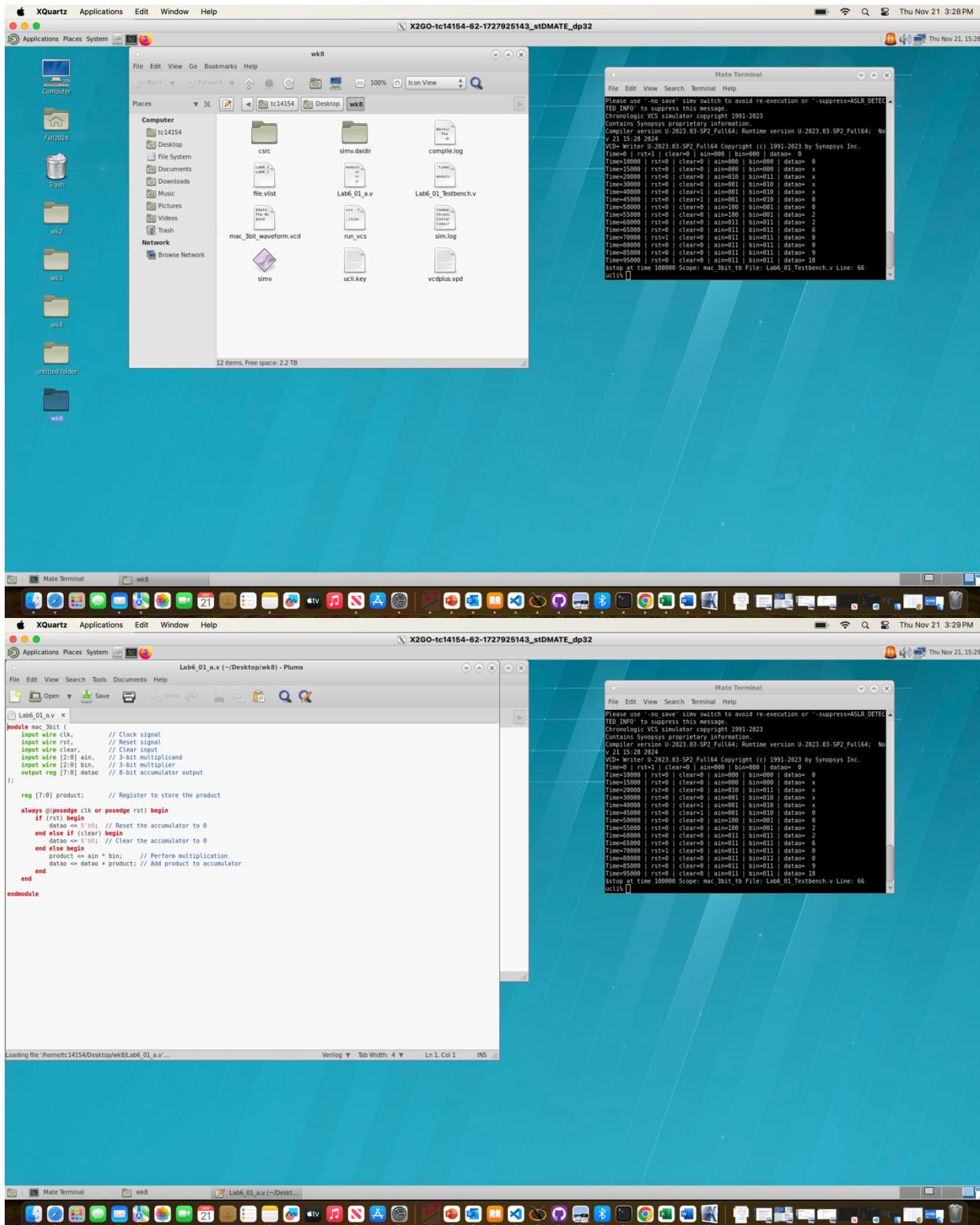
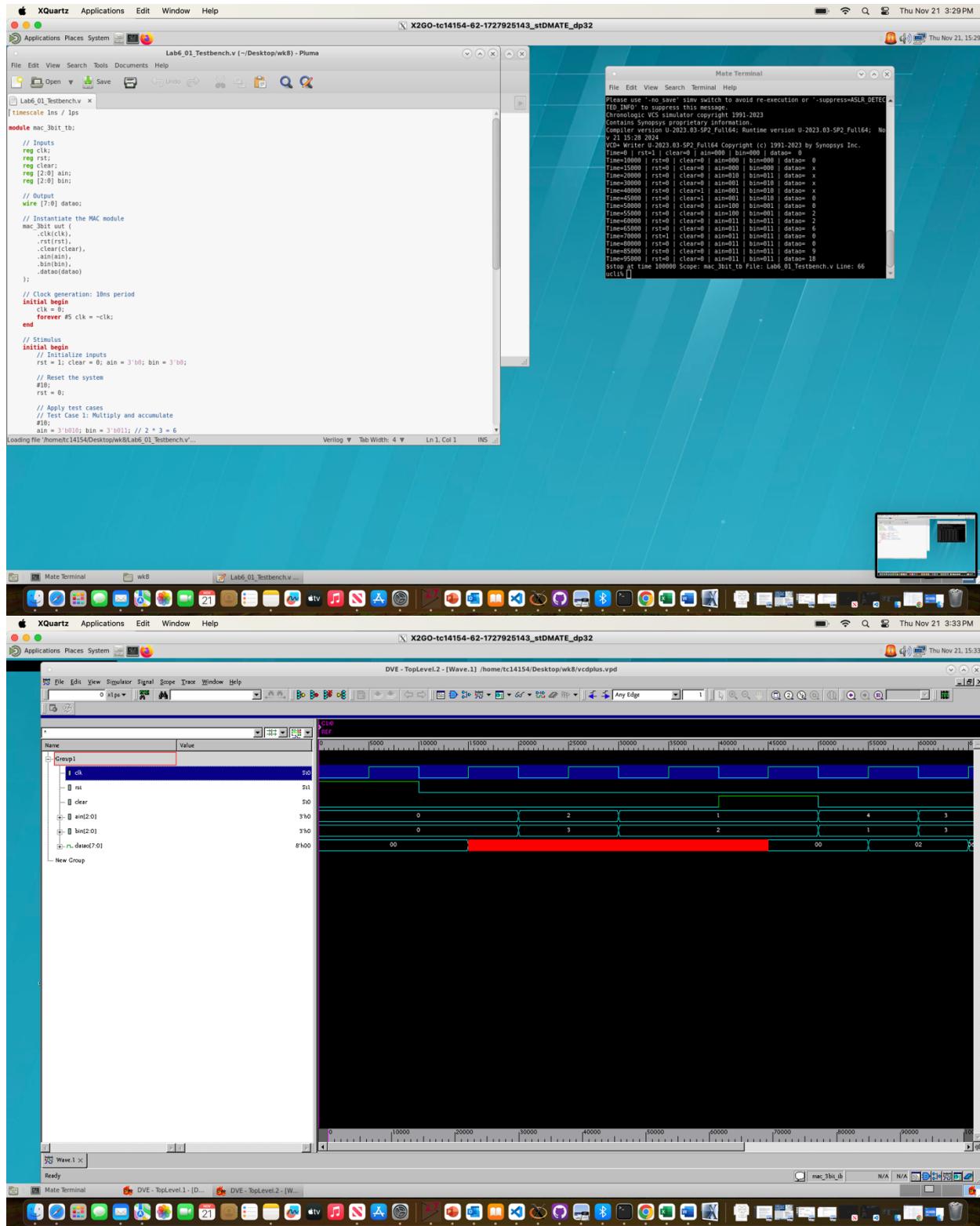
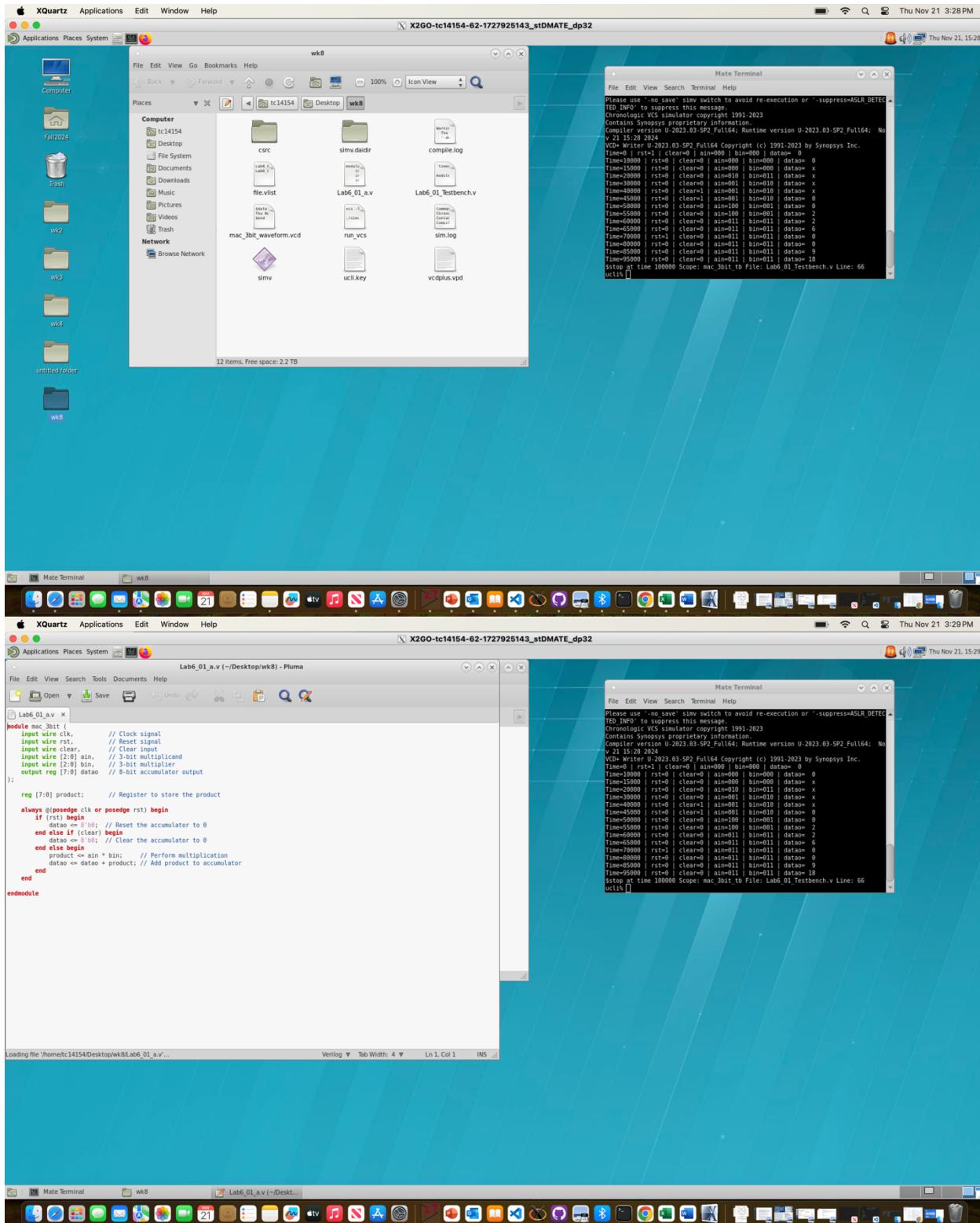
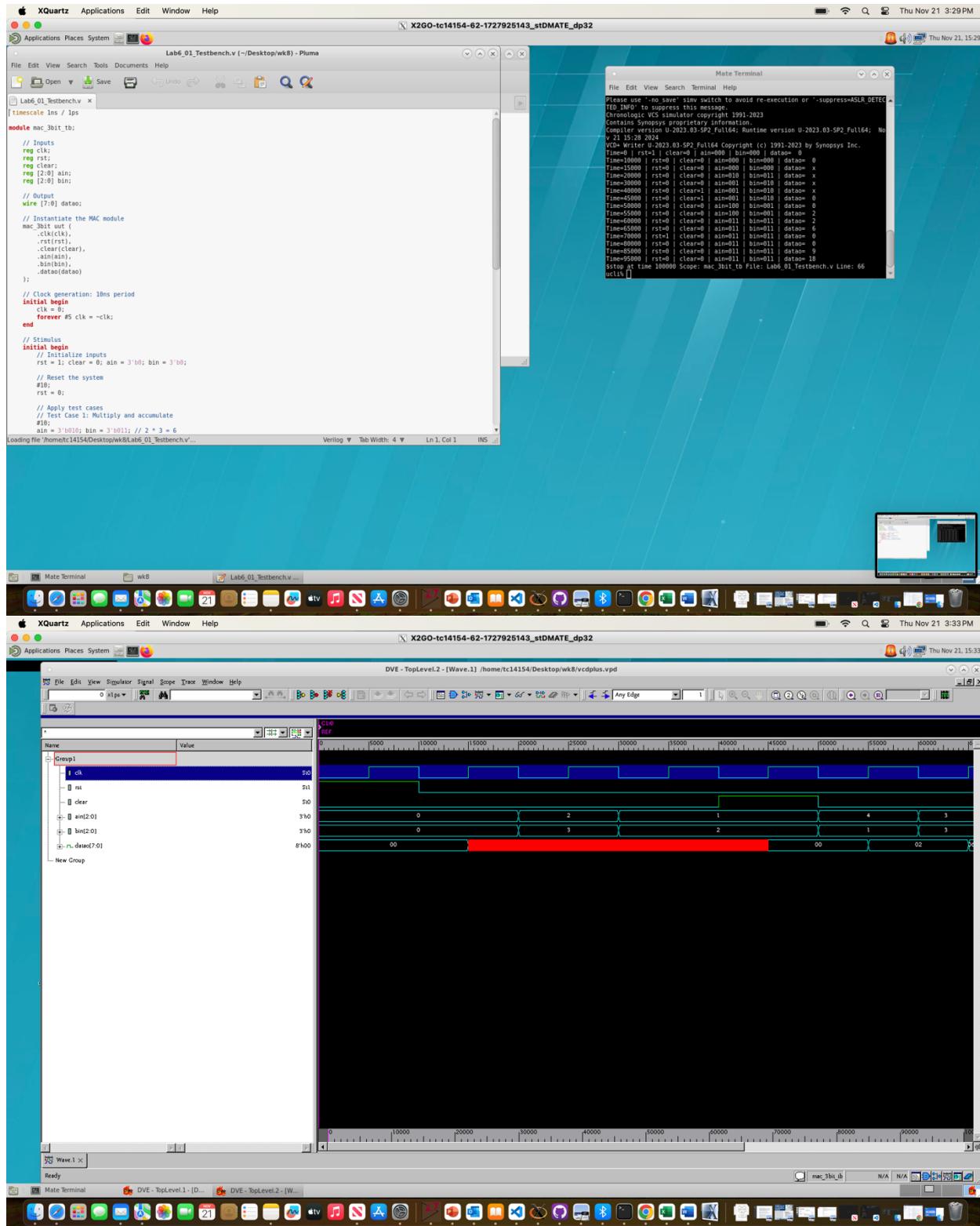


Lab06_01 a and b:









Lab06_02 a and b:

XQuartz Applications Edit Window Help

X2Go Client X2GO-tc14154-62-1727925143_stDMATE_dp32

Lab06_2.v (~/Desktop/wk8/Lab06_2) - Pluma

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Lab06_2.v

```
module data_scrambler_unscrambler (
    input wire clk,
    input wire reset,
    input wire sync,
    input wire bypass,
    input wire [8:0] data_in,
    output reg [7:0] data_out
);
    reg [15:0] lfsr;
    // Polynomial feedback: G(x) = "1" <math>\oplus</math> x<sup>5</sup> <math>\oplus</math> x<sup>4</sup> <math>\oplus</math> x<sup>3</sup> + 1
    wire feedback = lfsr[15] ^ lfsr[4] ^ lfsr[3] ^ lfsr[2] ^ lfsr[0];
    always @ (posedge clk or posedge reset) begin
        if (reset) begin
            lfsr <= 16'hFFFF; // Reset to initial seed
        end else if (sync) begin
            lfsr <= 16'hFFFF; // Reseed when sync is asserted
        end else begin
            lfsr <= (lfsr[14:0], feedback); // Shift LFSR
        end
    end
    always @ (posedge clk) begin
        if (bypass) begin
            data_out <= data_in; // Bypass mode
        end else begin
            data_out <= data_in ^ lfsr[5:8]; // XOR with LFSR for scrambling/unscrambling
        end
    end
endmodule
```

Mate Terminal

```
Nov 21 16:46 lsbasic
lation Report
ds; Data structure size: 0.0Mb
l
d...
ls -l
lisch 2964 Nov 21 16:46 compile.log
lisch 4096 Nov 21 16:46 file.vlist
lisch 923 Nov 21 16:46 Lab06_2.v
lisch 114 Nov 21 16:46 Lab06_2-Testbench.v
lisch 600 Nov 21 16:46 sim.log
lisch 1083 Nov 21 16:46 sim.key
lisch 4096 Nov 21 16:46 simv.daidir
lisch 0 Nov 21 16:46 uclibc.lib
lisch 3082 Nov 21 16:46 vcdplus.vpd
lisch 1380 Nov 21 16:46 waveform.vcd
lisch -vvp vcdplus.vpd &
```

Verilog Tab Width: 4 Ln 1, Col 1 INS ↵

XQuartz Applications Edit Window Help

X2Go Client X2GO-tc14154-62-1727925143_stDMATE_dp32

Lab06_2b_Testbench.v (~/Desktop/wk8/Lab06_2) - Pluma

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Lab06_2b_Testbench.v

```
timescale 1ns / 1ps

module tb_data_scrambler_unscrambler;
    reg clk;
    reg reset;
    reg sync;
    reg bypass;
    reg [7:0] data_in;
    wire [7:0] data_out;

    // Instantiate the module
    data_scrambler_unscrambler dut (
        .clk(clk),
        .reset(reset),
        .sync(sync),
        .bypass(bypass),
        .data_in(data_in),
        .data_out(data_out)
    );

    // Clock generation
    initial clk = 0;
    always #5 clk = ~clk;

    initial begin
        // Initialize Inputs
        reset = 1; sync = 6; bypass = 0; data_in = 8'h00;
        #10 reset = 0; // Deassert reset

        // Test reseed using sync
        #10 sync = 1; #10 sync = 0;

        // Apply input stimulus
        #10 data_in = 8'hAA;
        #10 data_in = 8'h55;
        #10 data_in = 8'hFF;

        // Test bypass functionality
        #10 bypass = 1; data_in = 8'h33;
        #10 bypass = 0;

        // Finish simulation
        #50 $finish;
    end

    // Waveform dump for analysis
    initial begin
        $dumpfile("waveform.vcd");
        $dumpvars(0, tb_data_scrambler_unscrambler);
    end
end
```

Mate Terminal

```
Nov 21 16:46 lsbasic
on R eport
Data structure size: 0.0Mb
l
lisch 2964 Nov 21 16:46 compile.log
lisch 4096 Nov 21 16:46 file.vlist
lisch 32 Nov 21 16:45 file.vlist
lisch 923 Nov 21 16:46 Lab06_2.v
lisch 114 Nov 21 16:46 Lab06_2-Testbench.v
lisch 600 Nov 21 16:46 sim.log
lisch 3082 Nov 21 16:46 vcdplus.vpd
lisch 1380 Nov 21 16:46 waveform.vcd
lisch vcdplus.vpd &
```

Verilog Tab Width: 4 Ln 1, Col 1 INS ↵

