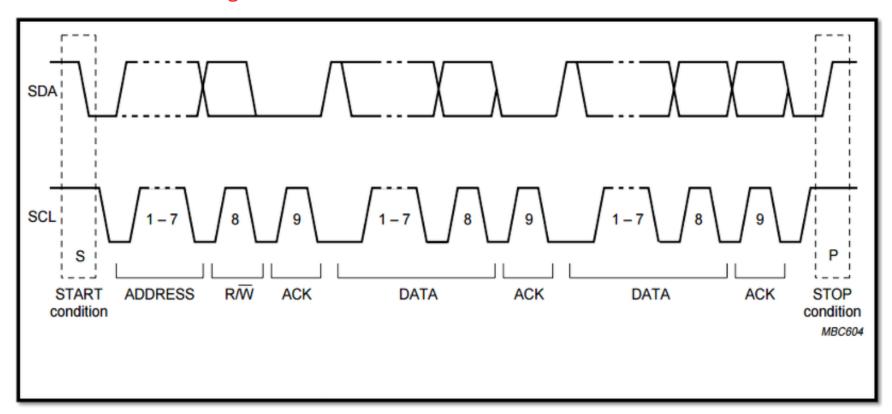




- 1. I2C(Inter-Intergrated Circuit)
- 2. Open-Drain Output (NMOS), Full-Up Register, Wired AND
- 3. Nuvoton NAU7802 FEATURES
- 4. Nuvoton NAU7802 System Block Diagram
- 5. Nuvoton NAU7802 Pin Configuration
- 6. 라즈베리 Setup
- 7. Nuvoton NAU7802 Write / Read Sequence
- 8. Nuvoton NAU7802 Register Setting
- 9. Nuvoton NAU7802 Register
- 10. Circuit diagram
- 11. Operation video

- ✔ 필립스에서 개발한 2개의 신호선으로 다수의 I2C통신을 지원하는 직렬통신방식
- Multi Master, Multi Slave(N:N)
- ✓ Half duplex synchronous
- ✓ 100k, 400k, 3.4Mk(SPI와 UART의 중간)
- ✓ Open-Drain, Wired AND, Full-Up Register
- ✓ 3.3V~5V
- ✓ SDA(Serial Data Line), SCLK(Serial Clock Line)

- ✓ Transmitter, Reciver, Master, Slave
- ✓ Ack(Acknowledge)



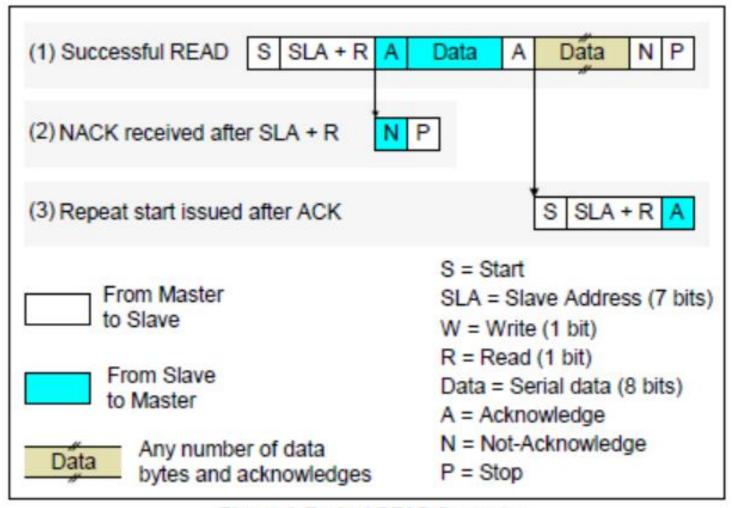


Figure 4. Typical READ Scenarios

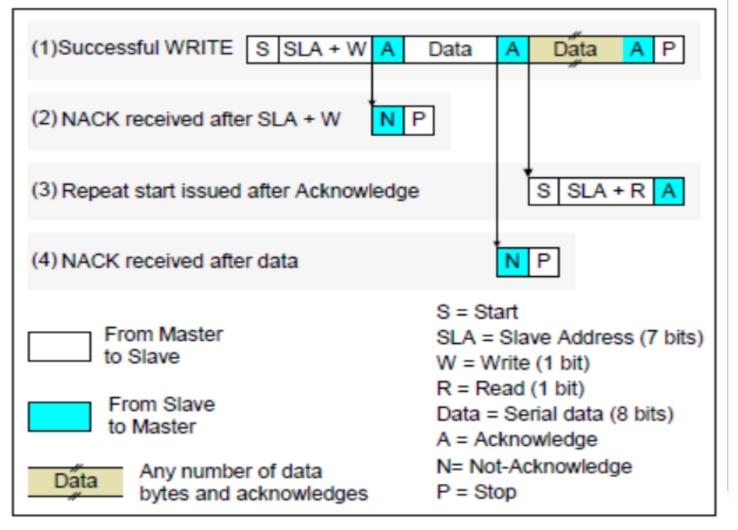
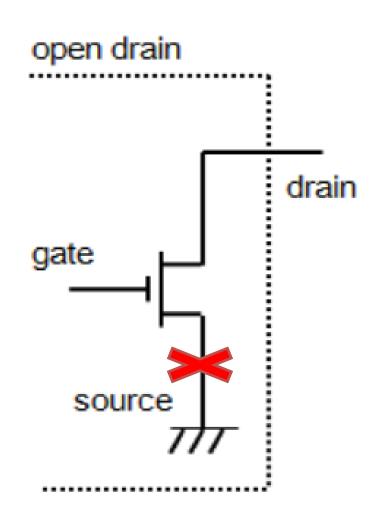


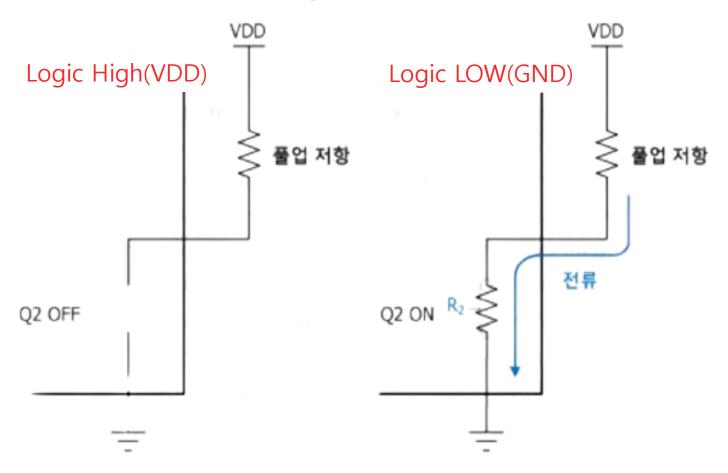
Figure 3. Typical WRITE Transfer Scenarios

Open-Drain Output (NMOS) Full-Up Register Wired AND



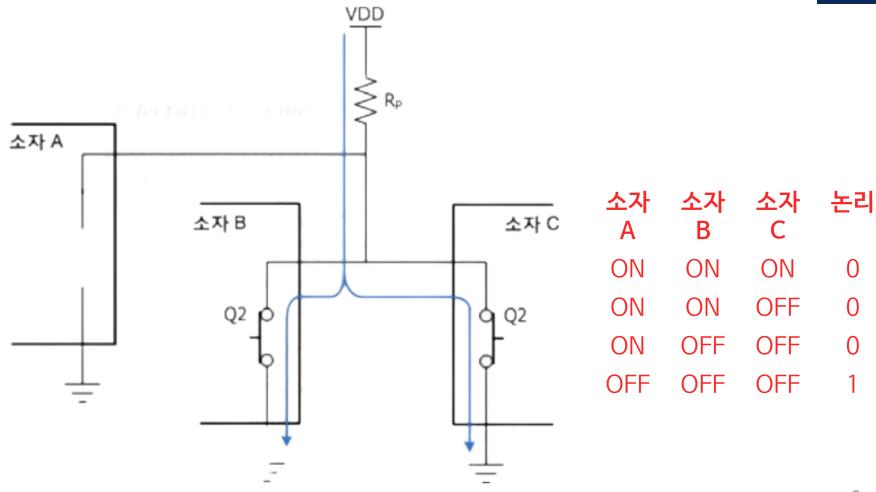
Open-Drain Output (NMOS) Full-Up Register Wired AND

Level Shift, Wired AND

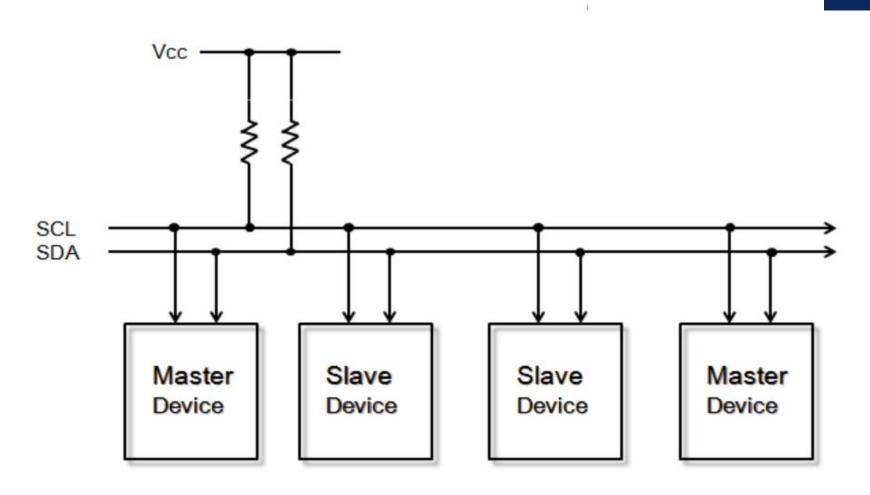


1 12C

Open-Drain Output (NMOS) Full-Up Register Wired AND



Open-Drain Output (NMOS) Full-Up Register Wired AND



Push – Pull Open – Collector Output

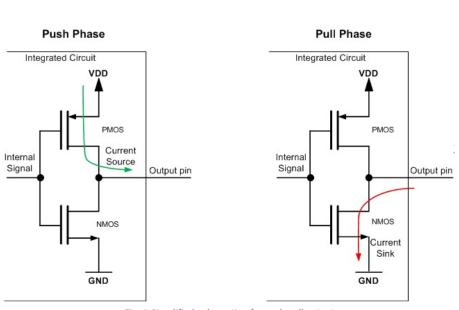
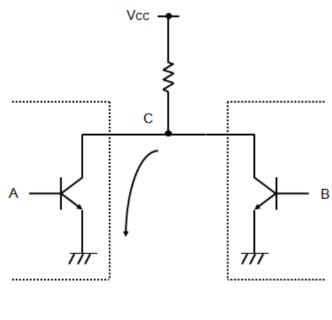


Fig. 1 Simplified schematic of a push-pull output



Α	В	С	C'
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

Nuvoton NAU7802 FEATURES

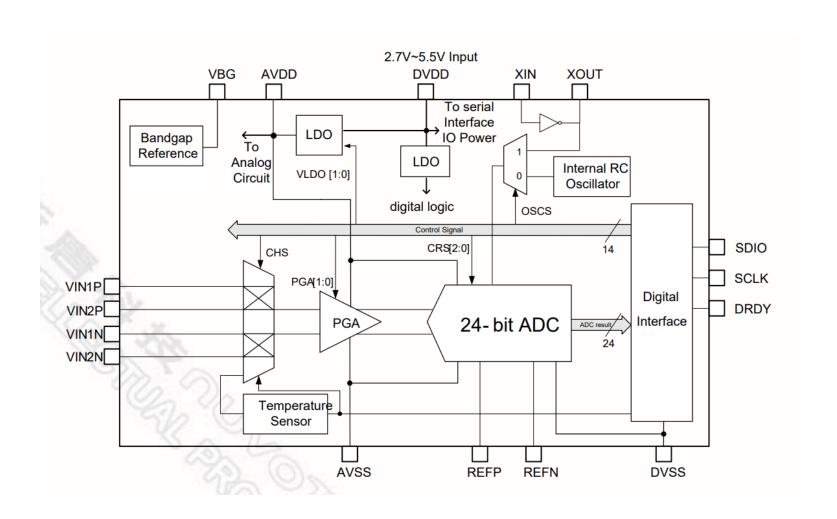
- ✓ Supply Power: 2.7V ~ 5.5V
- ✓ 저전력 24-Bit ADC
- ✓ I2C Interface
- ✓ Sigma-Delta ADC
- ✔ 외부 기준 차동 입력 :0.1V ~ 5V



- 작동 온도: -40° ~ 85°
- ✓ PGA (Programmable Gain Amplifier): 1 ~ 128
- ✓ Slave로만 동작, 표준모드(0~100Khz), 고속모드(0~400Khz)



Nuvoton NAU7802 System Block Diagram



Nuvoton NAU7802 Pin Configuration

ı 12C

PIN DESCRIPTION

Pin No.	Pin Name	Type	DESCRIPTIONS	
1	REFP	Al	Positive reference input	
2	VIN1N	Al	Inverting Input #1	
3	VIN1P	Al	Non-Inverting Input #1	
4	VIN2N	Al	Inverting Input #2	
5	VIN2P	Al	Non-Inverting Input #2	
6	VBG	Α	High impedance Reference Voltage Output and Bypass	
7	REFN	Al	Negative Reference Input	
8	AVSS	Р	Analog Ground	
9	DVSS	Р	Digital ground	
10	XIN	ı	External crystal oscillator input. Typically 4.9152 MHz	
11	XOUT	0	External crystal oscillator output.	
12	DRDY	0	Data Ready Output indicating a conversion is complete and new data are available for readout. (CMOS Driver high / low)	
13	SCLK	ı	Serial Data Clock Input (CMOS open drain output)	
14	SDIO	1/0	Data Input / Output for serial communication with host (CMOS open drain output)	
15	DVDD	Р	Digital power supply: 2.7V ~ 5.5V	
16	AVDD/LDO	P	Analog power supply: 1. From programmable LDO output, low ESR 1 ohm or less capacitor recommended 2. LDO off: external power supply: 2.7V ~ 5.5V	

REFP		1		16	AVDD/LDO
VIN1N		2		15	DVDD
VIN1P		3	SOP-16	14	SDIO
VIN2N		4	(150mil)	13	SCLK
VIN2P		5	or	12	DRDY
VBG		6	DIP-16	11	хоит
REFN		7		10	XIN
AVSS		8		9	DVSS
	- 1				I

Note: TYPE P: Power, Al: Analog input, AO: Analog output, I: input, O: output, I/O: bi-directional

Nuvoton NAU7802 Write / Read Sequence

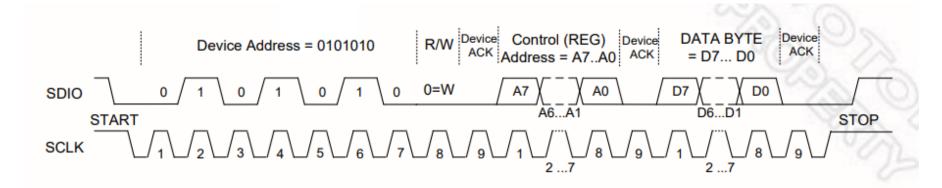


Figure 5: Single Write Sequence

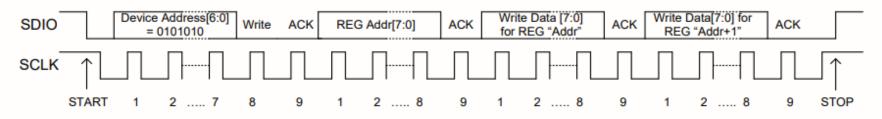


Figure 6: Burst Write Sequence

Nuvoton NAU7802 Write / Read Sequence

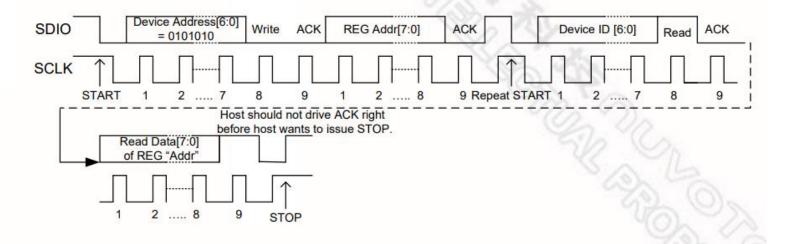


Figure 7: Single Read Sequence

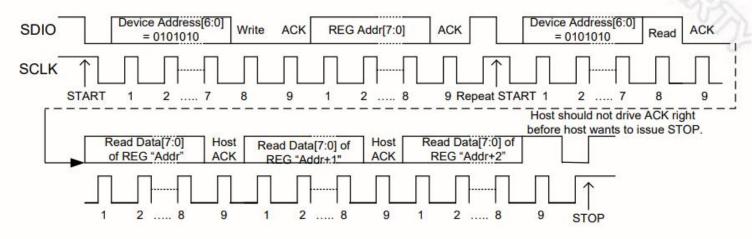


Figure 8: Burst Read Sequence

Nuvoton NAU7802 Register Setting

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	PU CTRL	AVDDS		-	CS	PUR	PUA	PUD	RR	0x00
0x01	CTRL1	CRP		VLDO) [2:0]	1	GAINS[2	2:0]		0x00
0x02	CTRL2	CHS	CRS[1	:0]			CALS	CALMO	OD[1:0]	0x00
0x03	OCAL1_B2	CH1 OF	FSET (Calibra	ation[2	23:16]	10	72.1	1	0x00
0x04	OCAL1_B1	CH1 OF	FSET (Calibra	ation[1	15:8]	-	(6)	~ (0)	0x00
0x05	OCAL1 B0	CH1 OF	FSET (Calibra	ation[7	7:0]		5	0	0x00
0x06	GCAL1 B3	CH1 GA	IN Cali	bratio	n[31:2	4]			00	0x00
0x07	GCAL1 B2	CH1 GA	IN Cali	bratio	n[23:1	6]			2	0x80
80x0	GCAL1_B1	CH1 GA	IN Cali	bratio	n[15:8]			(0x00
0x09	GCAL1_B0	CH1 GA	IN Cali	bratio	n[7:0]					0x00
0x0A	OCAL2_B2	CH2 OF	FSET (Calibra	ation[2	23:16]				0x00
0x0B	OCAL2 B1	CH2 OF	FSET (Calibra	ation[1	15:8]				0x00
0x0C	OCAL2 B0	CH2 OF	FSET (Calibra	ation[7	7:0]				0x00
0x0D	GCAL2 B3	CH2 GAIN Calibration[31:24]					0x00			
0x0E	GCAL2 B2	CH2 GAIN Calibration[23:16]					0x80			
0x0F	GCAL2_B1	CH2 GA	IN Cali	bratio	n[15:8]				0x00
0x10	GCAL2_B0	CH2 GA	IN Cali	bratio	n[7:0]					0x00
0x11	I2C Control	CRSD	FDR	SPE/	WPD	SI	BOPGA	TS / BO	GPCP	0x00
0x12	ADCO B2	ADC_O	JT[23:1	[6]						RO
0x13	ADCO B1	ADC_O	JT[15:8	3]						RO
0x14	ADCO B0	ADC_OUT[7:0]				RO				
0x15	OTP B1	OTP[15:8]				RO				
0x16	OTP_B0	OTP[7:0]							RO
0x1F		Device F	Revisio	n Cod	е					RO

Bit	Name	Description
7	AVDDS	AVDD source select 1 = Internal LDO 0 = AVDD pin input (default)
6	oscs	System clock source select 1 = External Crystal 0 = Internal RC oscillator (default)
5	CR	Cycle ready (Read only Status) 1 = ADC DATA is ready
4	cs	Cycle start Synchronize conversion to the rising edge of this register
3	PUR	Power up ready (Read Only Status) 1 = Power Up ready 0 = Power down, not ready
2	PUA	Power up analog circuit 1 = Power up the chip analog circuits (PUD must be 1) 0 = Power down (default)
1	PUD	Power up digital circuit 1 = Power up the chip digital logic 0 = power down (default)
0	RR	Register reset 1 = Register Reset, reset all register except RR 0 = Normal Operation (default) RR is a level trigger reset control. RR=1, enter reset state, RR=0, leave reset state back to normal state.

```
wiringPil2CWriteReg8(fd, device 주소, bit data) wiringPil2CWriteReg8 (fd, 0x00, 0x01);
```

// RR(1)모든 레지스터 초기화

wiringPil2CWriteReg8 (fd, 0x00, 0x96);

// RR(0) 표준동작, PUD(1) 디지털회로 전원 ON ,PUA(1) 아날로그회로 전원 ON,CS(1) ADC 변환시작, AVDDS(1) 내부AVDD사용

Nuvoton NAU7802 Register Setting

Bit	Name	Description
7	CRP	Conversion Ready Pin Polarity (16 Pin Package Only) 1=CRDY pin is LOW Active (Ready when 0) 0=CRDY pin is High Active(Ready when 1) (default)
6	DRDY_SEL	Select the function of DRDY pin 1: DRDY output the Buffered Crystal Clock if OSCS=1 output the internal OSC clock if OSCS= 0 0: DRDY output the conversion ready (default)
5:3	VLDO	LDO Voltage 111 = 2.4 110 = 2.7 101 = 3.0 100 = 3.3 011 = 3.6 010 = 3.9 001 = 4.2 000 = 4.5 (default)

Bit	Name	Description			
5:4 REG_CHPS		Select the CLK	CHP clock fr	equency.	
		REG_CPHS[1]	REG_CPHS[0]	CLK_CHP clock frequency	
	-0.000	0	0	Reserved	
	EG_CHPS	0	1	Reserved	
	1	0	Reserved		
		1	1	turned off, high ('1') state	

Bit	Name	Description
7	CHS	Analog input channel select 1 = Ch2 0 = Ch1 (default)
6:4	CRS	Conversion rate select 111 = 320SPS 011 = 80SPS 010 = 40SPS 001 = 20SPS 000 = 10SPS (default)
3	CAL_ERR	Read Only calibration result 1: there is error in this calibration 0: there is no error
2	CALS	Write 1 to this bit will trigger calibration based on the selection in CALMOD[1:0] This is an "Action" register bit. When calibration is finished, it will reset to 0 While this bit is still 1, the chip is still calibrating. An I2C write to this bit will be ignored and no additional calibration will be triggered
1:0	CALMOD	11 = Gain Calibration System 10 = Offset Calibration System 01 = Reserved 00 = Offset Calibration Internal (default)

```
wiringPil2CWriteReg8 (fd, 0x01, 0x11);
//VLDO 011(3.6V), 실제로 측정되는 값이 3.3V임
wiringPil2CWriteReg8(fd, 0x02, (Channel<< 7));
//CHS(0)(default)>> CH1,CHS(1)>>CH2
wiringPil2CWriteReg8 (fd, 0x15, 0x30);
//ADC 레지스터 부분, 클럭을 꺼짐('1')상태 설정
```

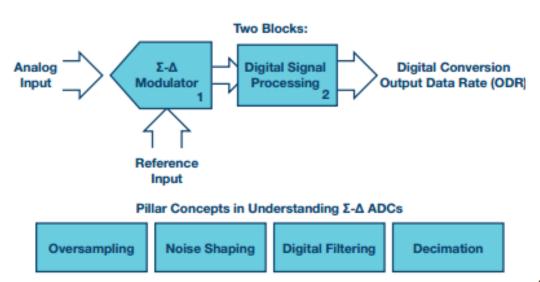
Nuvoton NAU7802 Register

Bit	Name	Description
7	AVDDS	AVDD source select 1 = Internal LDO 0 = AVDD pin input (default)
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1	PUD	Power up digital circuit 1 = Power up the chip digital logic 0 = power down (default)
0	RR	Register reset 1 = Register Reset, reset all register except RR 0 = Normal Operation (default) RR is a level trigger reset control. RR=1, enter reset state, RR=0, leave reset state back to normal state.

```
do
       st = wiringPil2CReadReg8(fd,0x00);
while( st & 0x28 == 0x00 );
 // CR(1) ADC DATA ready, PUR(1) Power Up
    ready
data_H = wiringPil2CReadReg8(fd, 0x12);
 //23:16 상위 비트 읽는 순서 중요!
data_M = wiringPil2CReadReg8(fd, 0x13);
 //15:8 중간 비트
data_L = wiringPiI2CReadReg8(fd, 0x14);
 //7:0 하위 비트
```

11.9 REG0x12-REG0x14: ADC Conversion Result

REG0x12 (Read Only)	ADCO_B2	ADC Conversion Result bit 23 to bit 16
REG0x13 (Read Only)	ADCO_B1	ADC Conversion Result bit 15 to bit 8
REG0x14 (Read Only)	ADCO_B0	ADC Conversion Result bit 7 to bit 0



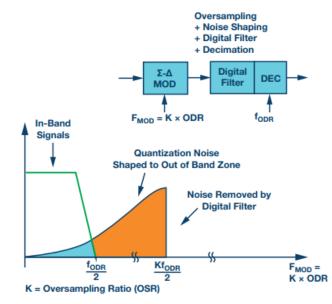
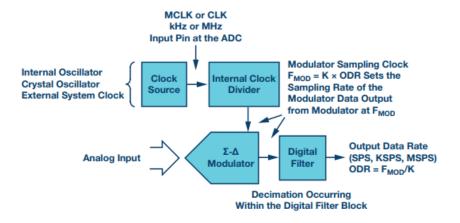


Figure 2c. Σ - Δ ADC scenario. Oversampled and noise shaped, sampling occurring at $F_{MOD} = K \times F_{ODR}$.

Sigma – Delta ADC



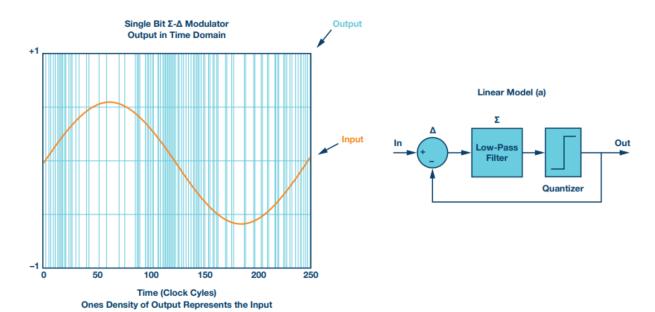
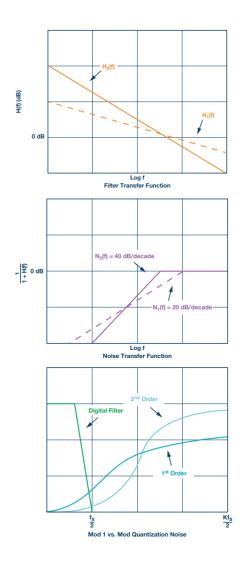
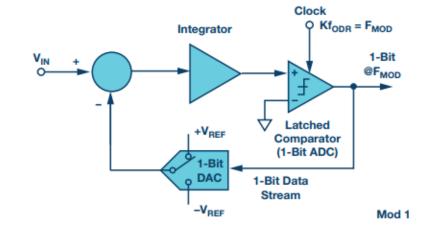
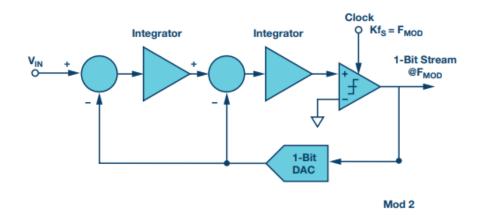


Figure 4. Σ - Δ ones density in response to sine wave input. Linear model (a) of the Mod 1 Σ - Δ loop.

Sigma – Delta ADC







명령어	설명
i2cdetect	이 명령어는 i2c버스에 감지되는 슬레이브 장치가 있는지를 검사하기 위해 사용합니다.
i2cdump	지정한 주소값에해당하는 슬레이브의 전체 레지스터값을 읽어와서 출력해 줍니다.
i2cget	이 명령어는 원하는 슬레이브에서 원하는 레지스터값을 읽어올 때 사용합니다.
i2cset	이 명령어는 i2cget 과 반대로 원하는 슬레이브의 레지스터를 지정해서 값을 레지스터의 값을 변경할 때 사용합니다.

```
sudo apt-get install i2c-tools
```

```
pi@hyojin:~ $ ls -l /dev/i2c*
crw-rw---- 1 root i2c 89,  1 Jan 23 22:49 /dev/i2c-1
crw-rw---- 1 root i2c 89, 20 Jan 23 22:49 /dev/i2c-20
crw-rw---- 1 root i2c 89, 21 Jan 23 22:49 /dev/i2c-21
```

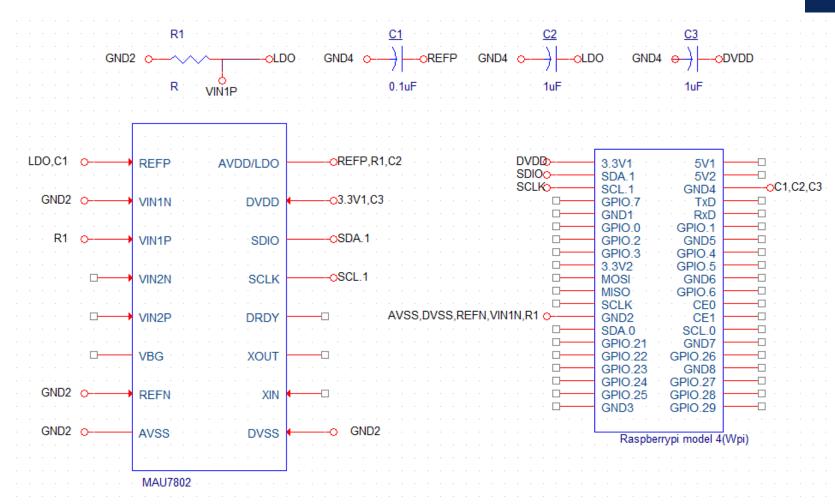
라즈베리 Setup.

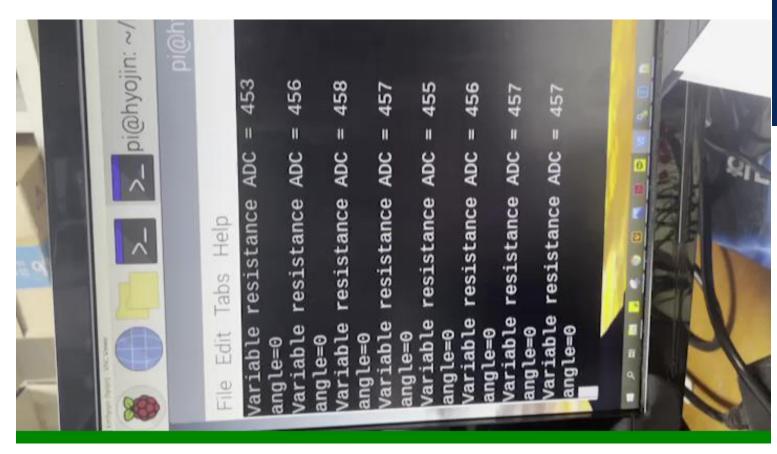
```
int wiringPiI2CSetup(int devld);
               반환값 : 표준리눅스 파일, -1이면 오류
           devld : 연결할 장치의 ID=슬레이브 장치의 주소
       - int wiringPiI2CRead(int fd);
  int wiringPiI2CWrite(int fd, int data);

    int wiringPiI2CWriteReg8(int fd, int reg,

                  int data);
 - int wiringPiI2CWriteReg16(int fd, int reg,
                  int data);
int wiringPiI2CReadReg8(int fd, int reg);
int wiringPiI2CReadReg16(int fd, int reg);
```

12C





문제 I2C(온습도센서), PWM(소프트웨어)로 온도에 따라 각도 변화

