CZ3001
Advanced Computer Architecture

LAMS 4 – Datapath – MIPS pipelined

* 1(a). Consider a non-pipelined machine with 6 execution stages of lengths 50 ns, 50 ns, 60 ns, 60 ns, 50 ns, and 50 ns. Find the clock period of this machine.

Choose one of the following answers.

- 60 ns
- 50 ns
- ✔ 320 ns

The correct answer is 320 ns.

Clock period = 50+50+60+60+50+50= 320 ns

- 110 ns

Marks for this submission: 1/1.

* 1(b) How much time does it take to execute 100 instructions?

Choose one of the following answers.

- 100 ns
- ✔ 32000 ns

The correct answer is 32000 ns

Time taken to execute 100 instructions = 100*320 = 32000 ns

- 5000 ns
- 6000 ns

Marks for this submission: 1/1.

* 1(c) Suppose we introduce pipelining on this machine. Assume that when introducing pipelining, the clock skew adds 5ns of overhead to each execution stage. What is the clock period on the pipelined machine?

Choose one of the following answers.

- 5 ns
- 55 ns
- ✔ 65 ns

The correct answer is 65 ns

Remember that in the pipelined implementation, the length of the pipe stages must all be the same (i.e. the speed of the slowest stage plus overhead). With 5ns overhead it comes to:

The length of pipelined stage = MAX(lengths of unpipelined stages) + overhead = 60 + 5 = 65 ns

Clock period= 65 ns

- 320 ns

Marks for this submission: 1/1.

* 1(d) What is the speedup obtained from pipelining? Assume that there are no stalls.

Choose one of the following answers.

- ✔ 4.92

The correct answer is 4.92

Average instruction time not pipelined = 320 ns
Average instruction time pipelined = 65 ns
Speedup for 100 instructions = 320/65 = 4.92

- 1.08
- 5.33
- 2.5

Marks for this submission: 1/1.

* 2. Name the dependency in the following instruction:
  - ADD X1,X2,X3
  - STUR X1, [X5, #8]

Choose one of the following answers.

✔ ◉ RAW	The correct answer is RAW. The second instruction should only read X1 after the first instruction writes back to X1.
○ WAW	
○ WAR	
○ None of the above	

Marks for this submission: 1/1.

* 3. Name the dependency in the following instruction
  - LDUR X1,[X3, #8]
  - SUB X1, X4, X5

Choose one of the following answers.

- RAW
- ✔ WAW

  The correct answer is WAW.

  The second instruction should only write to X1 after the first instruction writes to X1.
- WAR
- None of the above

Marks for this submission: 1/1.

* 4. We begin with a computer implemented in single-cycle implementation. When the stages are split by functionality, the stages do not require exactly the same amount of time. The original machine had a clock cycle time of 7 ns. After the stages were split, the measured times were IF, 1 ns; ID, 1.5 ns; EX, 1 ns; MEM, 2 ns; and WB, 1.5 ns. The pipeline register delay is 0.1 ns.

4(a) What is the clock cycle time of the 5-stage pipelined machine?

Choose one of the following answers.

- 1 ns
- 2 ns
- 1.1 ns
- ✔ 2.1 ns

The correct answer is 2.1 ns

2 ns + 0.1 ns = 2.1 ns

Marks for this submission: 1/1.

* 4(b) If there is a stall after every 4 instructions, what is the CPI of the new machine? Here, a stall means stop of pipeline for one clock cycle.

Choose one of the following answers.

- 1
- 2
- ✔ 1.25

The correct answer is 1.25.

- Steady state CPI = (No of instructions + no of stalls)/no of instructions
- (4+1)/4 instructions = 1.25

- 1.5

Marks for this submission: 1/1.

* 4(c) What is the speedup of the pipelined machine over the single-cycle machine?

Choose one of the following answers.

- 3.33
- 0.3
- ✔ 2.67

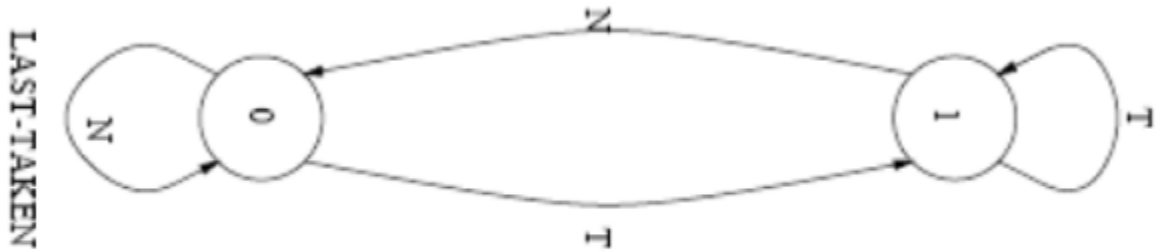
The correct answer is 2.67.

- Execution Time = I × CPI × Cycle period
- Speedup = (I × 1 × 7(non-pipelined))/(I × 1.25 × 2.1(pipelined)) = 2.67

- 0.375

Marks for this submission: 1/1.

* 5. Calculate the prediction accuracy for the last taken 1 bit predictor. The execution pattern for the branch is NTNNTTTN. Note that the starting point is “not taken”.



Choose one of the following answers.

✔ 0.5

The correct answer is 0.5

exe. Time	outcome	state	prediction	
0	N	0	N	Correct
1	T	0	N	Incorrect
2	N	1	T	Incorrect
3	N	0	N	Correct
4	T	0	N	Incorrect
5	T	1	T	Correct
6	T	1	T	Correct
7	N	1	T	Incorrect

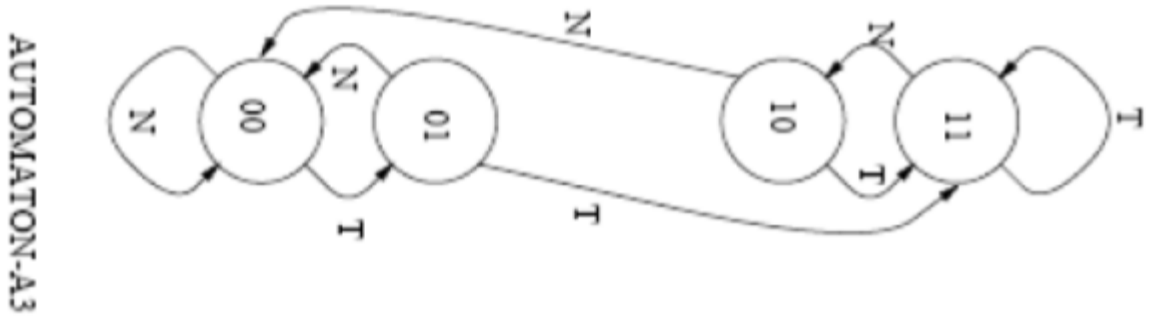
0.6

1

0.2

Marks for this submission: 1/1.

* 6. Calculate the prediction accuracy for the 2 bit predictor. The execution pattern for the branch is NTNNTTTN. Note that the starting point is "01".



Choose one of the following answers.

- 0.6
- ✔ 0.5

The correct answer is 0.5

Execution Time	Branch Execution	State Before	Prediction	Correct or Incorrect	State After
0	N	01	NT	Correct	00
1	T	00	NT	Incorrect	01
2	N	01	NT	Correct	00
3	N	00	NT	Correct	00
4	T	00	NT	Incorrect	01
5	T	01	NT	Incorrect	11
6	T	11	T	Correct	11
7	N	11	T	Incorrect	10

- 1
- 0.2

Marks for this submission: 1/1.