Designing with STM32F7 Family

Course Description

Designing with STM32F7 Family is a 3 days ST official course.

The course provides all necessary theoretical and practical know-how for start developing platforms based on STM32F7xx families with STMCube.

The course begins with an introduction to STM32 microcontroller family's roadmap and focuses on Cortex-M7 architecture.

The course continues with an in-depth study of the memory organization, bus architecture, reset and clock controller, interrupts handling, low power modes, hardware semaphore, MDMA, security, and most of the SoC peripherals such as clocks, reset, power, embedded Flash, FMC, NVIC, EXTI, GPIO, ADC, USART, DAC, SPI, USB, DMA, CRC, I2C, CAN, RTC, IWDG, WWDG, TIM, LPTIM, SAI, HDMI, DCMI, crypto processor, Hash processor, RNG and debug.

The course also employs hardware and software design tools, and combines 50% theory with 50% practical work in every meeting.

Course Duration

3 days

Goals

1. Become familiar with STM32F7 families
2. Become familiar with ARM Cortex-M7 architecture
3. Understand the bus and memory topology to get the best performance
4. Become familiar with STM32F7 peripherals
5. Become familiar with hardware and software design tools
6. Build a new project using the STMCube
7. Work with Firmware libraries

Target Audience

Software engineers who would like start developing with STM32F7xxx microcontrollers

Prerequisites

- Computer architecture background
- Experience in C programming
- Experience in developing embedded systems

Course Material

- STMCube
- ST Eval board: 32F723EDISCOVERY
- Course book (including labs)

Agenda

Day #1

- **STM32F7 Series Overview**
  - STM32F7 block diagram
  - STM32F7 product series

- **STM32F7 System Architecture**
  - System architecture overview
  - AXI and AHB bus matrices
  - TCM buses
  - Bus bridges
  - Inter-domain buses
  - Cortex-M7 busses (AXIM, ITCM, DTCM, AHBS, AHBP)
  - Bus master peripherals

- **STM32F7 Memory Organization**
  - Memory map
  - Embedded SRAM (D1, D2, D3 domains, TCMs)
  - ECC
  - Embedded Flash
  - Boot configuration
  - Embedded bootloader

- **STM32F7 Embedded Flash**
  - Main features supported
  - Flash block diagram
  - Protection mechanism
  - Flash programming/erase/read operations
  - Flash parallel operations
  - ECC and CRC
  - Flash bank and register swapping
  - Clock and reset management
  - Flash option bytes
  - Low power modes
  - interrupts

- **STM32F7 Reset & Clock Control (RCC)**
  - Main features supported

- RCC block diagram
- Which sources can generate reset?
- Power-on/off reset
- System reset
- Local reset
- Identifying reset source
- Low power mode security reset
- Backup domain reset
- Power-on wakeup sequence
- Boot from pin reset
- Boot from system standby
- Clock generators (HIS, HSE, LSE, LSI, CSI, HSI48)
- Clock security system (CSS)
- Clock output generation
- PLLs
- System clock selection & generation
- Clock generators behavior in stop and standby modes
- Peripheral allocation and clock gating control
- CPU and bus matrix clock gating control
- RCC interrupts

STM32F7 System Power Control (PWR)

- Main features
- Power supply schemes
- VDDUSB
- Supply monitoring and reset circuitry
- Power supply supervisor
- Backup domain
- Voltage regulator and internal reset modes
- Voltage regulator and operating modes
- Voltage regulator ON
- Sleep and Low-power sleep modes
- Sleep Now!
- Sleep on exit
- Low power modes description
- Low power modes transitions
- Voltage scaling
- Power consumption figures
- LSE new modes (STM32F7x6)
- Option bytes
- Debug information

Day #2

- **STM32F7 DMA Controller (DMA)**
  - DMA main features
  - Individual channel flexibility
  - Channel transfer management
  - STM32F7 instances
  - DMA1 controller
  - DMA2 controller
  - Interrupts

- **STM32F7 Basic Extended CAN Interface (bxCAN)**
  - CAN overview
  - BxCAN block diagram
  - BxCAN features
  - BxCAN operating modes
  - BxCAN test modes
  - BxCAN interrupts
  - CAN related peripherals

- **STM32F7 General Purpose I/O (GPIO)**
  - Key features
  - Operating modes
  - Alternate functions
  - Special considerations for I/O pins
  - Special considerations for HSE/LSI pins
  - Multi-supply I/O pins

- **STM32F7 NVIC and EXTI**
  - NVIC features
  - SysTick calibration value register
  - Interrupt and exception vectors
  - Exception entry and return
  - EXTI main features
  - EXTI block diagram
  - Wakeup event management
  - Hardware interrupt selection
  - Hardware event selection
  - Software interrupt/event selection

- External interrupt/event line mapping

- **STM32F7 Flexible Memory Controller (FMC)**
  - FMC features
  - FMC block diagram
  - AHB and AXI interfaces
  - Supported memories and transactions
  - External device address mapping
  - NOR Flash/PSRAM controller
  - Synchronous and asynchronous transactions
  - NAND Flash controller
  - NAND Flash supported memories and transactions
  - NAND Flash operations
  - NAND Flash prewait feature
  - ECC in NAND Flash
  - SDRAM controller
  - SDRAM memory organization
  - SDRAM initialization
  - SDRAM controller write cycle
  - SDRAM controller read cycle
  - Row and bank boundary management
  - Memory latency computation
  - SDRAM controller refresh cycle
  - Low power modes (self-refresh, power down)

- **STM32F7 CRC**
  - CRC main features
  - Secure access mode
  - CRC block diagram
  - Input and output format
  - Performance

- **STM32F7 True Random Number Generator (RNG)**
  - RNG main features
  - RNG block diagram
  - Random number generation
  - RNG initialization
  - Normal operations
  - Low power operations
  - RNG clocking
  - Error management

- RNG low power usage
- RNG interrupts
- RNG processing time
- Entropy source validation

- **STM32F7 Cryptographic Processor (CRYP)**
  - CRYP main features
  - CRYP block diagram
  - CRYP DES/TDES cryptographic core
  - CRYP AES cryptographic core
  - CRYP stealing and data padding
  - Suspend/resume operations
  - ECB, CBC chaining modes
  - AES counter mode
  - CRYP data registers and data swapping
  - DMA interface
  - CRYP interrupts
  - CRYP processing time

- **STM32F7 Hash Processor (HASH)**
  - HASH main features
  - HASH block diagram
  - Hash algorithms
  - Message data feeding
  - Message digest computing
  - Message padding
  - HMAC processing
  - Context swapping
  - HASH DMA interface
  - HASH interrupts
  - HASH processing time

Day #3

- **STM32F7 ADC**
  - ADC main features
  - ADC block diagram
  - High performance features
  - ADC conversion speeds
  - Sampling times
  - ADC clocks
  - ADC conversion modes
  - Analog watchdog
  - Data transfers
  - Injected conversions
  - Interrupts
  - DMA requests
  - Related peripherals
  - Features for each individual ADC (ADC1/2/3)

- **STM32F7 DAC**
  - DAC main features
  - DAC block diagram
  - DAC with output buffer
  - DAC data formats
  - DAC conversion triggers
  - DAC output voltage
  - DAC trigger selection
  - DMA requests
  - Noise generation
  - Triangle wave generation
  - DAC channel modes
  - DAC interrupts

- **STM32F7 Digital Camera Interface (DCMI)**
  - DCMI features
  - DCMI block diagram
  - DCMI data transfer
  - DCMI extended data mode
  - DCMI capture mode
  - DCMI CROP feature

- **STM32F7 HDMI-CEC**
  - HDMI-CEC v2 controller features
  - HDMI-CEC controller block diagram
  - HDMI-CEC interrupts
  - RX tolerance margins
  - Errors handling
  - Bit timing error detection
  - Signal Free Time (SFT) configuration
  - Message structure
  - SFT option bit
  - CEC v2 differences

- **STM32F7 Independent Watchdog (IWDG)**
  - IWDG features
  - IWDG block diagram
  - Configuring IWDG hardware start
  - Configuring IWDG software start
  - IWDG settings and reset flag
  - Window option
  - Behavior in Stop and Standby modes
  - Low power freeze
  - Register access protection
  - Debug mode

- **STM32F7 Window Watchdog (WWDG)**
  - WWDG features
  - WWDG block diagram
  - Enabling the watchdog
  - Controlling the downcounter
  - WWDG settings and reset flag
  - Advanced watchdog interrupt feature
  - Low power modes
  - How to program the watchdog timeout
  - Debug mode

- **STM32F7 Universal Synchronous Asynchronous Receiver Transmitter (USART)**
  - USART features
  - Extended capability
  - USART block diagram
  - USART character description
  - USART FIFOs and thresholds
  - USART transmitter & receiver
  - USART baud rate generation
  - USART auto baud rate detection
  - USART multiprocessor communication
  - USART Modbus communication
  - USART parity control
  - USART LIN mode
  - USART synchronous mode
  - USART smartcard mode
  - USART IrDA SIR
  - USART and DMA
  - RS232 and RS485 support
  - USART low power management
  - USART interrupts

- **STM32F7 Serial Peripheral Interface (SPI) and I2S**
  - SPI features
  - SPI block diagram
  - Communications between one master and one slave
  - Standard multi-slave communication
  - Multi-master communication
  - Slave select pin management
  - Communication formats
  - SPI data transmission and reception procedures
  - Data packing
  - Disabling SPI
  - Communication using DMA
  - SPI modes and control
  - CRC computation
  - Low power mode management
  - SPI wakeup and interrupts
  - I2S main features
  - Pin sharing with SPI function
  - Slave and master modes

- Supported audio protocols
- Internal FIFOs
- Frame error detection
- DMA interface
- I2S wakeup and interrupts

- **STM32F7 USB 2.0 On-The-Go High Speed (OTG HS)**
  - Main features
  - Host mode features
  - Peripheral-mode features
  - OTG block diagram
  - OTG dual role device
  - USB peripheral
  - USB host
  - SOF trigger
  - OTG low power modes
  - USB data FIFOs
  - OTG_HS interrupts

- **STM32F7 Serial Audio Interface (SAI)**
  - SAI main features
  - SAI block diagram
  - Free protocol modes (I2S, TDM, PCM, master, slave)
  - Slot configuration
  - Sampling rate adjustment
  - SAI synchronization
  - Companding
  - Mute mode
  - Anticipated/late frame error
  - Overrun/underrun handling
  - SPDIF protocol
  - AC'97 protocol
  - Interrupts
  - DMA requests
  - Application examples

- **STM32F7 Debug**
  - Debug main features
  - Debug infrastructure block diagram
  - Clock domains and reset
  - ID codes and locking mechanism

- JTAG debug port
- Serial wire (SW) debug port
- AHB Access ports (AHB-AP)
- Core debug
- Debug under system reset
- Flash Patch Breakpoint (FPB)
- Data Watchpoint Trigger (DWT)
- Instrumentation Trace Macrocell (ITM)
- Embedded Trace Macrocell (ETM)
- MCU debug component (DBGMCU)
- System ROM tables
- Trace port interface unit (TPIU)