Makefile

Make

- ☐ Make :

- ☐ Make   :

- ☐   make

  .

  - ● ,

  - ●

- ☐ Makefile : make   application
     make   .

- ☐   : make [-f makefile] [option] … target …

Makefile

☐ Makefile   .

☐ Make file   (target),   (dependency),
   (command)   .

● (target) :   .
    object   . (
                            action   )

● (dependency) : target

● (command) : make   action.
                                  .   . (
        shell   )

```
)  target  ...: dependency ...
        command
        ...
```
←

☐   command   Tab   .   Tab
   target   command   .

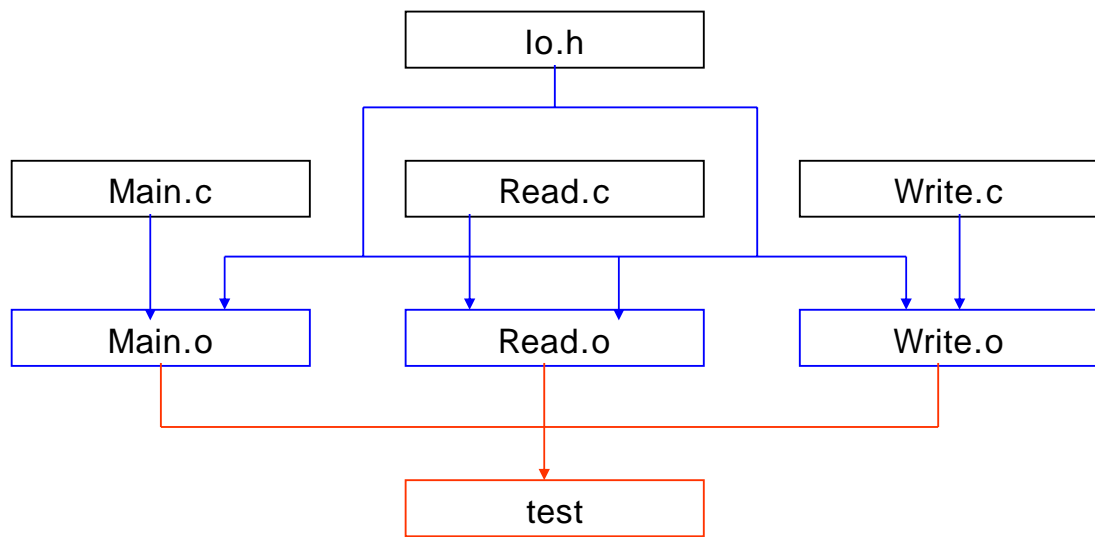☐   application

                    .
            .

☐ Mskefile

test : main.o read.o write.o
    gcc - o test main.o read.o write.o

main.o : io.h main.c
    gcc - c main.c

read.o : io.h read.c
    gcc - c read.c

write.o: io.h write.c
    gcc - c write.c

target

- command   dependencies
  dependencies   target
       .

- target   command   dependencies
              .   `clean'   target
  command   dependencies

- makefile   targets(
)
             .   target   dependencies
  target   .

- default goal
       . Default goal
  tartget   .   target
              makefile   .

Macro

□
- MacroName = macro-content

□
- ${MacroName}

□ Macro

□ Make macro makefile
.
.

□ Pre-defined macro
- Make –p make (,
) .

Macro

```
OBJECTS = main.o read.o write.o
SRCS = main.c read.c write.c          <-

CC = gcc                              <- gcc
CFLAGS = -g -c                        <- gcc           -g

TARGET = test                         <-              test

$(TARGET) : $(OBJECTS)
      $(CC) -o $(TARGET) $(OBJECTS)

lean :
      rm -rf $(OBJECTS) $(TARGET)

main.o : io.h main.c                  <- (1)       macro CFLAGS    setting
read.o : io.h read.c                  <-           make
write.o: io.h write.c
```

□   Make   makefile

□   make

□   pre-defined macro   default
                                              make
      make   .

□   makefile
             .

□   Macro   (1)   .
)   > ls
         sample.c
         > make sample
         cc sample.c –o sample
         > ls
         sample sample.c

---

macro

□   .
      makefile
                                               (suffix)

□   macro : .SUFFIX
    ●   Makefile   .
    ●   : .SUFFIX: old_suffix .new_suffix
        ➢   : .SUFFIX: .c.o

□   macro :   macro   . Macro
       ,   macro.
    ● $* <-   (Target)
    ● $@ <-   (Target)
    ● $< <-
    ● $? <-   (Target)   list

macro

main.o : main.c io.h

    gcc - c $*.c

☐ $* $*   main

    .

test : $(OBJS)

    gcc - o $@ $*.c

☐ $@   .   test   .

.c.o :

    gcc - c $< (gcc - c $*.c)

☐ $<

    . .o   .c   .

      main.o   main.c   main.c $<