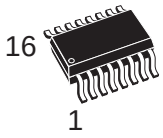
# CRX14

## Low Cost ISO14443 type-B Contactless Coupler Chip with anti-collision, CRC management and anti-clone function

**PRELIMINARY DATA**

- Single 5V ±500mV Supply Voltage
- SO16N package
- Contactless Communication
  - ISO14443 type-B protocol
  - 13.56MHz Carrier Frequency using external oscillator
  - 106Kbit/sec data rate
  - 36 bytes Input/Output frame register
  - Support Frame Answer with/without SOF/EOF
  - CRC generation and check
  - France Telecom Proprietary Anti-Clone Function
  - Automated ST anti-collision exchange
- I²C Communication
  - Two Wire I²C Serial Interface
  - Supports 400 kHz Protocol
  - 3 Chip Enable pin
  - Up to 8 CRX14 connected on the same bus

**Figure 1. Delivery Forms**




SO16 Narrow (MQ)

**Figure 2. CRX14 Pad Connections**

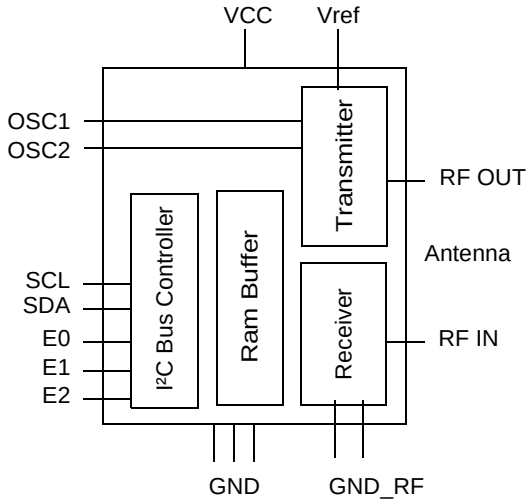



**Table 1. Signal Names**

| | |
|---|---|
| RF OUT | Antenna Output Driver |
| RF IN | Antenna Input Filter |
| VCC / GND | Power Supply & Ground |
| GND_RF | Ground for RF circuitry |
| OSC1 / OSC2 | Oscillator input |
| Vref | Transmitter Reference Voltage |
| SCL | I²C Clock |
| SDA | I²C Bi-Directional Data |
| E0 | I²C Chip Enable |
| E1 | I²C Chip Enable |
| E2 | I²C Chip Enable |

### DESCRIPTION

The CRX14 is a contactless coupler compliant with the short range ISO14443 type-B standard controlled using the two wire I²C bus.

The CRX14 generates a 13.56MHz signal on a external antenna. Transmitted data are modulated using Amplitude Shift Keying modulation signal (ASK). Received data are demodulated from the PICC (Proximity integrated Coupling Card) load variation signal, generated on the antenna, using Bit Phase Shift Keying coding (BPSK) of a 847kHz sub-carrier. The Transmitted ASK wave is 10% modulated. The Data transfer rate between the CRX14 and the PICC is 106Kbit/s in both transmission and reception modes.

The CRX14 follows the ISO14443 type-B recommendation for Radio frequency power and signal interface.

## DESCRIPTION (CONT'D)

The CRX14 targets short range applications which need disposable or secured and re-usable products. The CRX14 includes an automated anti-collision mechanism which allowed to detect and select ST short range memory present at the same time in the CRX14 range. The anti-collision is based on the STMicroelectronics probabilist scanning methodology. The CRX14 provides an anti-clone function from FRANCE TELECOM which allows ST short range memory authentication. With the use of the single chip coupler CRX14, it is easy to design a reader with the authentication capability and get a final application with a high level of security at low cost.

The CRX14 provide a complete analog interface compliant with the ISO14443 type-B recommendations for Radio frequency power and signal interface. It allows to power and control data transmission of any ISO14443 type-B PICC products through a simple antenna. The CRX14 is fabricated with STMicroelectronics High Endurance Single Polysilicone CMOS technology.

The CRX14 is organized as 4 different blocks:

– The I²C bus controller handle the serial connection with the application host. It is compliant with the 400kHz I²C bus specification and it controls the read/write access to all the CRX14 registers.

– The RAM buffer is bi-directional. It stores all the request frame bytes to be transmitted to the PICC and all received bytes send by the PICC on the answer frame.

– The transmitter powers PICCs by generating a 13.56MHz signal on an external antenna. The resulting field is 10% modulated using ASK (amplitude shift keying) modulation for outgoing data.

– The receiver demodulates the signal generated on the antenna by the load variation of the PICC. The resulting signal is decoded by a 847KHz BPSK (binary phase shift keying) sub-carrier decoder.

The CRX14 is designed to be connected to a digital host (Microcontroller or Asic) which will have to manage all the communication protocol in both transmit and receive mode through the I²C serial bus.

**Table 2. Absolute Maximum Ratings (Target Data. Can be updated during product qualification)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient Operating Temperature | -20 to 85 | °C |
| $T_{STG}$ | Storage Temperature (for SO16N package) | -65 to 150 | °C |
| $T_{LEAD}$ | Lead Temperature, Soldering SO16N 40 sec | 215 | °C |
| $V_{IO}$ | Input or Output range (SDA) | -0.3 to 6.5 | V |
| $V_{IO}$ | Input or Output range (others pads) | -0.3 to Vcc+0.3 | V |
| $V_{CC}$ | Supply Voltage | -0.3 to 6.5 | V |
| $P_{OUT}$ | Output Power on Antenna Output Driver (RF OUT) | 100 | mW |
| $V_{ESD}$ | Electrostatic Discharge Voltage (Human Body model) (2) | 2000 | V |
| | Electrostatic Discharge Voltage (Machine model) (3) | 200 | V |

Notes 1) Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

2) MIL-STD-883C, 3015.7 (100pF, 1500 Ω)

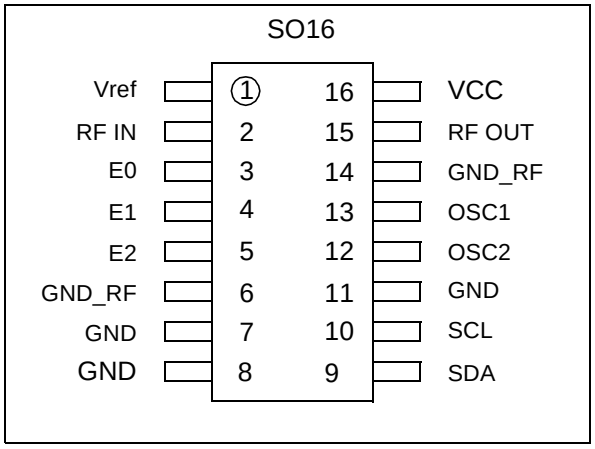
3) EIAJ IC-121 (Condition C) (200pF, 0 Ω)

## SIGNALS DESCRIPTION

### Oscillator (OSC1, OSC2).

These pins are internally connected to the on-chip oscillator circuit. A 13.56MHz quartz must be connected between these 2 pins in order to allow the correct CRX14 operation. The Osc1 pin is the input pin, the Osc2 is the output pin. When an external clock is used, it must be applied on Osc1 and Osc2 must be left open.

**Figure 3. CRX14 Pin Connection**




### Antenna Output Driver (RF OUT).

This pin must be connected to the antenna circuitry as shown in Figure 4. The LRC antenna circuitry must be connected between the RF OUT pin and GND. This pin generates the modulated 13.56MHz signal on the antenna. Care must be taken as it does not support short-circuit.

### Antenna Input Filter (RF IN).

This is the antenna input filter of the CRX14. It must be connected to the external antenna as shown in Figure 4 throught an adaptation circuitry. The input filter demodulates the signal generated on the antenna by the load variation of the PICC. The resulting signal is then decoded by the 847kHz BPSK decoder.

### Transmitter Reference Voltage (Vref)

The Vref input provides a reference voltage used by the output driver for ASK modulation. It must be connected to an external capacitor as shown on Figure 4.

**Figure 4. CRX14 Application Schematic**

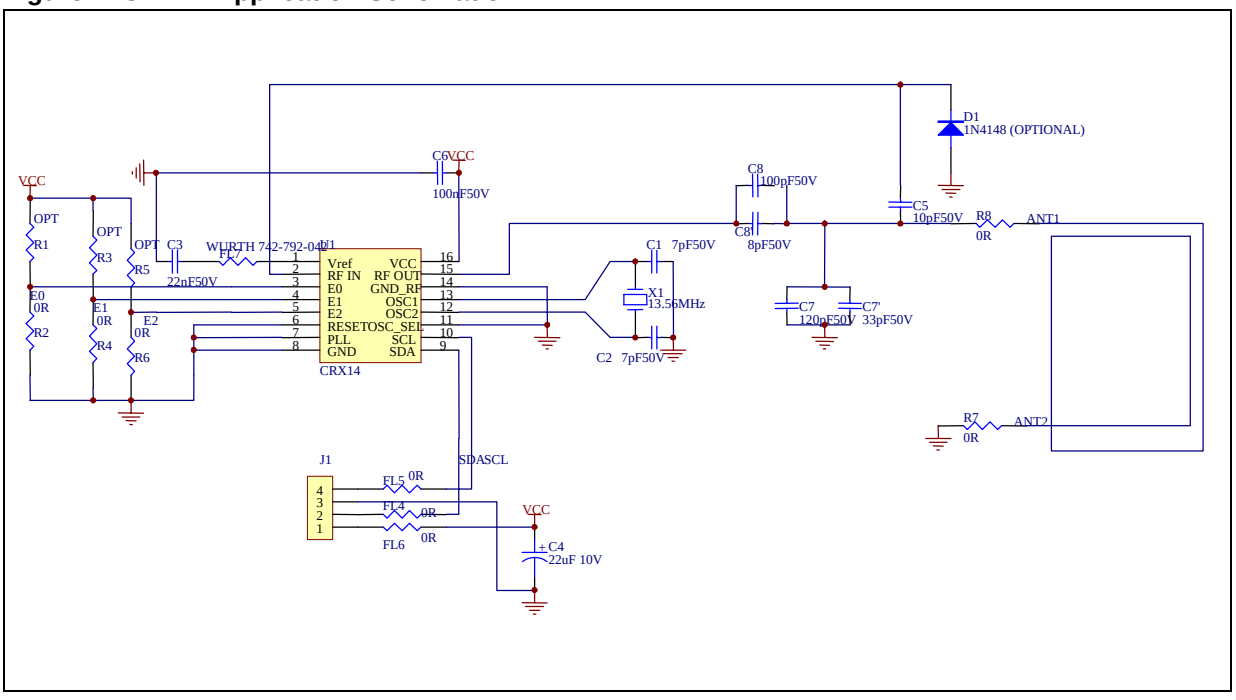
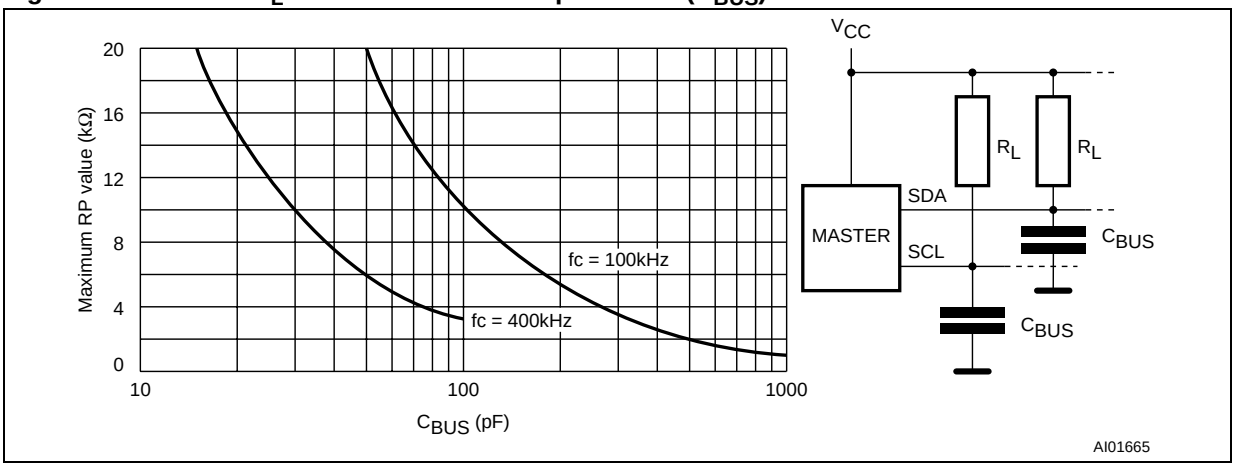


**Figure 5. Maximum $R_L$ Value versus Bus Capacitance ($C_{BUS}$) for an I²C Bus**




### Serial Clock (SCL)

The SCL input pin is used to strobe all I²C data in and out of the CRX14. In applications where this line is used by slaves to synchronize the bus to a slower clock, the master must have an open drain output, and a pull-up resistor must be connected from the SCL line to VCC. (Figure 5 indicates how the value of the pull-up resistor can be calculated).

In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the master has a push-pull (rather than open drain) output.

### Serial Data (SDA)

The SDA pin is bi-directional, and is used to transfer I²C data in or out of the CRX14. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from the SDA bus to VCC. (Figure 5 indicates how the value of the pull-up resistor can be calculated).

### Chip Enable (E0, E1, E2)

These chip enable inputs are used to set the 3 Chip Enable bits (b3, b2, b1) of the 7 bit I²C Device Select Code. They are used for hard wire addressing and up to eight CRX14 devices can be addressing on the same I²C bus. These inputs may be driven dynamically or tied to VCC or GND to establish the device select code (note that the VIL and VIH levels for the inputs are CMOS compatible, not TTL compatible). When they are left open, they are internally read at the logic level 0 due to internal pull down resistor connected on each inputs.

### Power Supply (VCC, GND, GND_RF)

Power is supplied to the CRX14 using these pins. VCC is the +5V supply voltage input and GND and GND_RF are ground connections. GND and GND_RF must be connected alltogether. Power line must be correctly filtered using decoupling capacitors as shown in Figure 4.

## CRX14 DEVICE OPERATION

The CRX14 chip coupler provides 4 volatile registers that control all the digital and analog part of the device. In the I²C protocol, all data bytes are transmitted Most Significant Byte first and a byte is transmitted Most significant bit first. The CRX14 provides 2 more registers at locations 04h and 05h which must not be used in final application. Their access is restricted to STMicroelectronics.

**Table 3. CRX14 Control Registers**

| Address | | Length | Access | Purpose |
|---|---|---|---|---|
| 00h | Parameters register | 1 byte | W | Set parameter register |
| | | | R | Read parameter register |
| 01h | Input/Output frame register | 36 bytes | W | Store and send request frame to the PICC. Wait for PICC answer frame |
| | | | R | Transfer PICC answered frame data to Host |
| 02h | Authenticate register | NA | W | Start the Authenticate process |
| | | | R | Get the Authenticate status |
| 03h | Slot Marker register | 1 byte | W | Launch the automated anti-collision process from Slot_0 to Slot_15 |
| | | | R | Return data FFh. |
| 04h | ST Reserved | NA | R & W | ST Reserved. Must not be used |
| 05h | ST Reserved | NA | R & W | ST Reserved. Must not be used |

### – Parameter Register (00h)

The parameter register is used to configure the CRX14. It allows to customize the circuit behaviour. The parameter register is located at the I²C address 00h and it is accessible in I²C read & write. It is a 8 bits volatile register. Its default setting value 00h set the CRX14 in standard ISO14443 type-B configuration.

**Table 4. Parameter Register Bits Description**

| Bit | Control | | Description |
|---|---|---|---|
| $b_0$ | Frame Standard | 0 | ISO14443 type-B frame management |
| | | 1 | RFU* |
| $b_1$ | RFU | 0 | Not used |
| $b_2$ | Answer Frame Format | 0 | Answer PICC Frames are delimited by SOF and EOF |
| | | 1 | Answer PICC Frames do not provide SOF and EOF delimiters |
| $b_3$ | ASK Modulation Depth | 0 | 10% ASK modulation depth mode |
| | | 1 | RFU* |
| $b_4$ | Carrier Frequency | 0 | 13.56MHz carrier on RF OUT is OFF |
| | | 1 | 13.56MHz carrier on RF OUT is ON |
| $b_5$ | $t_{WDG}$ Answer delay watchdog | | - b5=0, b6=0 : Watchdog time-out = 500µs to be used for read<br>- b5=0, b6=1 : Watchdog time-out = 5ms to be used for authenticate<br>- b5=1, b6=0 : Watchdog time-out = 10ms to be used for write<br>- b5=1, b6=1 : Watchdog time-out = 309ms to be used for MCU timings |
| $b_6$ | | | |
| $b_7$ | RFU | 0 | Not used |
| *RFU: Reserved For Future Used | | | |

**– Input/Output Frame Register (01h)**

The Input/Output frame register is the buffer in which the CRX14 stores the data bytes of the request frame to be sent to the PICC. It stores automatically data bytes of the answer frame received from the PICC. It is a 36 bytes buffer that is accessed serially from byte 0 up to byte 35 (see Table 5). It is located at the I²C address 01h. The first byte (byte 0) of the Input/Output Frame Register is used to store the frame length for both transmission and reception.

When accessed in I²C write, it stores the request frame bytes which will be transmitted to the PICC. Byte 0 must be set with the request frame length (in byte) and the frame is stored from byte 1. At the end of the transmission, the 16 bits CRC is automatically added. After the transmission, the CRX14 wait for the PICC to send back an answer frame. When correctly decoded, the PICC answer frame bytes are stored in the register from byte 1. Byte 0 then stores the number of bytes received from the PICC. When accessed in I²C read, it send back the last PICC answer frame bytes, if any, with byte 0 transmitted first. The 16 bits CRC is not stored and not send back on I²C bus.

The Input/Output Frame Register is set to all 00h between transmission and reception. If there is no answer from the PICC, byte 0 is set to 00h. In case of CRC error, byte 0 is set to FFh, data are discarded and not appended in the register.

**Table 5. Input/Output Frame Register Description**

| Byte 0 | Byte 1 | Byte 2 | Byte 3 | ... | Byte 34 | Byte 35 |
|---|---|---|---|---|---|---|
| **Frame Length** | **First data byte** | **Second data byte** | | | | **Last data byte** |
| | <---------- Request and Answer Frame bytes exchanged through the RF ----------> | | | | | |

| | |
|---|---|
| 00h | No byte transmitted |
| FFh | CRC Error |
| xxh | Number of transmitted bytes |

With the Input/Output Frame Register concept, it is possible to generate all the ST short range memory command frames. It is also possible to generate all standardised ISO14443 type-B command frame like REQB, SLOT-MARKER, ATTRIB, HALT and get all the answers like ATQB or answer to ATTRIB. All ISO14443 type-B compliant PICC can be accessed by the CRX14 if their data frame exchange is not longer than 35 bytes in both request and answer.

**– Authenticate Register (02h)**

The Authenticate register is used to trigger the complete authentication exchange between the CRX14 and the secured ST short range memory. It is located at the I²C address 02h.

The Authenticate system is based on a proprietary challenge/response mechanism which allows the application software to authenticate a secured ST short range memory from the SRX--- family. A reader designed with the CRX14 can check the authenticity of a memory device and protect the application system against silicon copy or emulator.

Complete description of the Authenticate system is available under Non Disclosure Agreement (NDA) with STMicroelectronics. To get more details about this CRX14 function, please contact the nearest STMicroelectronics sales office.

**– Slot Marker Register (03h)**

The slot marker register is used to trigger an automated anti-collision sequence between the CRX14 and ST short range memory available in the electromagnetic field. With one I²C access, the CRX14 launch a complete stream of commands starting with the PCALL16(), SLOT_MARKER(1), SLOT_MARKER(2) up to SLOT_MARKER(15) and stores all the identified Chip_ID in the Input/Output Frame Register (I²C address 01h). This automated anti-collision sequence simplify the host software development and reduce the time needed to interrogate the 16 slots of the STMicroelectronics anti-collision mechanism. It is located at the I²C address 03h.

When accessed in I²C write, it starts generating the anti-collision commands in sequence. After each command, the CRX14 wait for the ST short range memory answer frame which contain the Chip_ID. The validity of the answer is checked and stored in corresponding status slot bit (Byte 1 and Byte 2 as described in Table 6). If the answer is OK, the status slot bit is set to 1 and the Chip_ID is stored in the corresponding Slot_Register. If no answer or a CRC error is detected, the status slot bit is set to 0 and the corresponding Slot_Register is set to 00h for “NO ANSWER” or to FFh for “CRC ERROR”. Each time the Slot Marker Register is accessed in I²C write, byte 0 of the Input/Output Frame Register is set to 18, byte 1 & 2 provides status bits slot information and byte 3 to byte 18 stores Chip_ID or error code.

Access in I²C read is not possible. To get all these anti-collision data, it is needed to read the Input/Output Frame Register at the I²C address 01h.

**Table 6. Slot Marker Register Description**

| | $b_7$ | $b_6$ | $b_5$ | $b_4$ | $b_3$ | $b_2$ | $b_1$ | $b_0$ |
|---|---|---|---|---|---|---|---|---|
| Byte 0 | Number of stored bytes: fixed to 18 | | | | | | | |
| Byte 1 | status Slot bit 7 | status Slot bit 6 | status Slot bit 5 | status Slot bit 4 | status Slot bit 3 | status Slot bit 2 | status Slot bit 1 | status Slot bit 0 |
| Byte 2 | status Slot bit 15 | status Slot bit 14 | status Slot bit 13 | status Slot bit 12 | status Slot bit 11 | status Slot bit 10 | status Slot bit 9 | status Slot bit 8 |
| Byte 3 | Slot_Register 0 = Chip_ID value detected in Slot 0 | | | | | | | |
| Byte 4 | Slot_Register 1 = Chip_ID value detected in Slot 1 | | | | | | | |
| Byte 5 | Slot_Register 2 = Chip_ID value detected in Slot 2 | | | | | | | |
| Byte 6 | Slot_Register 3 = Chip_ID value detected in Slot 3 | | | | | | | |
| Byte n | ..... | | | | | | | |
| Byte 17 | Slot_Register 14 = Chip_ID value detected in Slot 14 | | | | | | | |
| Byte 18 | Slot_Register 15 = Chip_ID value detected in Slot 15 | | | | | | | |

Status bit value description:
- 1: No error detected. The Chip_ID stored in the Slot register is valid.
- 0: Error detected
  - Slot register = 00h: No answer frame detected from ST short range memory
  - Slot register = FFh: Answer Frame detected with CRC error. Collision may occur

## CRX14 I²C PROTOCOL DESCRIPTION

The CRX14 is compatible with the I²C serial bus memory standard. This is a two wire serial interface that uses a bi-directional data bus and serial clock. The CRX14 carries a built-in 4 bit device identification codes: '1010' (as shown in Table 7) which corresponds to the I²C bus definition. This is used together with 3 chip enable inputs (E2, E1, E0) so that up to eight CRX14 devices may be attached to the I²C bus and selected individually.

The CRX14 behaves as a slave device in the I²C protocol, with all CRX14 operations synchronized by the serial clock. I²C Read and write operations are initiated by a START condition, generated by the bus master. The START condition is followed by the Device Select Code which is composed of a stream of 7 bits (1010xxx as shown in Table 7), plus one read/write bit ($R/\overline{W}$) and is terminated by an acknowledge bit.

When writing data to the CRX14, it inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a STOP condition after an Ack for WRITE, and after a NoACK for READ.

**Table 7. Device Select Code**

| | Device Code | | | | Chip Enable | | | $R\overline{W}$ |
|---|---|---|---|---|---|---|---|---|
| | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| CRX14 Select | 1 | 0 | 1 | 0 | E2 | E1 | E0 | $R\overline{W}$ |

The CRX14 supports the I²C protocol, as summarized in Figure 6. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the master, and the other as the slave. A data transfer can only be initiated by the master, which will also provide the serial clock for synchronization. The CRX14 is always a slave device in all I²C communication. All data are transmitted Most Significant Bit first (MSB).

### I²C Start Condition

START is identified by a high to low transition of the SDA line while the clock, SCL, is stable in the high state. A START condition must precede any data transfer command. The CRX14 continuously monitors (except during a radio frequency data exchange) the SDA and SCL lines for a START condition, and will not respond unless one is given.

### I²C Stop Condition

STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the CRX14 and the bus master. A STOP condition at the end of an I²C Read command, after (and only after) a NoACK, forces the CRX14 into its stand-by state. A STOP condition at the end of an I²C Write command triggers the radio frequency data exchange between the CRX14 and the PICC.

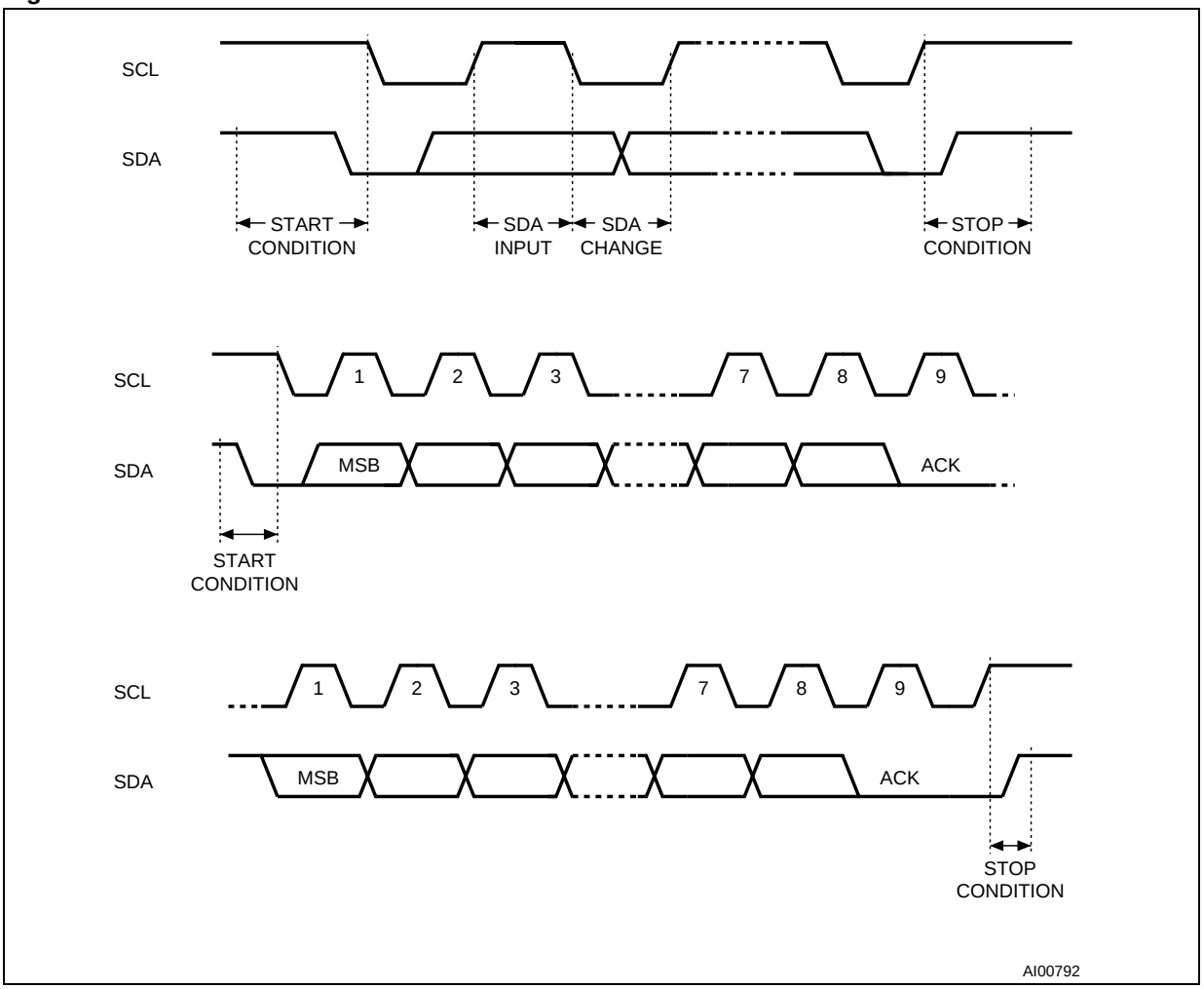
### I²C Acknowledge Bit (ACK)

An acknowledge signal is used to indicate a successful data transfer on the I²C bus. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the $9^{th}$ clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 data bits.

### I²C Data Input

During data input, the CRX14 samples the SDA bus signal on the rising edge of the clock, SCL. For correct device operation, the SDA signal must be stable during the clock low-to-high transition, and the data must change *only* when the SCL line is low.

**Figure 6. I²C Bus Protocol**



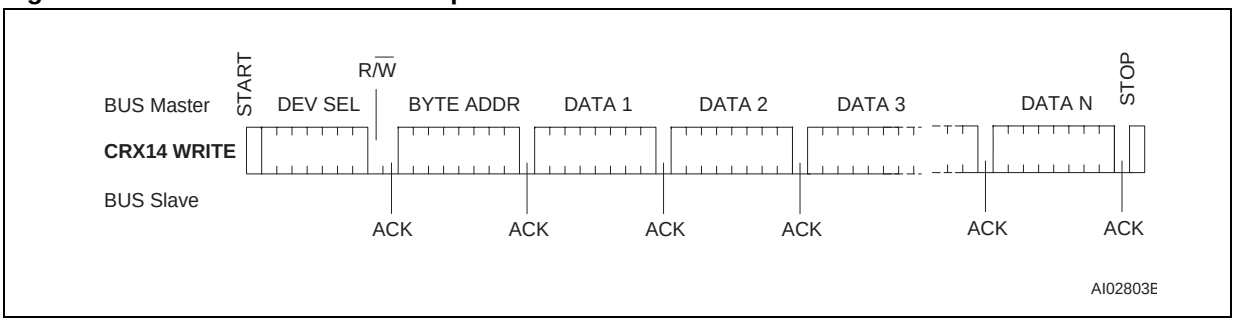

### I²C Memory Addressing

To start communication between the bus master and the CRX14, the master must initiate a START condition. Following this, the master sends 8 bits to the SDA bus line (with the most significant bit first). These bits represent the Device Select Code (7 bits) and a $\overline{RW}$ bit. The seven most significant bits of the Device Select Code are the Device Type Identifier, according to the I²C bus definition. For the CRX14, the seven bits are fixed as shown in Table 7. The $8^{th}$ bit is the read or write bit ($\overline{RW}$). This bit is set to '1' for I²C read and '0' for I²C write operations. If a match occurs on the Device Select Code, the corresponding CRX14 gives an acknowledgment on the SDA bus during the $9^{th}$ bit time. If the CRX14 does not match the Device Select code, a No-ACK is generated. The CRX14 deselect itself from the bus and go into stand-by mode.

### CRX14 I²C Write Operations

Following a START condition, the master sends a Device Select code with the $\overline{RW}$ bit set to '0'. The CRX14 acknowledges it and waits for a byte address, which provides access to the register area. After receipt of the address, the CRX14 again responds with an acknowledge and waits for the data bytes. In the CRX14 I²C Write mode, the master may sends one or more data bytes depending on the selected register. The CRX14 replies with an ACK after each data byte. The master terminates the transfer by generating a STOP condition. The STOP condition launch the radio frequency data exchange between the CRX14 and the PICC when the Input/output register, authenticate or anti-collision are accessed in write.

**Figure 7. CRX14 I²C Write Mode Sequence**




During the radio frequency data exchange, the CRX14 disconnects itself from the I²C bus. The time ($t_{RFEX}$) needed to complete the exchange is not fixed as it depends on the PICC command format. To make use of this, an ACK polling sequence can be used by the master.

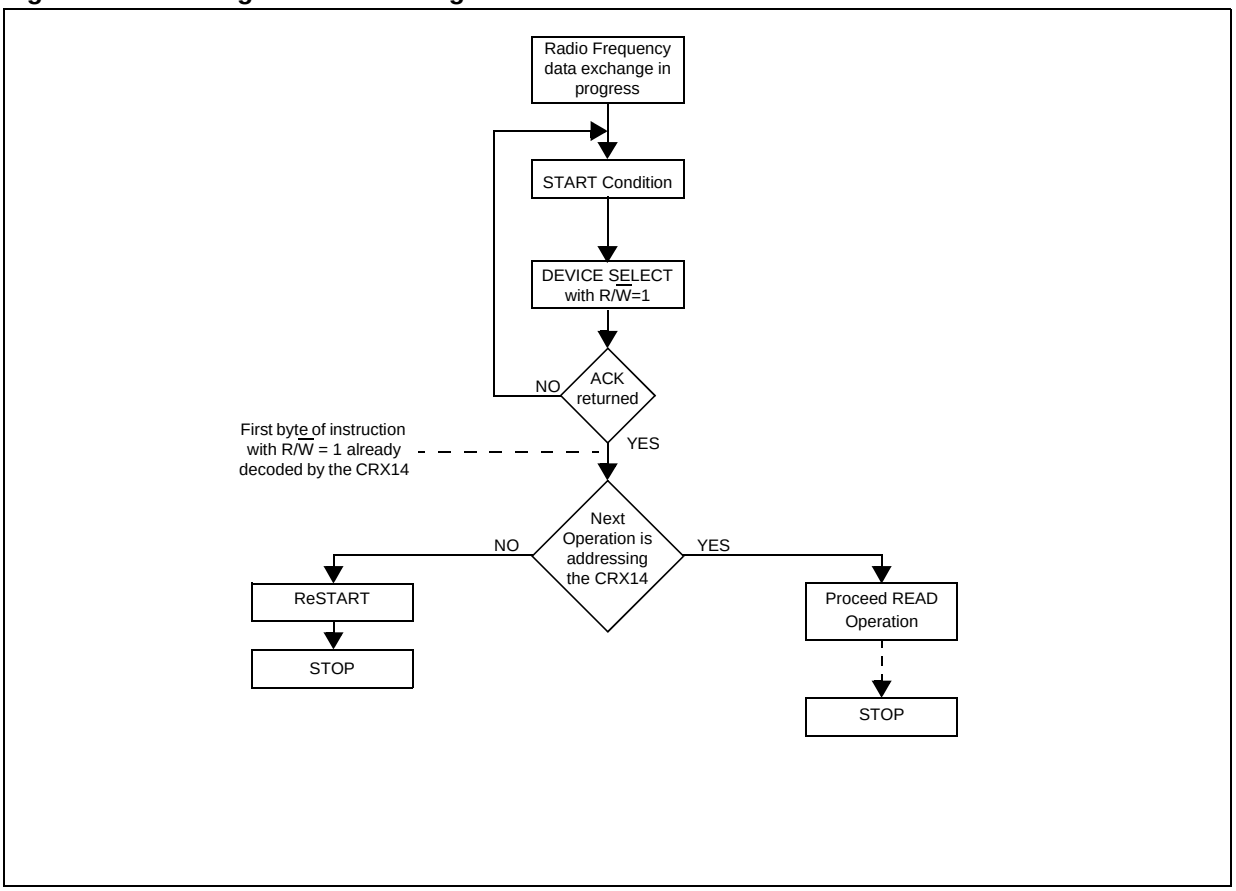
The sequence, as shown in Figure 8, is as follows:

– Initial condition: a radio frequency data exchange is in progress.

– Step 1: the master issues a START condition followed by a device select byte (first byte of the new instruction).

– Step 2: if the CRX14 is busy, no ACK will be returned and the master goes back to Step 1. If the CRX14 has completed the radio frequency data exchange, it responds with an ACK, indicating that it is ready to receive the second part of the next instruction (the first byte of this instruction having been sent during Step 1).

**Figure 8. I²C Polling Flowchart using ACK**



### CRX14 I²C Read Operations

Following a START condition, the master sends a Device Select code with the R/$\overline{W}$ bit set to '1'. The CRX14 acknowledges it and outputs the first data byte of the addressed register. In order to select a specific register, a dummy write must be performed up to the address byte, as shown in Figure 9. This dummy command stores the register address into the internal address pointer. The read select automatically the register pointed by the internal address pointer. In the I²C Read mode, the CRX14 may get one or more data bytes depending on the selected register. The master must generate an acknowledge after each data byte in order to continuously read all the data of the register. The master must *not* acknowledge the last data byte output, and terminates the transfer with a STOP condition, as shown in Figure 9.

In the I²C read mode, the CRX14 waits for an acknowledgment during the 9$^{th}$ bit time. If the master does not pull the SDA line low during this time, the CRX14 terminates the data transfer and switches to its standby state.

**Figure 9. CRX14 I²C Read Modes Sequences**

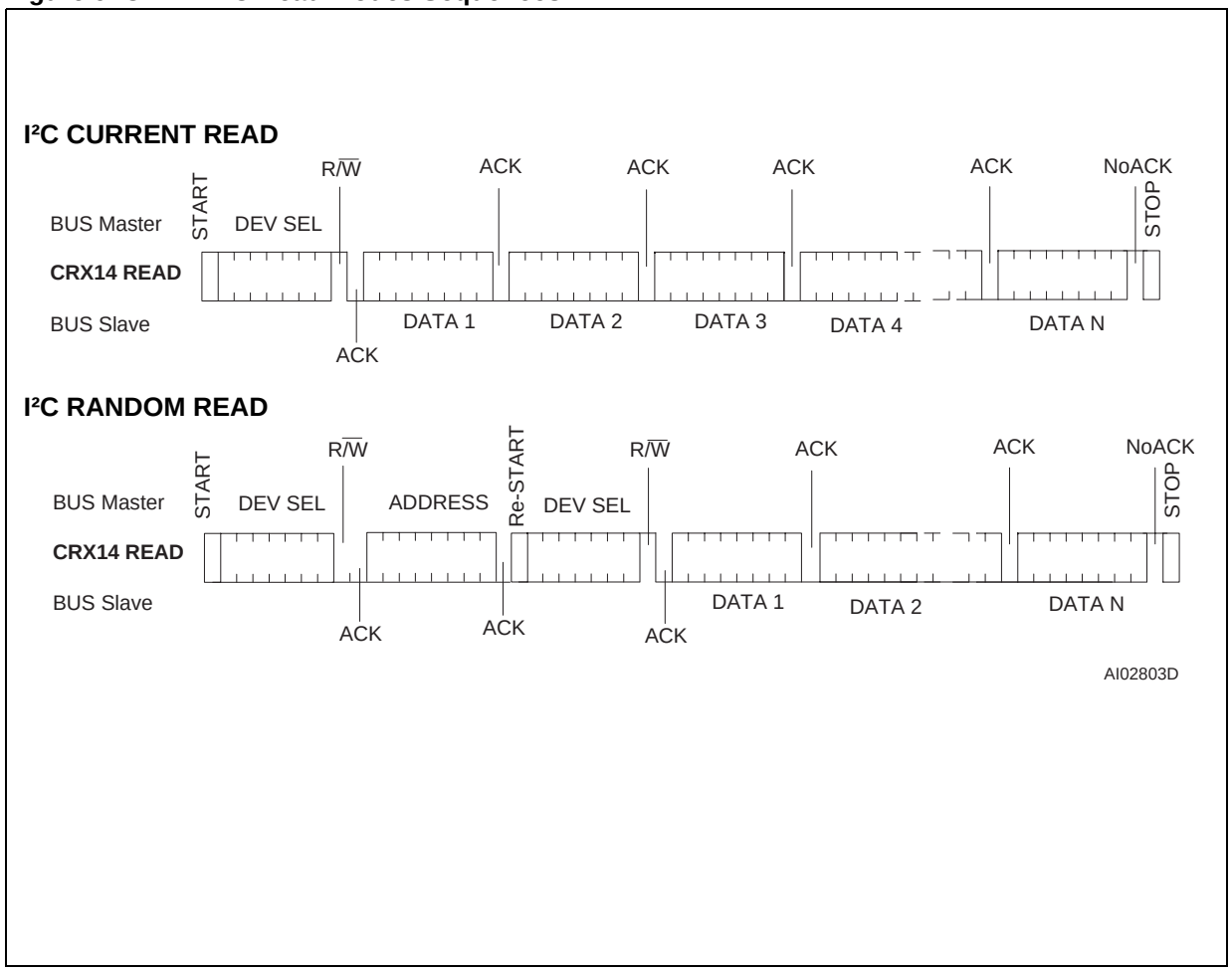


**Table 8. I²C AC Characteristics ($T_A$ = -20 to 85 °C; VCC = 5V ± 500mV)**

| Symbol | Alt. | Parameter | Fast $I^2C$ 400 kHz | | $I^2C$ 100 kHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{CH1CH2}$ [2] | $t_R$ | Clock Rise Time | | 300 | | 1000 | ns |
| $t_{CL1CL2}$ [2] | $t_F$ | Clock Fall Time | | 300 | | 300 | ns |
| $t_{DH1DH2}$ [2] | $t_R$ | SDA Rise Time | 20 | 300 | 20 | 1000 | ns |
| $t_{DL1DL2}$ [2] | $t_F$ | SDA Fall Time | 20 | 300 | 20 | 300 | ns |
| $t_{CHDX}$ [1] | $t_{SU:STA}$ | Clock High to Input Transition | 600 | | 4700 | | ns |
| $t_{CHCL}$ | $t_{HIGH}$ | Clock Pulse Width High | 600 | | 4000 | | ns |
| $t_{DLCL}$ | $t_{HD:STA}$ | Input Low to Clock Low (START) | 600 | | 4000 | | ns |
| $t_{CLDX}$ | $t_{HD:DAT}$ | Clock Low to Input Transition | 0 | | 0 | | µs |
| $t_{CLCH}$ | $t_{LOW}$ | Clock Pulse Width Low | 1.3 | | 4.7 | | µs |
| $t_{DXCX}$ | $t_{SU:DAT}$ | Input Transition to Clock Transition | 100 | | 250 | | ns |
| $t_{CHDH}$ | $t_{SU:STO}$ | Clock High to Input High (STOP) | 600 | | 4000 | | ns |
| $t_{DHDL}$ | $t_{BUF}$ | Input High to Input Low (Bus Free) | 1.3 | | 4.7 | | µs |
| $t_{CLQV}$ | $t_{AA}$ | Clock Low to Data Out Valid | | 1000 | | 3500 | ns |
| $t_{CLQX}$ | $t_{DH}$ | Data Out Hold Time After Clock Low | 200 | | 200 | | ns |
| $f_C$ | $f_{SCL}$ | Clock Frequency | | 400 | | 100 | kHz |

Note: 1. For a reSTART condition, or following a write cycle.
2. Sampled only, not 100% tested

**Table 9. I²C DC Characteristics ($T_A$ = -20 to 85 °C; $V_{CC}$ = 5V ± 500mV)**

| Symbol | Parameter | Test Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current (SCL, SDA, E0, E1, E2) | $0 V \le V_{IN} \le V_{CC}$ | | ± 2 | µA |
| $I_{LO}$ | Output Leakage Current (SCL, SDA, E0, E1, E2) | $0 V \le V_{OUT} \le V_{CC,}$ SDA in Hi-Z | | ± 2 | µA |
| $I_{CC}$ | Supply Current | $V_{CC}$=5V, $f_c$=400kHz (rise/fall time < 30ns), RF OFF | | 6 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$=5V, $f_c$=400kHz (rise/fall time < 30ns), RF ON | | 20 | mA |
| $I_{CC1}$ | Supply Current (Stand-by) | $V_{IN} = V_{SS}$ or $V_{CC}$ , $V_{CC}$ = 5 V, RF OFF | | 5 | mA |
| $V_{IL}$ | Input Low Voltage (SCL, SDA) | | - 0.3 | 0.3 $V_{CC}$ | V |
| $V_{IH}$ | Input High Voltage (SCL, SDA) | | 0.7 $V_{CC}$ | $V_{CC}$ + 1 | V |
| $V_{IL}$ | Input Low Voltage (E0, E1, E2) | | - 0.3 | 0.3 $V_{CC}$ | V |
| $V_{IH}$ | Input High Voltage (E0, E1, E2) | | 0.7 $V_{CC}$ | $V_{CC}$ + 1 | V |
| $V_{OL}$ | Output Low Voltage (SDA) | $I_{OL}$ = 3 mA, $V_{CC}$ = 5 V | | 0.4 | V |

**Figure 10. I²C AC Waveforms**

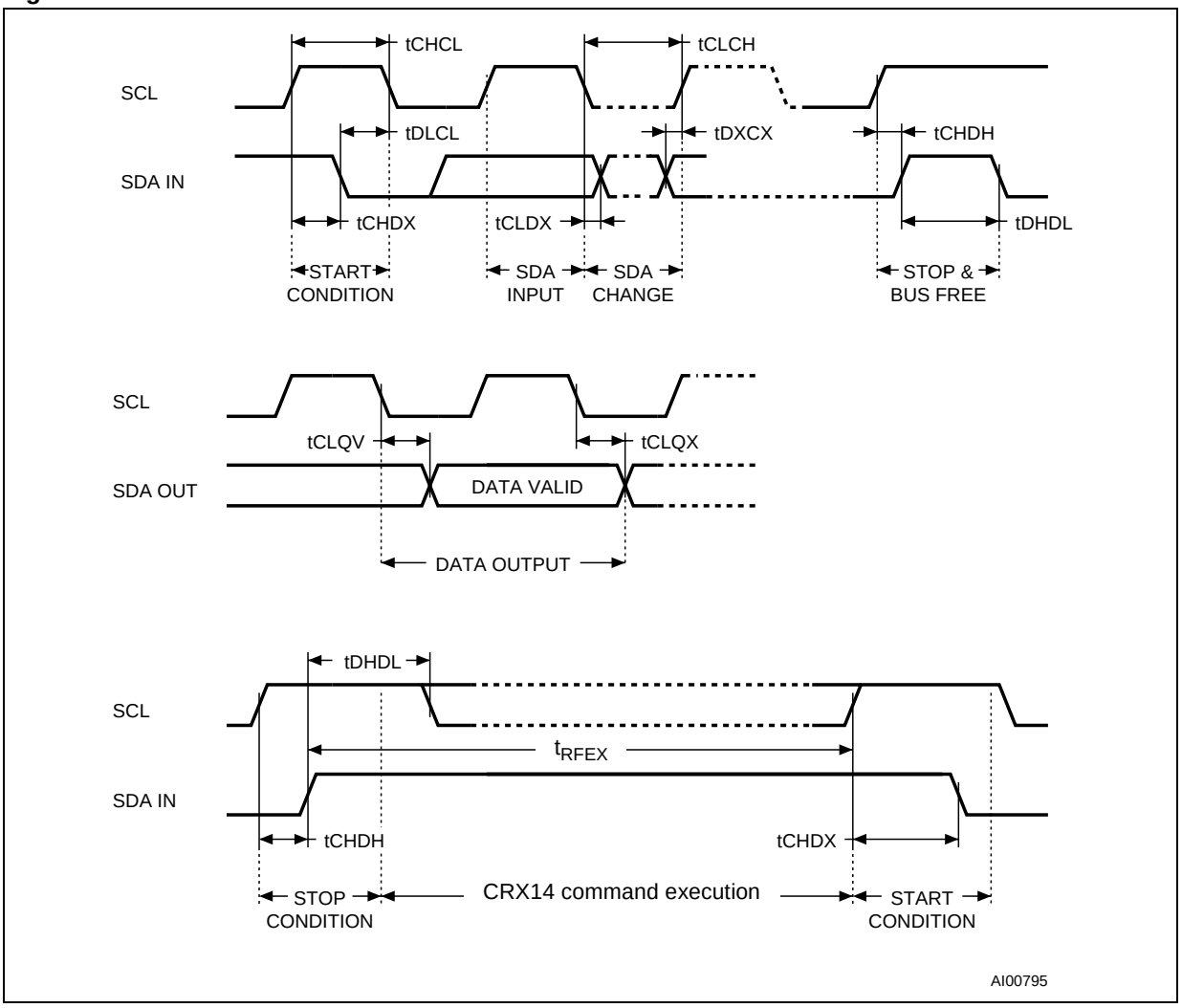



**Table 10. I²C AC Measurement Conditions**

| | |
|---|---|
| Input Rise and Fall Times | ≤ 50 ns |
| Input Pulse Voltages | $0.2V_{CC}$ to $0.8V_{CC}$ |
| Input and Output Timing Reference Voltages | $0.3V_{CC}$ to $0.7V_{CC}$ |

**Figure 11. I²C AC Testing Input Output Waveform**

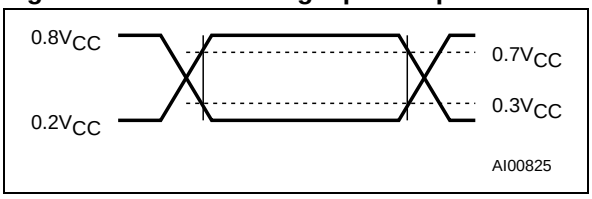



**Table 11. I²C Input Parameters[1] ($T_A$ = 25 °C, f = 400 kHz)**

| Symbol | Parameter | Test Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance (SDA) | | | 8 | pF |
| $C_{IN}$ | Input Capacitance (SCL, E0, E1, E2)) | | | 6 | pF |
| $t_{NS}$ | Low Pass Filter Input Time Constant (SCL & SDA Inputs) | | 100 | 400 | ns |

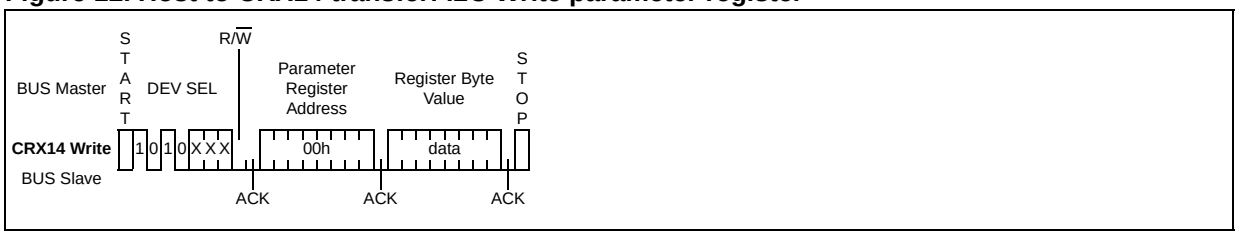
Note: 1. Sampled only, not 100% tested.

## I²C PROTOCOL DESCRIPTION TO THE CRX14 REGISTERS

### – I²C Parameter register protocol

Write a new data value in the parameter register. The new setting is active after the I²C STOP condition.

**Figure 12. Host to CRX14 transfer: I2C Write parameter register**




Get the parameter register content. Until NoACK generated by the I²C Host, the CRX14 re-sent the parameter register content. The CRX14 support the I²C current and random address read modes. The current address read mode can be used if the previous command was an access to the same register.

**Figure 13. CRX14 to Host transfer: I2C Random Read parameter register**

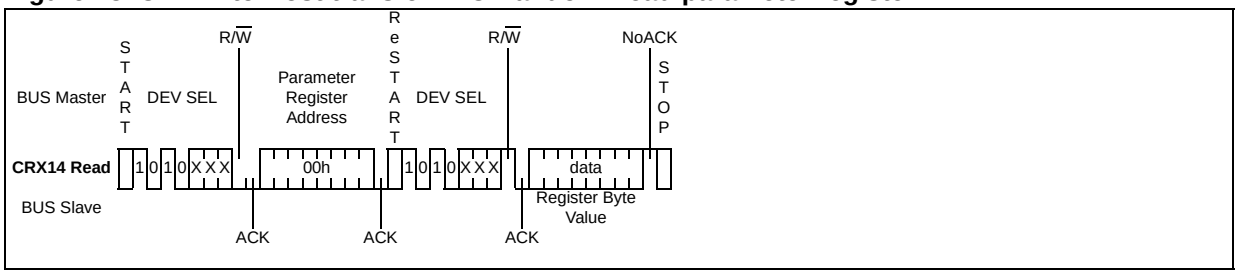
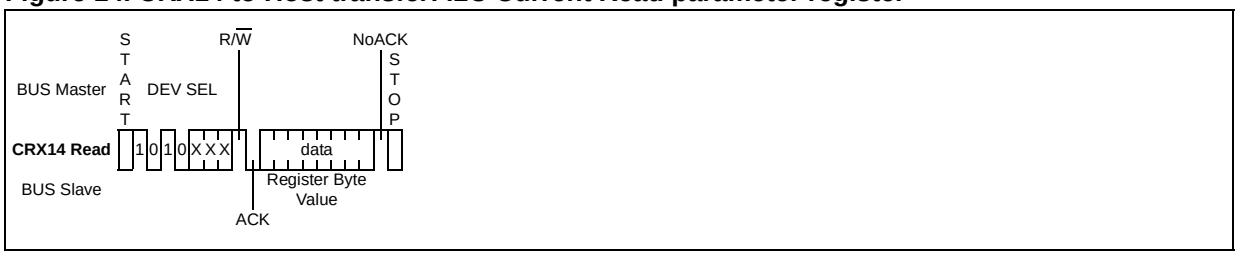


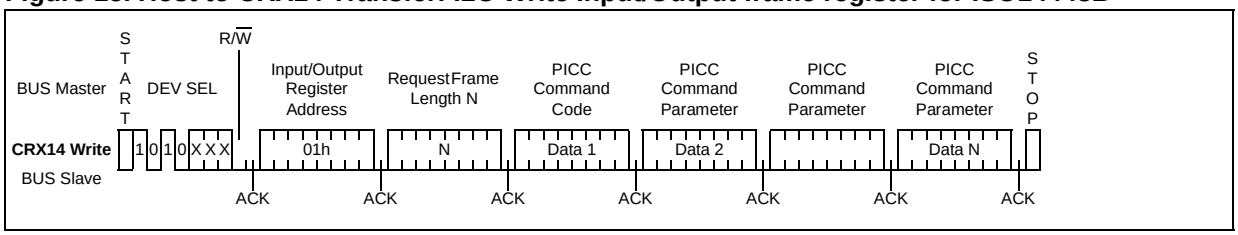

**Figure 14. CRX14 to Host transfer: I2C Current Read parameter register**



**– I²C Input/Output frame register protocol**

Store a PICC request frame command of N bytes in the input/output frame register. After the I²C STOP condition, the request frame is send on the RF in the ISO14443 type-B format. The CRX14 wait for the PICC answer frame which is stored in the same input/output frame register. The request frame is over-written by the answer frame.

**Figure 15. Host to CRX14 Transfer: I2C Write Input/Output frame register for ISO14443B**




Get the PICC answer frame of N bytes if any. The 2 CRC bytes generated by the PICC are not stored. Until NoACK is generated by the I²C Host, the CRX14 roll over into the Input/Output register content. The CRX14 support the I²C current and random address read modes. The current address read mode can be used if the previous command was an access to the same register.

**Figure 16. CRX14 to Host transfer: I2C Random Read Input/Output frame register for ISO14443B**

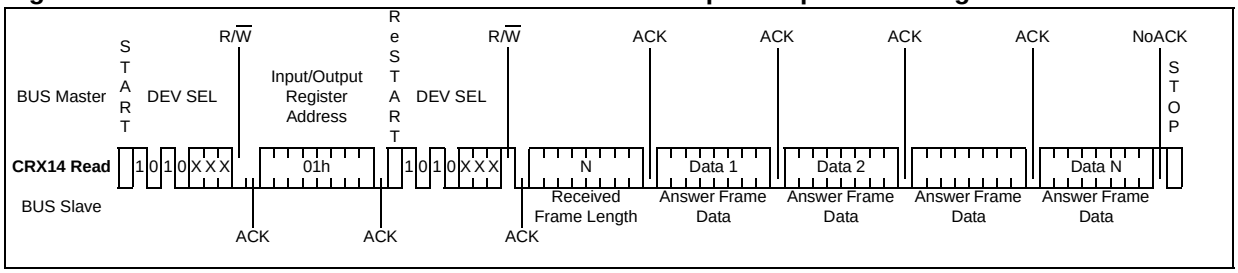
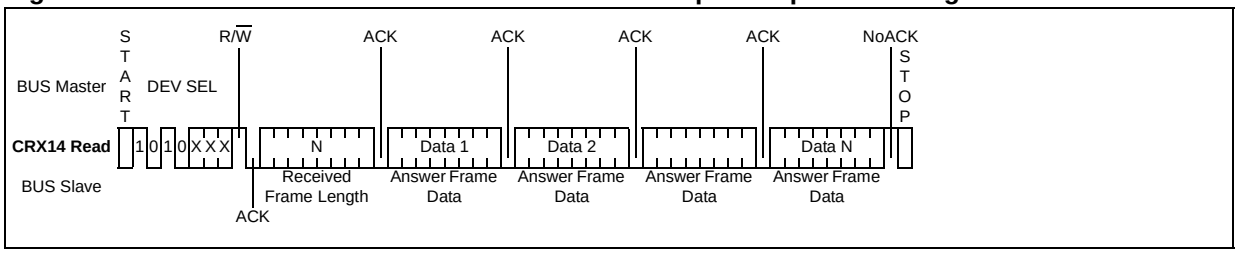



**Figure 17. CRX14 to Host transfer: I2C Current Read Input/Output frame register for ISO14443B**



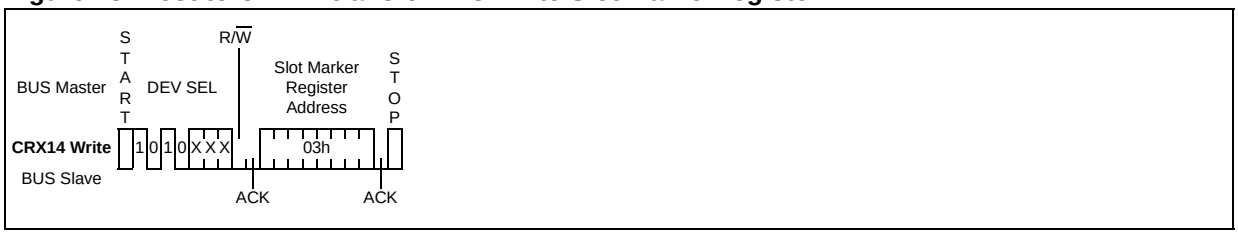

**– I²C Authenticate register protocol**

Please contact the nearest STMicroelectronics sales office.

### – I²C Slot Marker register protocol

An I²C write in the Slot Marker register generates an automated 16 loops command sequence. Each answers detected from ST short range memory are written in the Input/Output register.

**Figure 18. Host to CRX14 transfer: I2C Write Slot Marker register**




Read the I²C Slot Marker Register is not supported by the CRX14. The result of the detection sequence is stored in the Input/output register. The host has to read this frame register at the I2C address 01h using an I2C random read. When reading the Slot Marker Register, until NoACK is generated by the I²C Host, the CRX14 send back the data value FFh in both random and current read modes.

**Figure 19. CRX14 to Host transfer: I2C Random Read Slot Marker register**

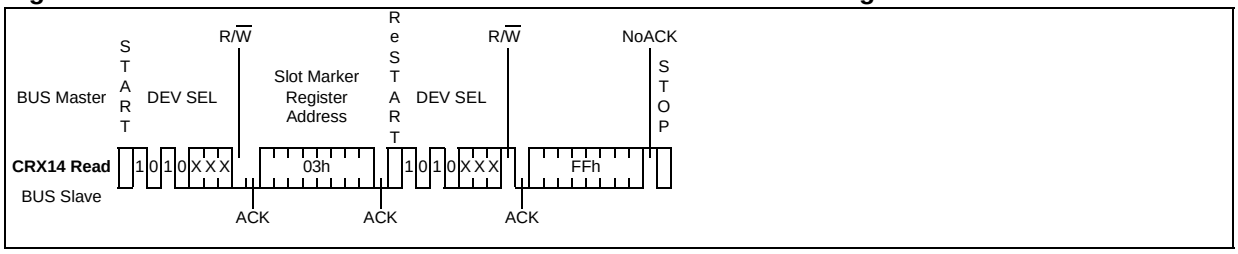
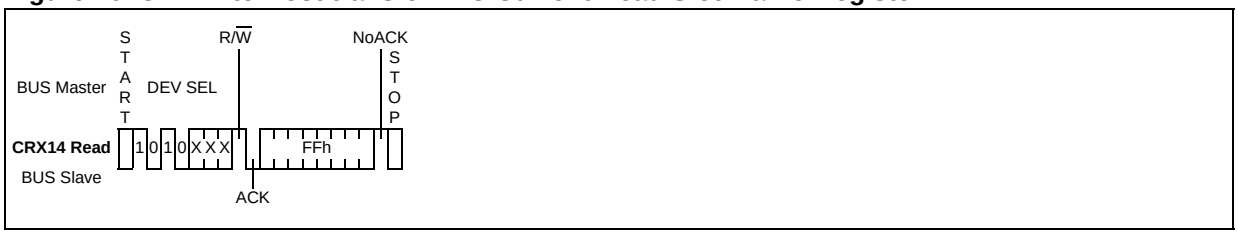



**Figure 20. CRX14 to Host transfer: I2C Current Read Slot Marker register**




### – Addresses above location 06h

For I2C Write commands, after the reception of the 8 bits of the register address, the CRX14 does not acknowledge (NoACK) it and deselect itself from the bus. The SDA line stays at logic 1 (pull-up resistor) and the I2C host receives a NoACK during the 9th bit. The SDA line stays high up to the STOP condition. For I2C current read, the CRX14 does not acknowledge the device select code after the START condition and it deselect itself from the bus.

## CRX14 ISO14443 TYPE-B RADIO FREQUENCY DATA TRANSFER

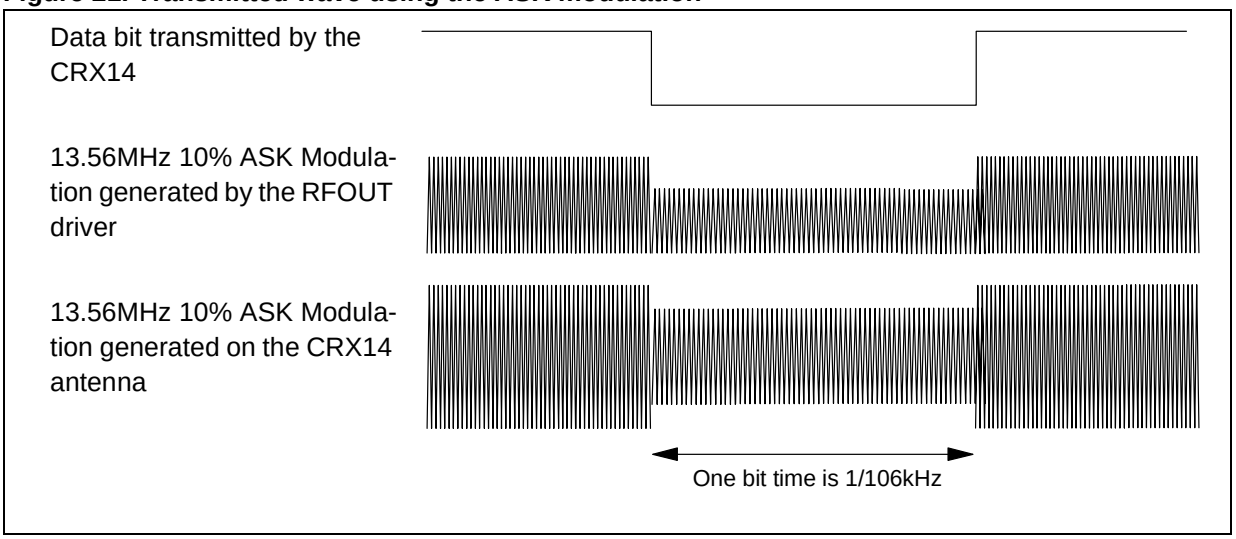
### Output RF data transfer from the CRX14 to the PICC (Request Frame)

The CRX14 output buffer is controlled by the 13.56MHz clock signal generated by the external oscillator and by the request frame generator. It can be directly connected to an external antenna circuit to generate

The current driven into the coil and its tuning impedance circuitry is directly . The CRX14 generates a 13.56MHz sinusoidal carrier frequency on its antenna.

If the antenna is correctly accorded, it emits a H-field with enough energy to power a contactless PICC at a short distance. The energy received on the PICC antenna is transformed to a Power Supply Voltage through a regulator and to data bits through the ASK demodulator. The CRX14 uses a 10% amplitude modulation mode of the 13.56MHz wave as shown in Figure 21. The data transfer rate is 106 Kbit/s.

**Figure 21. Transmitted wave using the ASK modulation**




### Character transmission format for Request Frame

The CRX14 transmit characters of 10 bits as detailed in Table 12 with the LSB ($b_0$) transmitted first. These characters, with the addition of the Start Of Frame (SOF) and the End Of Frame (EOF), are grouped to form a Request Frame as shown in Figure 23. The frame includes SOF, instructions, addresses, data, CRC and EOF as defined in the ISO14443 type-B.

Each bit duration is called ETU (Elementary Time Unit). One ETU is equal to 9.44µs (1/106Khz).

**Table 12. CRX14 Request Frame character format**

| | $b_0$ | $b_1$ | $b_2$ | $b_3$ | $b_4$ | $b_5$ | $b_6$ | $b_7$ | $b_8$ | $b_9$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 ETU | Start "0" | LSB | | | Information Byte | | | | MSB | Stop "1" |

| Bit | Description | Value |
|---|---|---|
| $b_0$ | start bit used to synchronize the transmission | $b_0 = 0$ |
| $b_1$ to $b_8$ | Information byte (instruction, address or data) | Information byte is sent LSB first |
| $b_9$ | Stop bit used to indicate the end of the character | $b_9 = 1$ |

### Request Start Of Frame

The SOF described in Table 13 is composed by:

– one falling edge,
– followed by 10 etu with a logical 0,
– followed by one single rising edge
– followed by 2 etu with a logical 1.

**Table 13. Request Start Of Frame**

| | $b_0$ | $b_1$ | $b_2$ | $b_3$ | $b_4$ | $b_5$ | $b_6$ | $b_7$ | $b_8$ | $b_9$ | $b_{10}$ | $b_{11}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ETU | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

### Request End Of Frame

The EOF shown in Table 14 is composed by:

– one falling edge,
– followed by 10 etu with a logical 0,
– followed by one single rising edge

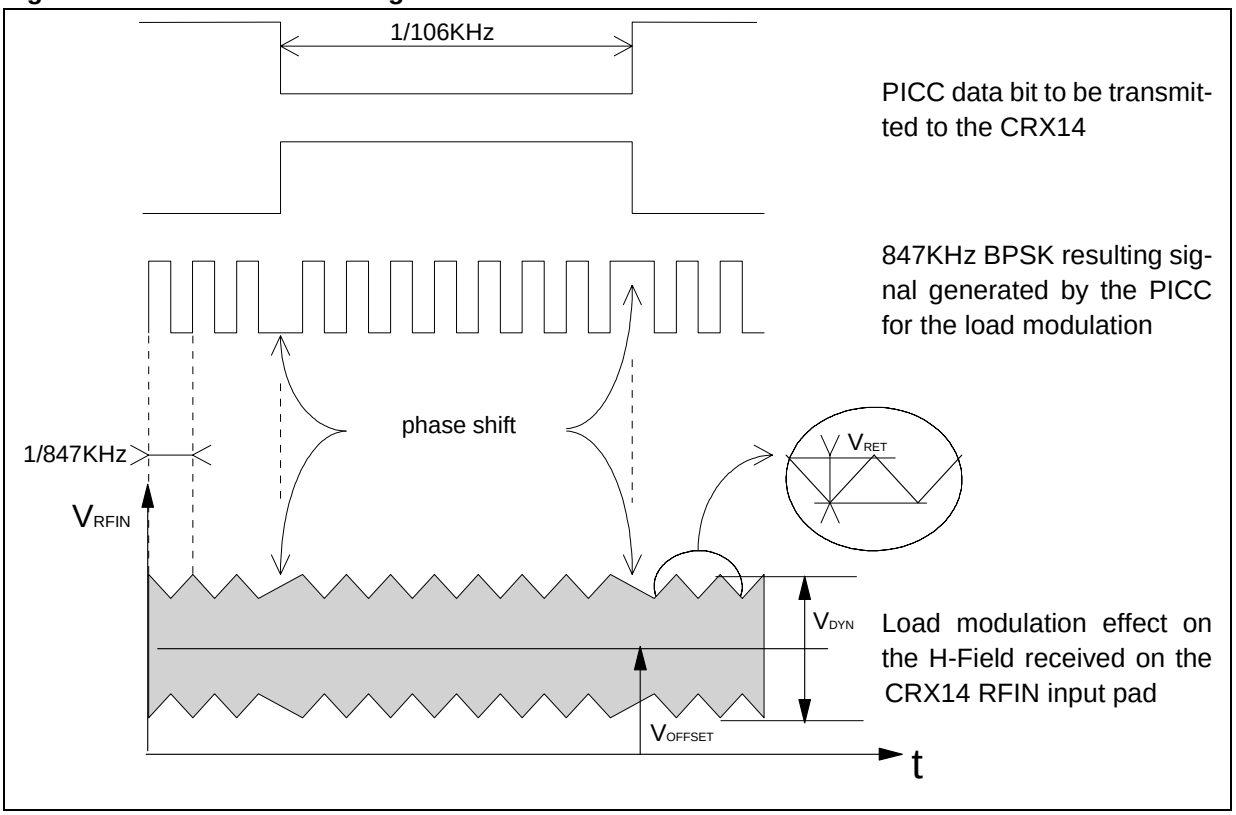
**Table 14. Request End Of Frame**

| | $b_0$ | $b_1$ | $b_2$ | $b_3$ | $b_4$ | $b_5$ | $b_6$ | $b_7$ | $b_8$ | $b_9$ |
|---|---|---|---|---|---|---|---|---|---|---|
| ETU | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### Input RF data transfer from the PICC to the CRX14 (Answer Frame)

The CRX14 used the ISO14443 type-B retro-modulation scheme which is demodulated and decoded by the RFIN circuitry. This modulation is obtained by modifying the PICC current consumption (load modulation). The load modulation, using the coupling phenomenon, induces a variation on the H-field that is detected by the CRX14 RFIN input as a voltage variation on the antenna. The RFIN input demodulates these variations and decodes the received information from the PICC. Data must be transmitted using the BPSK coding format of a 847kHz sub-carrier frequency $f_S$ as shown in Figure 22 and as specify in ISO14443 type-B. With the BPSK coding method, all data state transition (from 0 to 1 or 1 to 0) are coded by a sub-carrier phase shift.

**Figure 22. Received wave using the BPSK sub-carrier modulation**




### Character transmission format for Answer Frame

The character format of the PICC must be the same as for the output data transfer (Table 12). The answer frame includes SOF, data, CRC and EOF (Figure 23). The data transfer rate is 106 kbit/s. The CRX14 support also answer frame without SOF and EOF delimiters if it is correctly settled in the parameter register (Figure 23).

### Answer Start Of Frame

The PICC SOF must be compliant with the ISO14443 type-B , as described in Table 15.

– 10 or 11 etu with a logical 0,

– 2 etu with a logical 1.

**Table 15. Answer Start Of Frame**

| | $b_0$ | $b_1$ | $b_2$ | $b_3$ | $b_4$ | $b_5$ | $b_6$ | $b_7$ | $b_8$ | $b_9$ | $b_{10}$ | $b_{11}$ | $b_{12}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ETU | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

### Answer End Of Frame

The PICC EOF must be compliant with the ISO14443 type-B, as described in Table 16.

– 10 or 11 etu with a logical 0,

– 2 etu with a logical 1

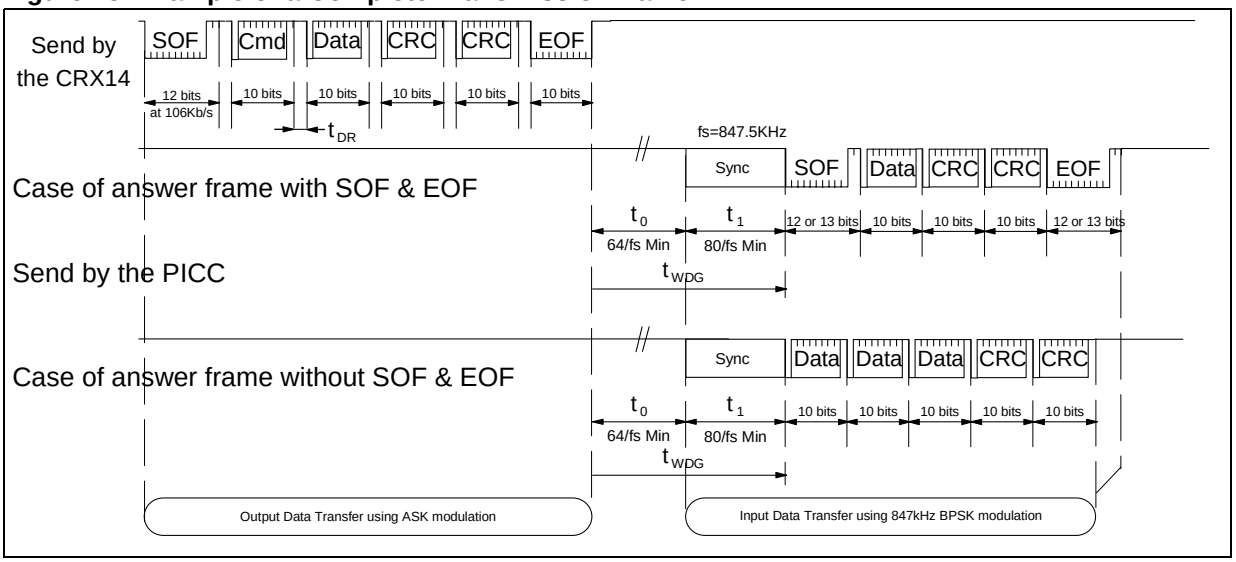
**Table 16. Answer End Of Frame**

| | $b_0$ | $b_1$ | $b_2$ | $b_3$ | $b_4$ | $b_5$ | $b_6$ | $b_7$ | $b_8$ | $b_9$ | $b_{10}$ | $b_{11}$ | $b_{12}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ETU | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

### Transmission frame

Between the Request frame and the Answer frame data transfer, there must be a guard time without ASK and BPSK modulation for a minimum delay of $t_0$ (see Table 18). This delay allows the CRX14 to switch from transmission to reception mode and must be applied after each frame. After $t_0$, the 13.56MHz carrier frequency is modulated by the PICC at 847kHz for a minimum delay of $t_1$ (see Table 18) to allow the CRX14 synchronization. After $t_1$, the first phase transition generated by the PICC represents the start bit (‘0’) of the Answer SOF (or the start bit ‘0’ of the first data character in non SOF/EOF mode).

**Figure 23. Example of a Complete Transmission frame**



### CRC

The 16 bits CRC used by the CRX14 follows the ISO14443 type B recommendation. For further information, please see the annex on page 26. The initial register content is all ones : "FFFF".

The two bytes CRC are appended to each Request and each Answer, within each frame, before the EOF. The CRC is calculated on all the bytes after the SOF up to the CRC field.

Upon transmission of a Request from the CRX14, the PICC verify that the CRC value is valid. If it is invalid, it discard the frame and does not answer to the CRX14.

Upon reception of an Answer from the PICC, the CRX14 verify that the CRC value is valid. If it is invalid, it stores the value 0xFF in the Input/Output frame register.

The CRC is transmitted Least Significant Byte first. Each byte is transmitted Least Significant Bit first.

**Table 17. CRC transmission rules**

| LSByte | | MSByte | |
|---|---|---|---|
| **LSBit** | **MSBit** | **LSBit** | **MSBit** |
| CRC 16 (8bits) | | CRC 16 (8 bits) | |

**Table 18. RFOUT AC Characteristics ($T_A$ = -20 to 85 °C; $V_{CC}$ = 5V ± 500mV)**

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{CC}$ | External Oscillator Frequency | Vcc=5V | 13.553 | 13.567 | MHz |
| $MI_{CARRIER}$ | Carrier Modulation Index | MI=(A-B)/(A+B) | 10 | 14 | % |
| $t_{RFR}$, $t_{RFF}$ | 10% Rise and Fall time | | 0.5 | 1.5 | µs |
| $t_{RFSBL}$ | Pulse Width on RFOUT | 1 ETU = 128/$f_{CC}$ | 9.44 | | µs |
| $t_{JIT}$ | ASK modulation bit jitter | CRX14 to PICC | -0.5 | 0.5 | µs |
| $t_0$ | Antenna Reversal delay | Min = 64/$f_S$ | 75 | | µs |
| $t_1$ | Synchronization delay | Min = 80/$f_S$ | 94 | | µs |
| $t_{WDG}$ | Answer delay watchdog ($b_5$=0, $b_6$=0) | Request EOF rising edge to first Answer start bit | | 500 | µs |
| $t_{WDG}$ | Answer delay watchdog ($b_5$=0, $b_6$=1) | | | 5 | ms |
| $t_{WGD}$ | Answer delay watchdog ($b_5$=1, $b_6$=0) | | | 10 | ms |
| $t_{WDG}$ | Answer delay watchdog ($b_5$=1, $b_6$=1) | | | 19 | ms |
| $t_{DR}$ | Time Between Request characters | CRX14 to PICC | 9.44 | | µs |
| $P_A$ | RFOUT output power | | | 90 | mW |
| $t_{POR}$ | CRX14 Power-On delay | | | 20 | ms |

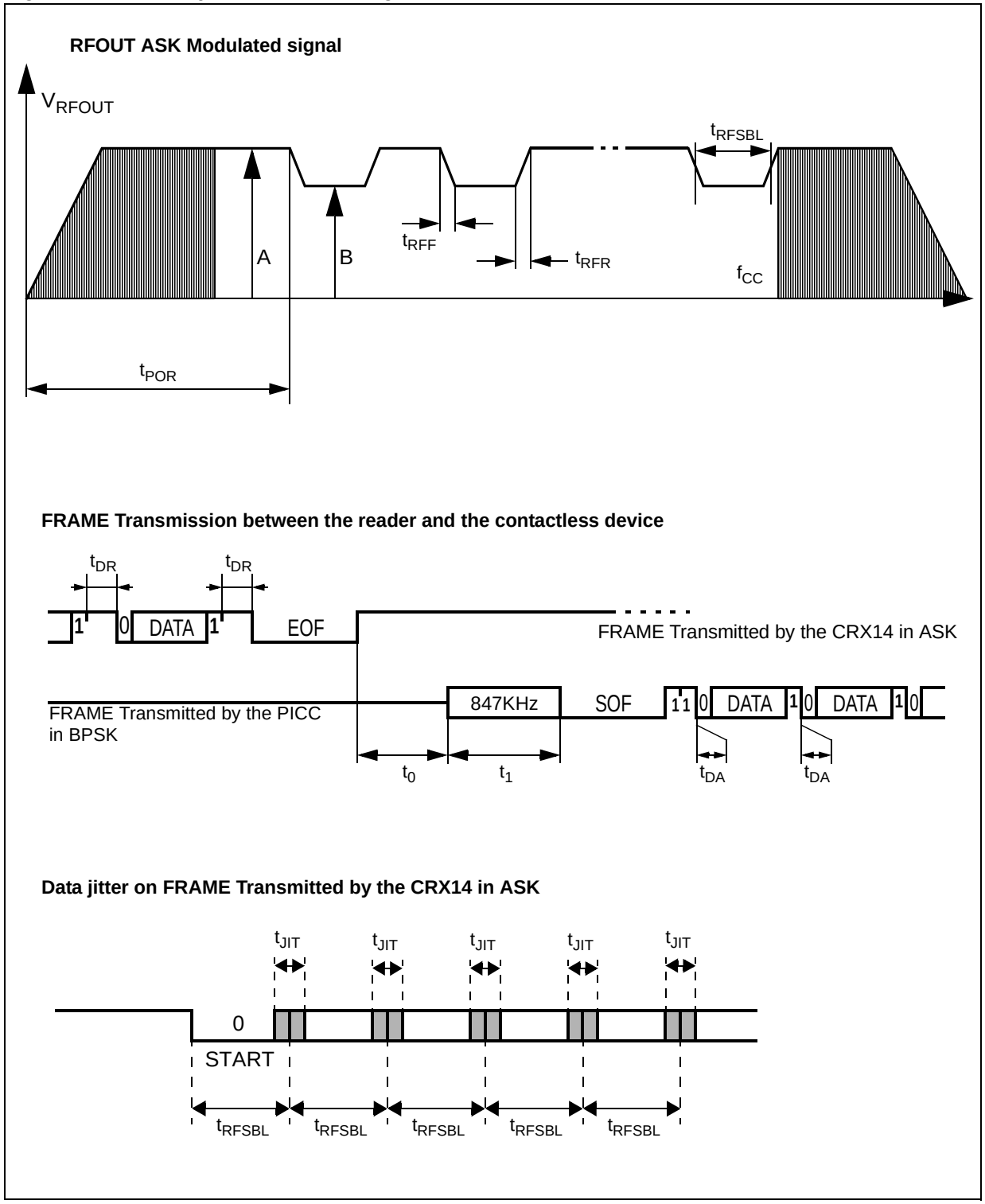
Note: Data specified in the table above are estimated or target values. All values can be updated during product qualification

**Table 19. RFIN AC Characteristics ($T_A$ = -20 to 85 °C; $V_{CC}$ = 5V ± 500mV)**

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{RFSBL}$ | PICC Pulse Width | 1 ETU = 128/$f_{CC}$ | 9.44 | | µs |
| $f_S$ | PICC Sub-carrier Frequency | $f_{CC}$/16 | 847.5 | | KHz |
| $t_{DA}$ | Time Between Answer characters | PICC to CRX14 | 0 | 19 | µs |
| $V_{DYN}$ | RFIN Dynamic Voltage Level | $V_{DYN}$ Max for $V_{OFFSET}$=$V_{CC}$/2 | 0.5 | $V_{CC}$/2 | V |
| $V_{OFFSET}$ | RFIN Offset Voltage Level | | 2 | 3 | V |
| $V_{RET}$ | RFIN Retro-modulation Level | | 120 | | mV |

Note: Data specified in the table above are estimated or target values. All values can be updated during product qualification

**Figure 24. CRX14 Synchronous Timing**



## TAG ACCESS DESCRIPTION USING THE CRX14 COUPLER

In all following I²C commands, the xxx value in the Device Select Code can be replace by all binary values (000, 001, 010, 011, 100, 101, 110, 111). These values are linked to the logic level applied to the E2, E1, E0 pad of the CRX14.

### Standard TAG command access description

Standard PICC commands like read and write are generated by the CRX14 using the input/output frame register. When the host need to send a standard frame command to the PICC, it need first to generates internally the complete frame bytes with the command code followed by the command parameters. The 2 bytes CRC must not be added as the CRX14 automatically add them during the RF transmission. When the frame is ready, the host has to write the request frame into the input/output frame register using the I²C write command specified in Figure 15 on page 15. After the I²C STOP condition, the CRX14 format the I²C bytes into the selected ISO characters (Table 12) and start to transmit on the RF the request frame to the PICC. After the RF transmission, the CRX14 wait for a PICC answer frame.

If the PICC answers, the received characters (Figure 23) are demodulated, decoded and stored into the input/output frame register as it is specified in Table 5. During all the RF transmission, the CRX14 disconnect itself from the I²C bus. On reception of the PICC EOF, the CRX14 check the CRC and re-connect itself to the I²C bus. The host can get the PICC answer frame by generating a input/output frame register read on the I²C bus as specified on Figure 16 or Figure 17.

If no answer is detected after a time-out delay fixed in the parameter register (bit $b_5$ & $b_6$), the input/output frame register is set as specified in Table 5.

**Figure 25. Standard TAG command: Request Frame Transmission**

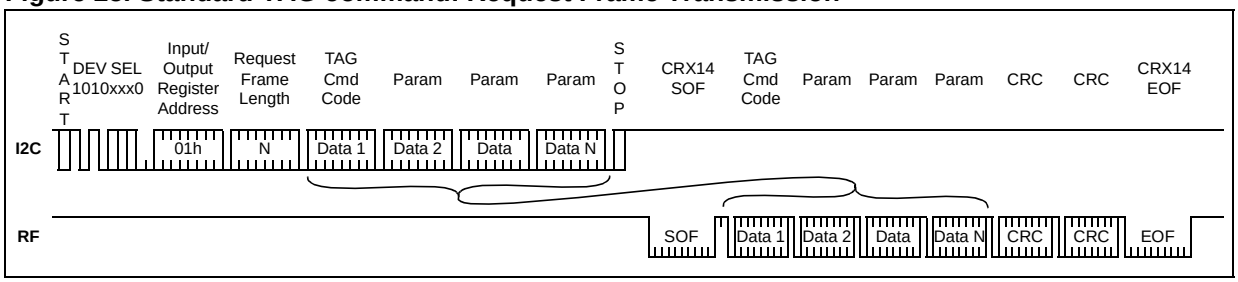



**Figure 26. Standard TAG command: Answer Frame Reception**

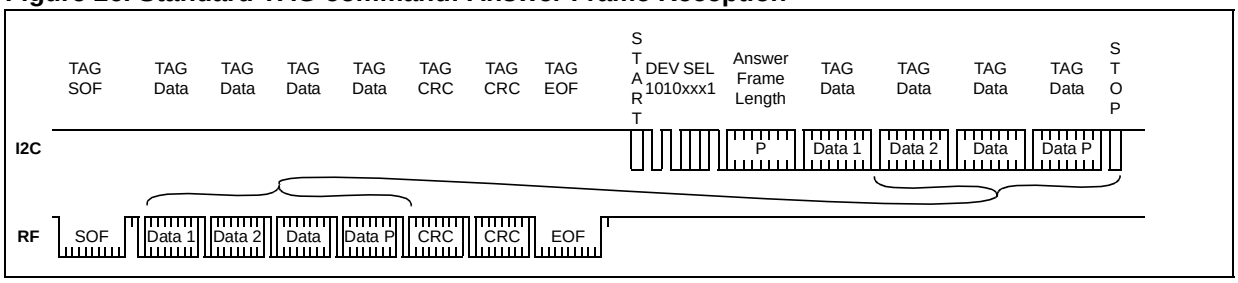
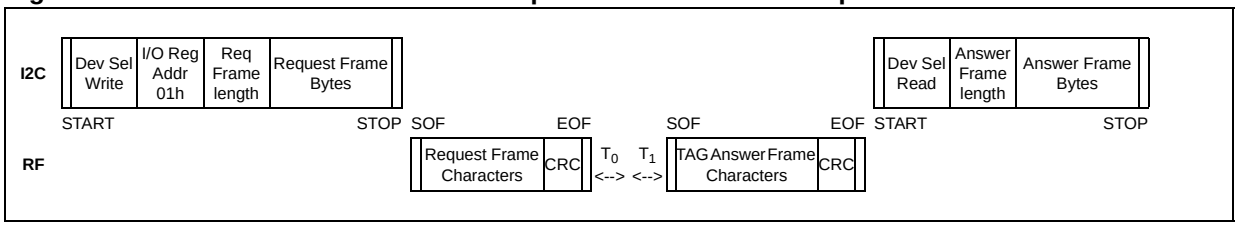



**Figure 27. Standard TAG Command: Complete TAG access description**

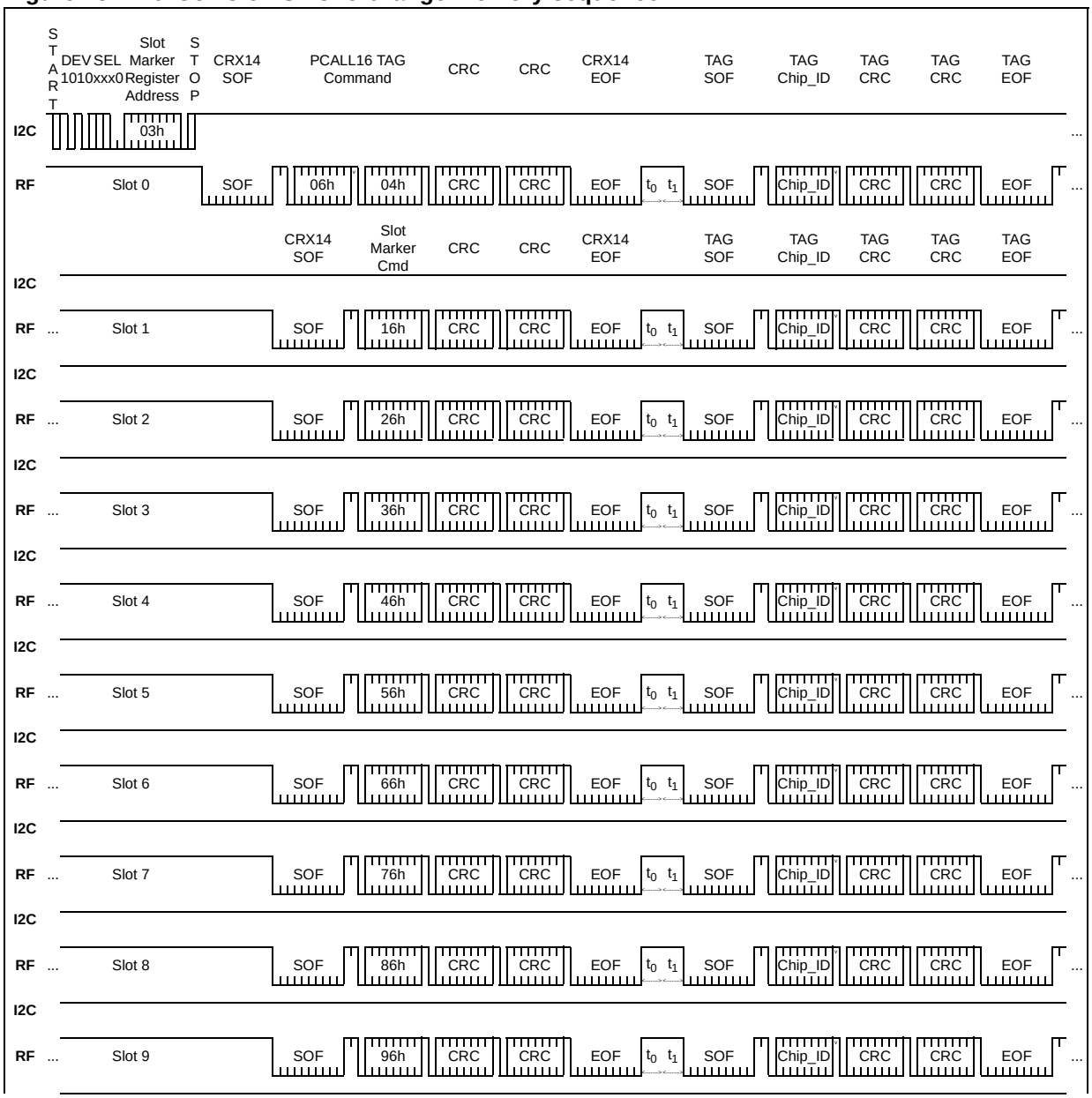


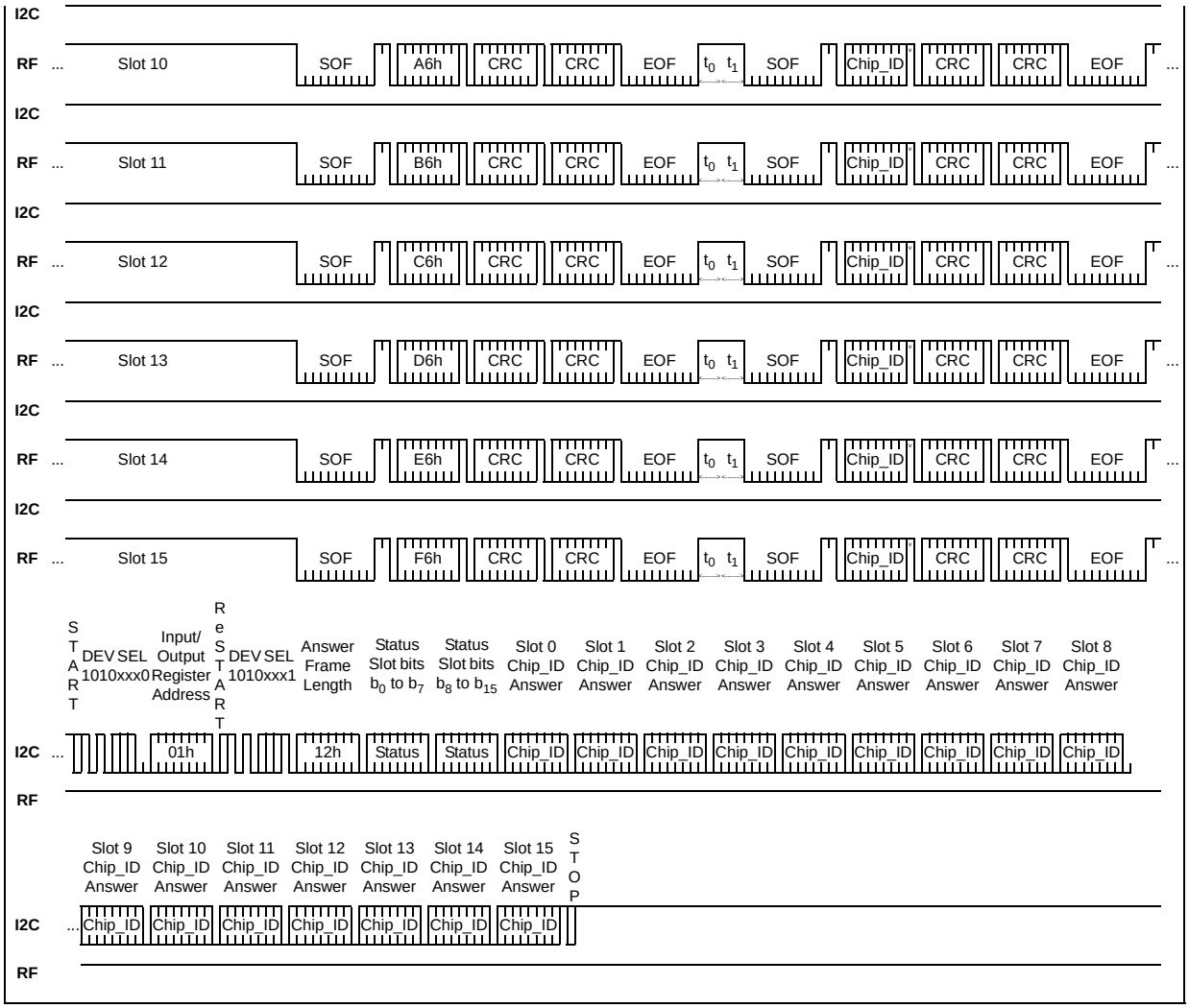
### Anti-Collision TAG sequence description

The CRX14 allows to identify ST short range memory using a proprietary anti-collision system. Using the slot marker register I²C write access (Figure 18), the CRX14 automatically generates a 16 slots anti-collision sequence and stores the identified Chip_ID into the input/output frame register as specified in Table 6.

After the slot marker register I²C write, the CRX14 generates a PCALL16 command on the RF followed by 15 SLOT_MARKER commands from SLOT_MARKER(1) to SLOT_MARKER(15). After each command, the CRX14 wait for a tag answer. If the answer is correctly decoded, the corresponding Chip_ID is stored in the Input/output frame register. If there is no answer or if the answer is wrong (CRC error for example), the CRX14 stores an error code into the input/output frame register. At the end of the sequence, the host has to read the input/output frame register in order to retrieve all the identified Chip_ID.

**Figure 28. Anti-Collision ST short range memory sequence**



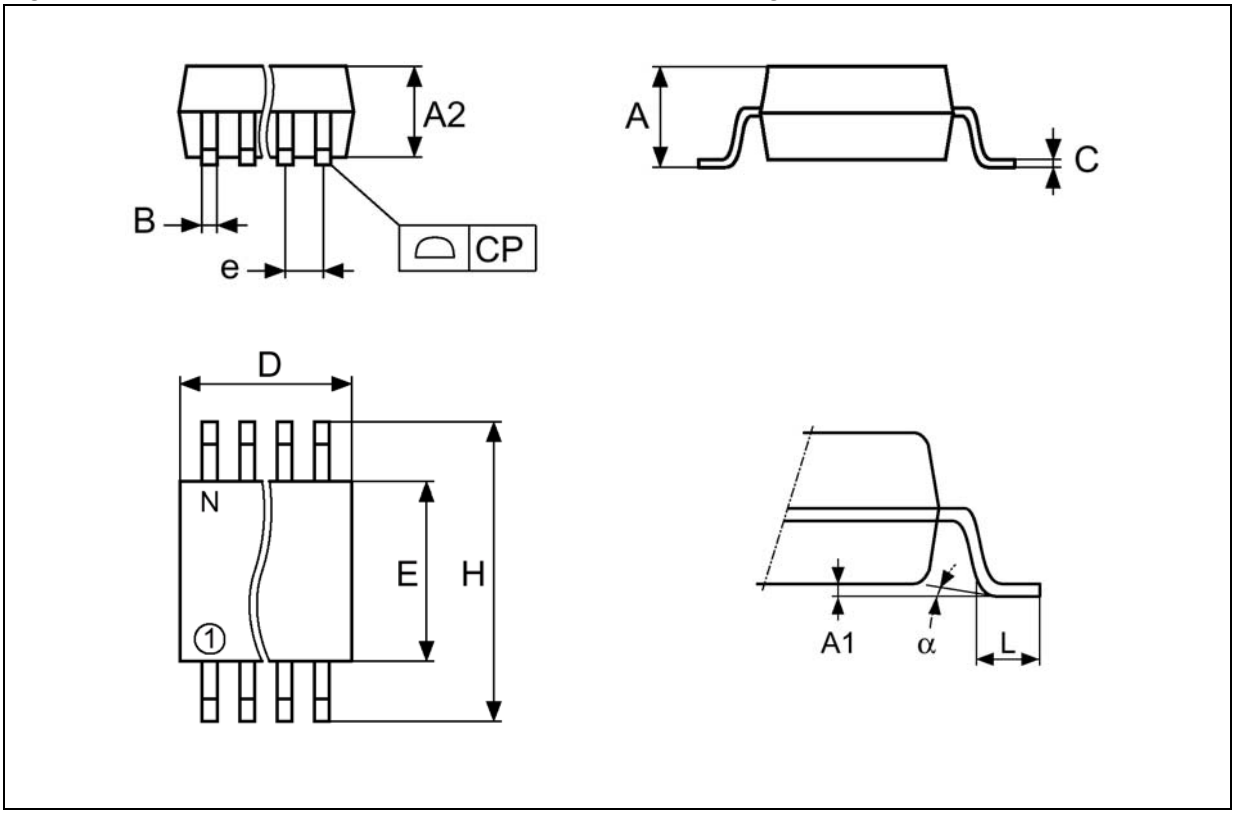


## ANNEX: ISO14443 TYPE B CRC CALCULATION

```
#include <stdio.h>
#include <stdlib.h>
#include <string.h>
#include <ctype.h>
#define BYTE  unsigned char
#define USHORTunsigned short

unsigned short UpdateCrc(BYTE ch, USHORT *lpwCrc)
{
  ch = (ch^(BYTE)((*lpwCrc) & 0x00FF));
  ch = (ch^(ch<<4));
  *lpwCrc = (*lpwCrc >> 8)^((USHORT)ch << 8)^((USHORT)ch<<3)^((USHORT)ch>>4);
  return(*lpwCrc);
}

void ComputeCrc(char *Data, int Length, BYTE *TransmitFirst, BYTE *TransmitSecond)
{
BYTE chBlock; USHORTt wCrc;
  wCrc = 0xFFFF; // ISO 3309
  do
    {
    chBlock = *Data++;
    UpdateCrc(chBlock, &wCrc);
    } while (--Length);
  wCrc = ~wCrc; // ISO 3309
  *TransmitFirst = (BYTE) (wCrc & 0xFF);
  *TransmitSecond = (BYTE) ((wCrc >> 8) & 0xFF);
  return;
}

int main(void)
{
BYTE BuffCRC_B[10] = {0x0A, 0x12, 0x34, 0x56}, First, Second, i;
  printf("Crc-16 G(x) = x^16 + x^12 + x^5 + 1”);
  printf("CRC_B of [ ");
  for(i=0; i<4; i++)
    printf("%02X ",BuffCRC_B[i]);
  ComputeCrc(BuffCRC_B, 4, &First, &Second);
  printf("] Transmitted: %02X then %02X.”, First, Second);
  return(0);
}
```

## PACKAGE MECHANICAL INFORMATION

**Figure 29. SO16 Narrow- 16 lead Plastic Small Outline Package**




Note: Drawing is not to scale

**Table 20. SO16 - 16 lead Plastic Small Outline Package Mechanical Data**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ. | Min. | Max. | Typ. | Min. | Max. |
| A | | | 1.75 | | | 0.069 |
| A1 | | 0.10 | 0.25 | | 0.004 | 0.010 |
| A2 | | | 1.60 | | | 0.063 |
| B | | 0.35 | 0.46 | | 0.014 | 0.018 |
| C | | 0.19 | 0.25 | | 0.007 | 0.010 |
| D | | 9.80 | 10.00 | | 0.386 | 0.394 |
| E | | 3.80 | 4.00 | | 0.150 | 0.158 |
| e | 1.27 | - | - | 0.050 | - | - |
| H | | 5.80 | 6.20 | | 0.228 | 0.244 |
| L | | 0.40 | 1.27 | | 0.016 | 0.050 |
| a | | 0° | 8° | | 0° | 8° |
| N | 16 | | | 16 | | |
| CP | | | 0.10 | | | 0.004 |

## ORDERING INFORMATION SCHEME

Example CRX14 - MQ / XXX

**Delivery Form**

MQ SO16 Narrow package

For a full list of the available options, please see the current Memory Shortform Catalogue.

For further information on any aspect of this device, please contact your nearest ST Sales Office.

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STMicroelectronics

EEPROM and ASM Division

Z.I. de Rousset

B.P. 2

13106 ROUSSET Cedex

FRANCE

Fax number for confidential information enquiries: 04.42.68.87.93

E-mail: memories.contactless@st.com