# **8-Bit Static Shift Register**

The MC14014B and MC14021B 8—bit static shift registers are constructed with MOS P—channel and N—channel enhancement mode devices in a single monolithic structure. These shift registers find primary use in parallel—to—serial data conversion, synchronous and asynchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

- Synchronous Parallel Input/Serial Output (MC14014B)
- Asynchronous Parallel Input/Serial Output (MC14021B)
- Synchronous Serial Input/Serial Output
- · Full Static Operation
- "Q" Outputs from Sixth, Seventh, and Eighth Stages
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range
- MC14014B Pin-for-Pin Replacement for CD4014B
- MC14021B Pin-for-Pin Replacement for CD4021B

## MAXIMUM RATINGS\* (Voltages Referenced to VSS)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	- 0.5 to + 18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	$-0.5$ to $V_{DD} + 0.5$	V
l <sub>in</sub> , l <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
PD	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature (8–Second Soldering)	260	°C

<sup>\*</sup> Maximum Ratings are those values beyond which damage to the device may occur. †Temperature Derating:

Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C Ceramic "L" Packages: – 12 mW/°C From 100°C To 125°C

# MC14014B MC14021B



L SUFFIX CERAMIC CASE 620



P SUFFIX PLASTIC CASE 648



D SUFFIX SOIC CASE 751B

### **ORDERING INFORMATION**

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

 $T_{\Delta} = -55^{\circ}$  to 125°C for all packages.

## TRUTH TABLE

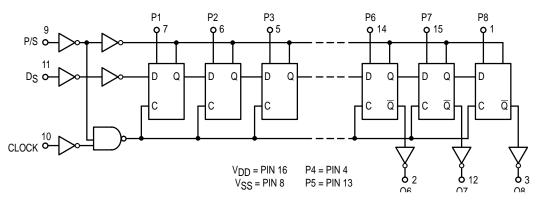
#### **SERIAL OPERATION:**

t	Clock	DS	P/S	Q6 t=n+6	Q7 t=n+7	Q8 t=n+8
n	\	0	0	0	?	?
n+1	_	1	0	1	0	?
n+2		0	0	0	1	0
n+3		1	0	1	0	1
	7	Х	0	Q6	Q7	Q8

### **PARALLEL OPERATION:**

CI					
MC14014B MC14021B		DS	P/S	Pn	*Qn
	Х	Х	1	0	0
	Х	Х	1	1	1

\* Q6, Q7, & Q8 are available externally X = Don't Care



LOGIC DIAGRAM

REV 3 1/94



**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V<sub>SS</sub>)

		V <sub>DD</sub>	- 5	5°C		25°C		125	5°C	
Characteristic	Symbol	Vdc	Min	Max	Min	Typ #	Max	Min	Max	Unit
Output Voltage "0" Leve	VOL	5.0 10 15	_ _ _	0.05 0.05 0.05	_ _ _	0 0 0	0.05 0.05 0.05	_ _ _	0.05 0.05 0.05	Vdc
V <sub>in</sub> = 0 or V <sub>DD</sub> "1" Leve	VOH	5.0 10 15	4.95 9.95 14.95	_ _ _	4.95 9.95 14.95	5.0 10 15	_ _ _	4.95 9.95 14.95	_ _ _	Vdc
Input Voltage "0" Leve (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	VIL	5.0 10 15		1.5 3.0 4.0	_ _ _	2.25 4.50 6.75	1.5 3.0 4.0		1.5 3.0 4.0	Vdc
$(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$ "1" Leve $(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$ $(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$	VIH	5.0 10 15	3.5 7.0 11	_ _ _	3.5 7.0 11	2.75 5.50 8.25	_ _ _	3.5 7.0 11	_ _ _	Vdc
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) Source (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	ЮН	5.0 5.0 10 15	- 3.0 - 0.64 - 1.6 - 4.2	_ _ _ _	- 2.4 - 0.51 - 1.3 - 3.4	- 4.2 - 0.88 - 2.25 - 8.8	_ _ _ _	- 1.7 - 0.36 - 0.9 - 2.4	_ _ _ _	mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ Sink $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	lOL	5.0 10 15	0.64 1.6 4.2	_ _ _	0.51 1.3 3.4	0.88 2.25 8.8	_ _ _	0.36 0.9 2.4	_ _ _	mAdc
Input Current	l <sub>in</sub>	15	_	± 0.1	_	±0.00001	± 0.1	_	± 1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	_	_	_	_	5.0	7.5	_	_	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0 10 15	_ _ _	5.0 10 15	_ _	0.005 0.010 0.015	5.0 10 15	_ _ _	150 300 600	μAdc
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	lΤ	5.0 10 15			$I_{T} = (1$	.75 μA/kHz) .50 μA/kHz) .25 μA/kHz)	f + I <sub>DD</sub>			μAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: IT is in  $\mu$ A (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.0015.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}.$  Unused inputs must always be tied to an appropriate logic voltage

level (e.g., either VSS or VDD). Unused outputs must be left open.

### **PIN ASSIGNMENT**

P8 [	1 ●	16	□ V <sub>DD</sub>
Q6 [	2	15	] P7
Q8 [	3	14	] P6
P4 [	4	13	] P5
P3 [	5	12	] Q7
P2 [	6	11	] D <sub>S</sub>
P1 [	7	10	] C
ss E	8	9	] P/S

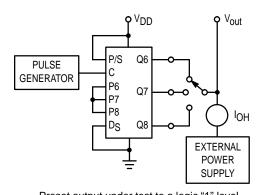
<sup>\*\*</sup>The formulas given are for the typical characteristics only at 25  $^{\circ}\text{C}.$ 

<sup>†</sup>To calculate total supply current at loads other than 50 pF:

Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time  t <sub>TLH</sub> , t <sub>THL</sub> = (1.5 ns/pF) C <sub>L</sub> + 25 ns  t <sub>TLH</sub> , t <sub>THL</sub> = (0.75 ns/pF) C <sub>L</sub> + 12.5 ns  t <sub>TLH</sub> , t <sub>THL</sub> = (0.55 ns/pF) C <sub>L</sub> + 9.5 ns	tTLH, tTHL	5.0 10 15	_ _ _	100 50 40	200 100 80	ns
Propagation Delay Time (Clock to Q, P/S to Q)  tpHL, tpLH = (1.7 ns/pF) C <sub>L</sub> + 315 ns  tpHL, tpLH = (0.66 ns/pF) C <sub>L</sub> + 137 ns  tpHL, tpLH = (0.5 ns/pF) C <sub>L</sub> + 90 ns	<sup>t</sup> PLH, <sup>t</sup> PHL	5.0 10 15	_ _ _	400 170 115	800 340 230	ns
Clock Pulse Width	tWH	5.0 10 15	400 175 135	150 75 40	_ _ _	ns
Clock Frequency	f <sub>C</sub> l	5.0 10 15	_ _ _	3.0 6.0 8.0	1.5 3.0 4.0	MHz
Parallel/Serial Control Pulse Width	tWH	5.0 10 15	400 175 135	150 75 40	_ _ _	ns
Setup Time P/S to Clock	<sup>t</sup> su	5.0 10 15	200 100 80	100 50 40	_ _ _	ns
Hold Time Clock to P/S	<sup>t</sup> h	5.0 10 15	20 20 25	- 2.5 - 10 0	_ _ _	ns
Setup Time Data (Parallel or Serial) to Clock or P/S	t <sub>su</sub>	5.0 10 15	350 80 60	150 50 30	_ _ _	ns
Hold Time Clock to D <sub>S</sub>	t <sub>h</sub>	5.0 10 15	45 35 35	0 0 5	_ _ _	ns
Hold Time Clock to P <sub>n</sub>	th	5.0 10 15	50 45 45	25 20 20	_ _ _	ns
Input Clock Rise Time	t <sub>r(Cl)</sub>	5.0 10 15	_ _ _	_ _ _	15 5 4	μs

<sup>\*</sup>The formulas given are for the typical characteristics only at 25°C.

<sup>#</sup>Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



Preset output under test to a logic "1" level.

**Figure 1. Output Source Current Test Circuit** 

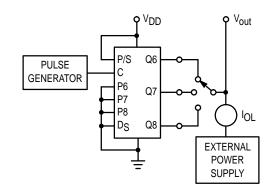


Figure 2. Output Sink Current Test Circuit

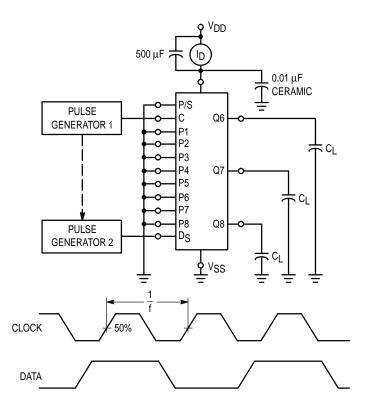


Figure 3. Power Dissipation Test Circuit and Waveform

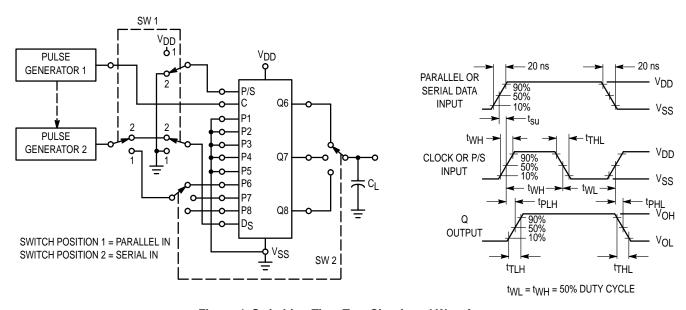
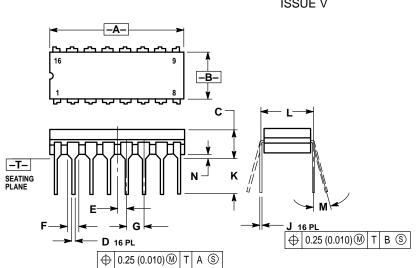


Figure 4. Switching Time Test Circuit and Waveforms

## **OUTLINE DIMENSIONS**

# **L SUFFIX** CERAMIC DIP PACKAGE CASE 620-10 ISSUE V



#### NOTES:

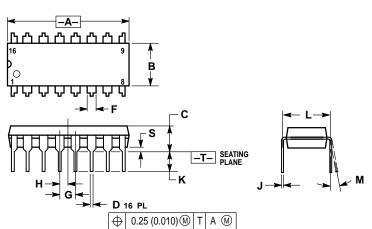
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

- ANSI Y14.5M, 1982.
  CONTROLLING DIMENSION: INCH.
  DIMENSION L TO CENTER OF LEAD WHEN
  FORMED PARALLEL.
  DIMENSION F MAY NARROW TO 0.76 (0.030)
  WHERE THE LEAD ENTERS THE CERAMIC

	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.750	0.785	19.05	19.93
В	0.240	0.295	6.10	7.49
С		0.200		5.08
D	0.015	0.020	0.39	0.50
Е	0.050	BSC	1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC 2.54 B		BSC	
Н	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300	0.300 BSC		BSC
М	0°	15°	0 °	15°
N	0.020	0.040	0.51	1.01

# **P SUFFIX**

PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



#### NOTES:

- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

  2. CONTROLLING DIMENSION: INCH.

  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

  5. ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.740	0.770	18.80	19.55
В	0.250	0.270	6.35	6.85
С	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100	BSC	2.54	BSC
Н	0.050	BSC	1.27	BSC
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10 °
S	0.020	0.040	0.51	1.01

#### **OUTLINE DIMENSIONS**



- DIMENSIONING AND TOLERANCING PER ANSI
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.

  MAXIMUM MOLD PROTRUSION 0.15 (0.006)
- PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
  PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	METERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	9.80	10.00	0.386	0.393
В	3.80	4.00	0.150	0.157
U	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050	BSC
7	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
М	0°	7°	0°	7°
Р	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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