

RADLAND LAPC-1 AUDIO CHIPSET SUPPLEMENT  
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# Radland LAPC-1 Audio Chipset Supplement

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*Target System: BRADSONIC 69000 (1988)*

*LAPC: Low-Latency Audio Packet Controller*

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## 1. Overview of the LAPC-1 Interface

The Radland LAPC-1 chipset is designed to handle low-latency, packetized audio streams, primarily for telecommunication applications (e.g., BBS audio). The chip operates via direct memory-mapped access. Proper initialization and streaming require strict adherence to the register access sequence and timing constraints.

## 2. Memory-Mapped Control Registers

The LAPC-1 interfaces with the BRADSONIC 69000 memory bus across five critical addresses in the 0Cx<sub>xxx</sub> memory block. These addresses are not contiguous and must be accessed individually.

Table 1: LAPC-1 Memory Map (I/O Addresses)

| Address (Hex) | Register Name            | Purpose   | R/W |
|---------------|--------------------------|---|-----|
| \$C400        | Master Power Register    | Write 01 to enable the primary audio circuitry.       | W   |
| \$C401        | Left Channel Stream      | Target for 8-bit PCM data stream (Mono or Left).      | W   |
| \$C402        | Right Channel Stream     | Target for 8-bit PCM data stream (Mono or Right).     | W   |
| \$C403        | Data Ready Flag          | Read status. Returns 01 when \$C800 has a new packet. | R   |
| \$C800        | Audio Data Packet Buffer | Read the current 8-bit PCM sample (single byte).      | R   |

## Operational Principles

- **System Constraint:** When the system is actively receiving a broadcast stream, the \$C403 Data Ready Flag will **fluctuate** rapidly between 00 (Empty) and 01 (Ready).
- **Prioritization:** The Master Power Register (\$C400) must be enabled before any streaming attempt.
- **Volume:** If no driver is active, writing a value to \$C401 or \$C402 sets the static output volume; however, when the streaming loop is running, the data written acts as the audio sample itself. For initialization, use 80 hex (mid-level) to test the speakers.

## 3. Low-Level Driver Construction

To establish a functioning stream, the driver must be broken into two segments. The assembly logic should be kept minimal and efficient.

### 3.1. Initialization Sequence

This sequence must execute only once when the system loads the driver.

1. \*\*Enable Chipset:\*\* Load the activation byte (01) into the accumulator. Store this byte into the \*\*Master Power Register (\$C400)\*\*.
2. \*\*Left Channel Diagnostic:\*\* Load the maximum volume byte (FF) into the accumulator. Store this byte into the \*\*Left Channel Stream (\$C401)\*\*. Store the mute byte (00) into the \*\*Right Channel Stream (\$C402)\*\*. A brief delay should be inserted here to allow the test signal to be audible on the left speaker.
3. \*\*Right Channel Diagnostic:\*\* Load the maximum volume byte (FF) into the accumulator. Store this byte into the \*\*Right Channel Stream (\$C402)\*\*. Store the mute byte (00) into the \*\*Left Channel Stream (\$C401)\*\*. A brief delay should be inserted here to allow the test signal to be audible on the right speaker.
4. \*\*Restore Default Volume (Stereo):\*\* Load the default volume byte (80) into the accumulator. Store this byte into the \*\*Left Channel Stream (\$C401)\*\* and then again into the \*\*Right Channel Stream (\$C402)\*\*.
5. \*\*Termination:\*\* The routine should conclude and hand over control to the continuous loop routine.

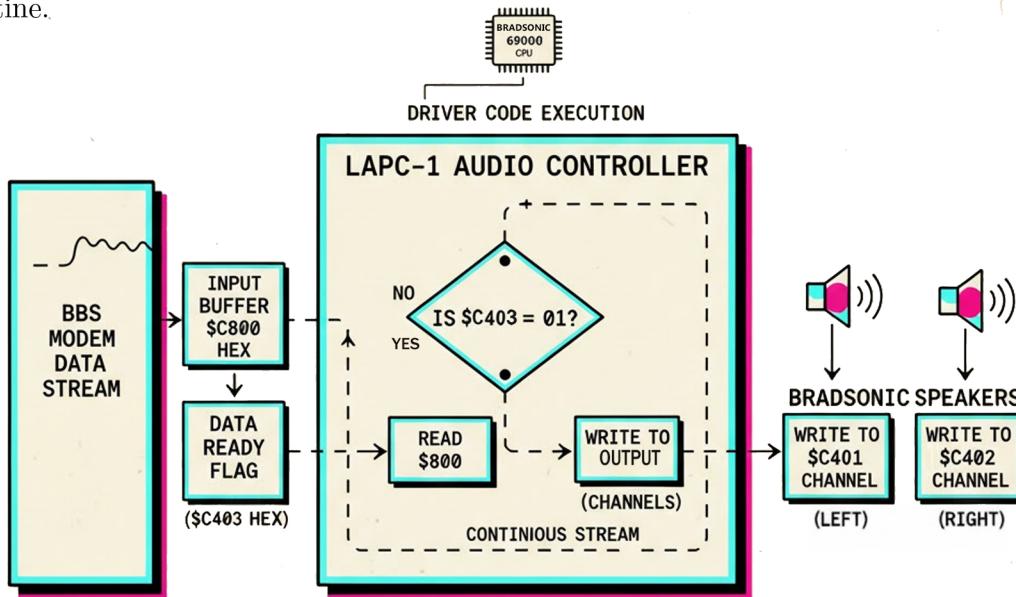


Fig. 1. Driver Logic for Continuous Audio Playback. Timing Criticality Highlighted.



### 3.2. Packet Streaming Loop

This is the continuous routine that manages the flow of incoming audio packets from the BBS modem stream. This loop cannot terminate while audio is expected.

1. \*\*Data Check:\*\* Load the status from the \*\*Data Ready Flag (\$C403)\*\*. Compare this status to the ready state (01). If the status does not match, the routine must \*\*branch\*\* back to the beginning of this check step and wait.
2. \*\*Data Transfer:\*\* Once the Data Ready Flag signals 01:
  - Load the 8-bit sample from the \*\*Audio Data Packet Buffer (\$C800)\*\*.
  - Immediately store this sample into the \*\*Left Channel Stream (\$C401)\*\*.
  - Immediately store this sample into the \*\*Right Channel Stream (\$C402)\*\*.
3. \*\*Continuation:\*\* The routine must then execute an \*\*unconditional jump\*\* back to the beginning of the Data Check step to wait for the next packet.