Project Selection and Team Formation Document

Project Team Composition (2-4 members)

Team Members:
1. Li, Yuhan, CE (Hardware)

2. Li, Songlin, CE (Hardware)

3. Jiang, Rongyou, CE (Hardware)

4. Lin, Ziqin, CE (Software)

Project Title: A Hardware Implementation of a CPU Value Prediction Unit

Project Supervisor: Prof. Roy Eagleson

Brief Project Description

In CPU pipelines, *true data dependency* occurs when one instruction must wait on the execution result of one or more previous instructions. Adjacent instructions with true data dependencies will cause the processing unit to idle, creating negative impacts on the efficiency of the pipeline. *Value prediction* is one technique for reducing pipeline idle time. It predicts the execution results of previous instructions before they finish and executes the dependent instructions speculatively. Research has shown that the instruction execution results are significantly predictable, and processors could utilize value prediction algorithms to enhance pipeline performance. However, value prediction units are not officially implemented in CPUs on the market so far.

In this project, we will be implementing one of the value prediction algorithms and integrate the value predictor into an existing implementation of a RISC CPU. The prototype processor will be validated using an FPGA, and the value prediction accuracy and improvement to the execution efficiency will be examined. Furthermore, we will carry out a brief study where the implemented value prediction hardware is compared to other true data dependency pipeline enhancements such as out-of-order execution, in terms of design complexity, safety, overall speed-up, size, and energy efficiency.

Successful development and presentation of this project will require an FPGA development platform, source code of a RISC CPU, digital logic verification tools, and CPU benchmark tools. A compatible OS is an optional method to test the prototype, and it might be required for running CPU benchmark tools.