LibreSilicon's Standard Cell Library

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Abstract

Table 1: Document Revision History

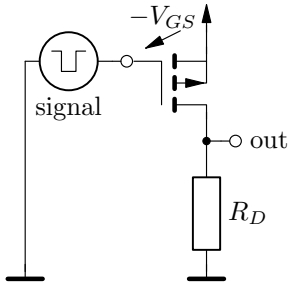
VERSION	DATE	DESCRIPTION	TRACKING NOTES
Draft 0.0	2018-02-01	START w/ empty document	-

1 CMOS in a nutshell

This basic initial project is dedicated to the CMOS Technology only and for this reason two types of metal–oxide–semiconductor field-effect transistors (MOSFET) are required.

Historicaly, the first chips with MOSFETs on the mass market were p-channel MOSFETs in enhancement-mode.

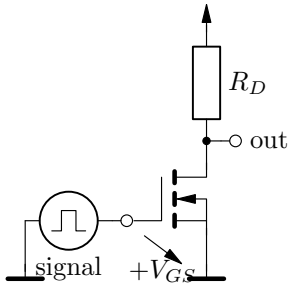
Figure 1: enhancement-mode PMOS transistor use-case



The sectional view of a PMOS transistor in silicon is being shown below

Historicaly later, faster chips with MOSFETs on the mass market were marked as n-channel MOSFETs in enhancement mode also.

Figure 2: enhancement-mode NMOS transistor use-case



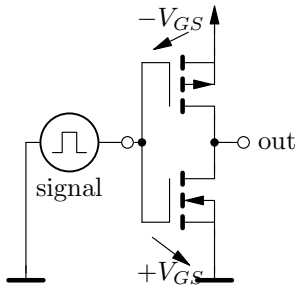
The sectional view of a NMOS transistor in silicon is being shown here also.

Both technologies, the older NMOS as the newer PMOS, have the same disadvantage. Every time, the transistor is switched on, the current between Drain and Source of the transistor is limited by the Resistor on Drain only. Higher currents here meaning higher power consumption for the chip where the transistors are integrated also. If the transistors are switched off, no currents flows between Drain and Source anymore, the power consumption of the chip also goes low.

Et violà, the US-Patent with Number 3356858[1]changed the world and combines both technologies to the new complementary metal-oxide-semiconductor

(CMOS) technology. Instead of every transistor is working against a weak resistor, the transistor works against a complementary switched-off transistor. With the Eyes of our antecessor CMOS doubles the transistor count, but contemporary chips all are build in CMOS.

Figure 3: complementary PMOS and NMOS transistor couple use-case



The sectional view of a NMOS and PMOS transistors couple in silicon - building the CMOS technology - are being shown here also.

[1] https://www.google.com/patents/US3356858

2 Design Decisions

3 Cell Descriptions

Cell

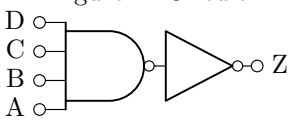
AND4 - a 4-input AND gate

Synopsys

AND4(Z, D, C, B, A)
AND4(Z, D, C, B, A, Vdd, Gnd)

Description

Figure 4: Circuit



Truth Table

Table 2: $Z = D \wedge C \wedge B \wedge A$

D	C	B	A	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Usage
Fan-in / Fan-out
Layout
Files

Cell

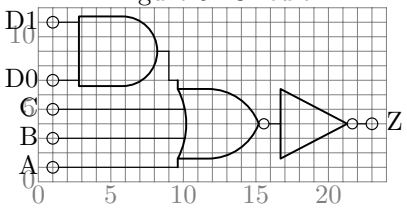
AO2111 - a 2-1-1-1-input AND-OR gate

Synopsys

AO2111(Z, D1, D0, C, B, A)
AO2111(Z, D1, D0, C, B, A, Vdd, Gnd)

Description

Figure 5: Circuit



Truth Table

Usage
Fan-in / Fan-out
Layout
Files
See also

AO3111 - a 3-1-1-1-input AND-OR gate [Page ??]
AO3211 - a 3-2-1-1-input AND-OR gate [Page ??]
AO3221 - a 3-2-2-1-input AND-OR gate [Page ??]
AO3222 - a 3-2-2-2-input AND-OR gate [Page ??]
AO3311 - a 3-3-1-1-input AND-OR gate [Page ??]
AO3321 - a 3-3-2-1-input AND-OR gate [Page ??]
AO3331 - a 3-3-3-1-input AND-OR gate [Page ??]
AO3332 - a 3-3-3-2-input AND-OR gate [Page ??]
AO3333 - a 3-3-3-3-input AND-OR gate [Page ??]
AO4111 - a 4-1-1-1-input AND-OR gate [Page ??]
AO4211 - a 4-2-1-1-input AND-OR gate [Page ??]
AO4221 - a 4-2-2-1-input AND-OR gate [Page ??]
AO4222 - a 4-2-2-2-input AND-OR gate [Page ??]
AO4311 - a 4-3-1-1-input AND-OR gate [Page ??]
AO4321 - a 4-3-2-1-input AND-OR gate [Page ??]
AO4322 - a 4-3-2-2-input AND-OR gate [Page ??]
AO4331 - a 4-3-3-1-input AND-OR gate [Page ??]
AO4332 - a 4-3-3-2-input AND-OR gate [Page ??]
AO4333 - a 4-3-3-3-input AND-OR gate [Page ??]
AO4411 - a 4-4-1-1-input AND-OR gate [Page ??]
AO4421 - a 4-4-2-1-input AND-OR gate [Page ??]
AO4431 - a 4-4-3-1-input AND-OR gate [Page ??]

Table 3: $Z = (D1 \wedge D0) \vee C \vee B \vee A$

D1	D0	C	B	A	Z
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	1
0	0	0	1	1	1
0	0	1	0	0	1
0	0	1	0	1	1
0	0	1	1	0	1
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	0	1	1
0	1	0	1	0	1
0	1	0	1	1	1
0	1	1	0	0	1
0	1	1	0	1	1
0	1	1	1	0	1
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	0	1	1
1	0	0	1	0	1
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	0	1	1
1	0	1	1	0	1
1	0	1	1	1	1
1	1	0	0	0	1
1	1	0	0	1	1
1	1	0	1	0	1
1	1	0	1	1	1
1	1	1	0	0	1
1	1	1	0	1	1
1	1	1	1	0	1
1	1	1	1	1	1

Cell

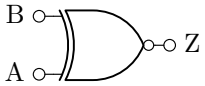
EQ2 - a 2-input Equality (or XNOR) gate

Synopsys

EQ2(Z, B, A)
EQ2(Z, B, A, Vdd, Gnd)

Description

Figure 6: Circuit



Truth Table

Table 4: $Z = \neg(B \oplus A)$

B	A	Z
0	0	1
0	1	0
1	0	0
1	1	1

Usage
Fan-in / Fan-out
Layout
Files
See also

XOR2 - a 2-input Exclusive-OR (or XOR) gate [Page 16]

Cell

NAND2 - a 2-input Not-AND (or NAND) gate

Synopsys

NAND2(Z, B, A)
NAND2(Z, B, A, Vdd, Gnd)

Description

Figure 7: Circuit

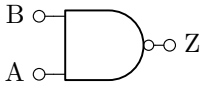
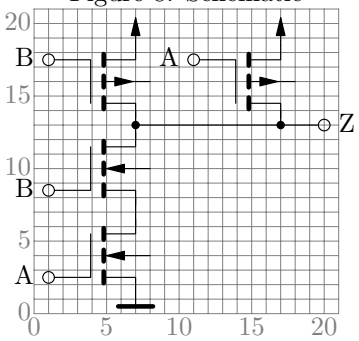


Figure 8: Schematic



Truth Table

Table 5: $Z = \neg(B \wedge A)$

B	A	Z
0	0	1
0	1	1
1	0	1
1	1	0

Usage
Fan-in / Fan-out
Layout
Files
See also

NAND3 - a 3-input Not-AND (or NAND) gate [Page 11]

Cell

NAND3 - a 3-input Not-AND (or NAND) gate

Synopsys

NAND3(Z, C, B, A)
NAND3(Z, C, B, A, Vdd, Gnd)

Description

Figure 9: Circuit

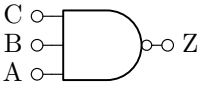
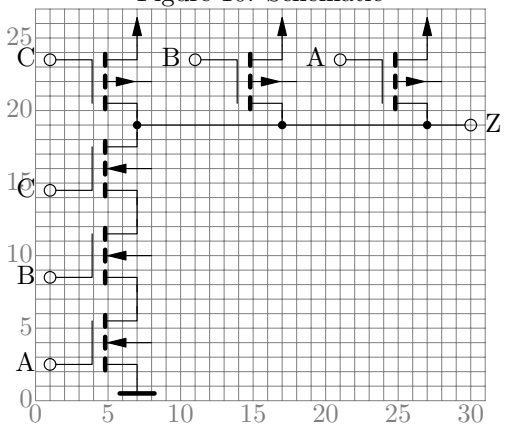


Figure 10: Schematic



Truth Table

Table 6: $Z = \neg(C \wedge B \wedge A)$

C	B	A	Z
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Cell

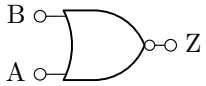
NOR2 - a 2-input Not-OR (or NOR) gate

Synopsys

NOR2(Z, B, A)
NOR2(Z, B, A, Vdd, Gnd)

Description

Figure 11: Circuit



Truth Table

Table 7: $Z = \neg(B \vee A)$

B	A	Z
0	0	1
0	1	0
1	0	0
1	1	0

Usage
Fan-in / Fan-out
Layout
Files
See also

NOR3 - a 3-input Not-OR (or NOR) gate [Page 14]

Cell

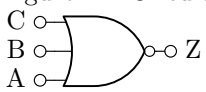
NOR3 - a 3-input Not-OR (or NOR) gate

Synopsys

NOR3(Z, C, B, A)
NOR3(Z, C, B, A, Vdd, Gnd)

Description

Figure 12: Circuit



Truth Table

Table 8: $Z = \neg(C \vee B \vee A)$

C	B	A	Z
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Usage
Fan-in / Fan-out
Layout
Files
See also

NOR2 - a 2-input Not-OR (or NOR) gate [Page 13]

Cell

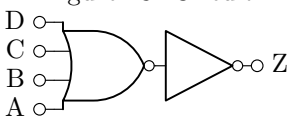
OR4 - a 4-input OR gate

Synopsys

OR4(Z, D, C, B, A)
OR4(Z, D, C, B, A, Vdd, Gnd)

Description

Figure 13: Circuit



Truth Table

Table 9: $Z = D \vee C \vee B \vee A$

D	C	B	A	Z
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Usage
Fan-in / Fan-out
Layout
Files

Cell

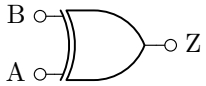
XOR2 - a 2-input Exclusive-OR (or XOR) gate

Synopsys

XOR2(Z, B, A)
XOR2(Z, B, A, Vdd, Gnd)

Description

Figure 14: Circuit



Truth Table

Table 10: $Z = B \oplus A$

B	A	Z
0	0	0
0	1	1
1	0	1
1	1	0

Usage
Fan-in / Fan-out
Layout
Files
See also

EQ2 - a 2-input Equality (or XNOR) gate [Page 9]