LibreSilicon's Standard Cell Library

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Abstract

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For further clarification consult the complete documentation of the process.

Table 1: Document Revision History

VERSION	DATE	DESCRIPTION	TRACKING NOTES
Draft 0.0	2018-02-01	START w/ empty document	-

0.1 CMOS in a nutshell

This basic initial project is dedicated to the CMOS Technology only and for this reason two types of metal–oxide–semiconductor field-effect transistors (MOS-FET) are required.

Historicaly, the first chips with MOSFETs on the mass market were p-channel MOSFETs in enhancement-mode.

Figure 1: enhancement-mode PMOS transistor use-case
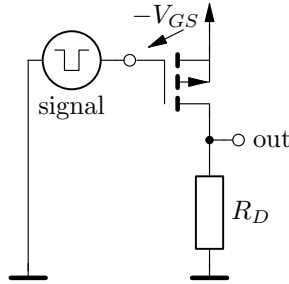
The sectional view of a PMOS transistor in silicon is being shown below

Historicaly later, faster chips with MOSFETs on the mass market were marked as n-channel MOSFETs in enhancement mode also.

Figure 2: enhancement-mode NMOS transistor use-case
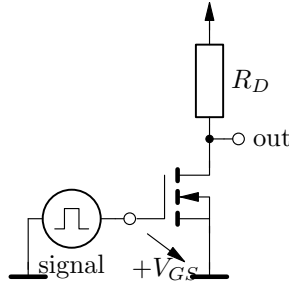
The sectional view of a NMOS transistor in silicon is being shown here also.

Both technologies, the older NMOS as the newer PMOS, have the same disadvantage. Every time, the transistor is switched on, the current between Drain and Source of the transistor is limited by the Resistor on Drain only. Higher currents here meaning higher power consumption for the chip where the transistors are integrated also. If the transistors are switched off, no currents flows between Drain and Source anymore, the power consumption of the chip also goes low.

Et violà, the US-Patent with Number 3356858[1]changed the world and combines both technologies to the new complementary metal-oxide-semiconductor

(CMOS) technology. Instead of every transistor is working against a weak resistor, the transistor works against a complementary switched-off transistor. With the Eyes of our antecessor CMOS doubles the transistor count, but contemporary chips all are build in CMOS.

Figure 3: complementary PMOS and NMOS transistor couple use-case
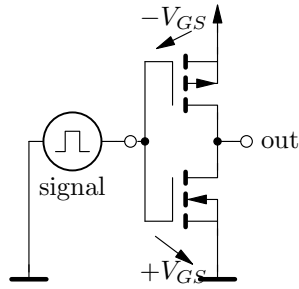
The sectional view of a NMOS and PMOS transistors couple in silicon - building the CMOS technology - are being shown here also.

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[1]https://www.google.com/patents/US3356858

0.2 Design Decisions

0.3   Cell Descriptions

Cell

AND4 - a 4-input AND gate

Synopsys

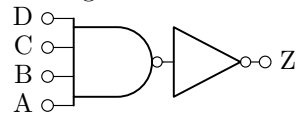AND4(Z, D, C, B, A)
AND4(Z, D, C, B, A, Vdd, Gnd)

Description

Figure 4: Circuit

Truth Table

Table 2: $Z = D \wedge C \wedge B \wedge A$

D	C	B	A	Z
0	X	X	X	0
X	0	X	X	0
X	X	0	X	0
X	X	X	0	0
1	1	1	1	1

Usage
Fan-in / Fan-out
Layout
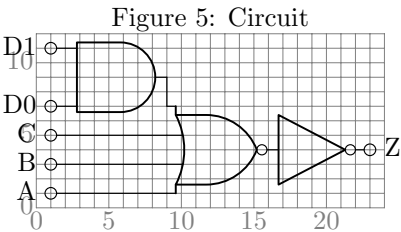Files

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Cell

AO2111 - a 2-1-1-1-input AND-OR gate

Synopsys

AO2111(Z, D1, D0, C, B, A)
AO2111(Z, D1, D0, C, B, A, Vdd, Gnd)

Description

Figure 5: Circuit

Truth Table

Table 3: $Z = (D1 \land D0) \lor C \lor B \lor A$

D1	D0	C	B	A	Z
0	X	0	0	0	0
0	X	1	X	X	1
0	X	X	1	X	1
0	X	X	X	1	1
X	0	0	0	0	0
X	0	1	X	X	1
X	0	X	1	X	1
X	0	X	X	1	1
1	1	X	X	X	1

Usage
Fan-in / Fan-out
Layout
Files
See also

AO3111 - a 3-1-1-1-input AND-OR gate [Page 7]
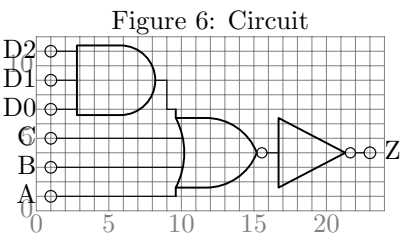
6

AO3111 - a 3-1-1-1-input AND-OR gate

Synopsys

    AO3111(Z, D2, D1, D0, C, B, A)
    AO3111(Z, D2, D1, D0, C, B, A, Vdd, Gnd)

Description

Figure 6: Circuit

Truth Table

Table 4: $Z = (D2 \wedge D1 \wedge D0) \vee C \vee B \vee A$

D2	D1	D0	C	B	A	Z
0	X	X	0	0	0	0
0	X	X	1	X	X	1
0	X	X	X	1	X	1
0	X	X	X	X	1	1
X	0	X	0	0	0	0
X	0	X	1	X	X	1
X	0	X	X	1	X	1
X	0	X	X	X	1	1
X	X	0	0	0	0	0
X	X	0	1	X	X	1
X	X	0	X	1	X	1
X	X	0	X	X	1	1
1	1	1	X	X	X	1

Usage
Fan-in / Fan-out
Layout
Files
See also

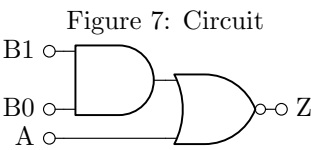   AO2111 - a 2-1-1-1-input AND-OR gate [Page 6]

AOI21 - a 2-1-input AND-OR-Invert gate

Synopsys

AOI21(Z, B1, B0, A)
AOI21(Z, B1, B0, A, Vdd, Gnd)

Description

Figure 7: Circuit

Truth Table

Table 5: $Z = \neg((B1 \wedge B0) \vee A)$

B1	B0	A	Z
0	X	0	1
1	1	X	0
X	0	0	1
X	X	1	0

Usage
Fan-in / Fan-out
Layout
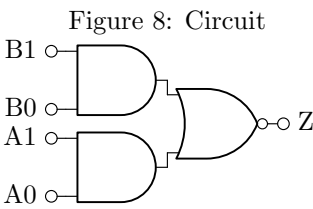Files
See also

AOI31 - a 3-1-input AND-OR-Invert gate [Page 10]

Cell

AOI22 - a 2-2-input AND-OR-Invert gate

Synopsys

AOI22(Z, B1, B0, A1, A0)
AOI22(Z, B1, B0, A1, A0, Vdd, Gnd)

Description

Figure 8: Circuit

B1 ○——
B0 ○——
A1 ○——
A0 ○—— ○ Z

Truth Table

Table 6: $Z = \neg((B1 \wedge B0) \vee (A1 \wedge A0))$

B1	B0	A1	A0	Z
0	X	0	X	1
0	X	X	0	1
1	1	X	X	0
X	0	0	X	1
X	0	X	0	1
X	X	1	1	0

Usage
Fan-in / Fan-out
Layout
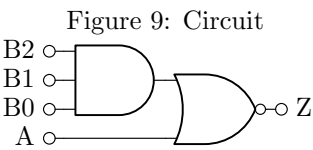Files
See also

AOI33 - a 3-3-input AND-OR-Invert gate [Page 12]

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AOI31 - a 3-1-input AND-OR-Invert gate

Synopsys

 AOI31(Z, B2, B1, B0, A)
 AOI31(Z, B2, B1, B0, A, Vdd, Gnd)

Description

Figure 9: Circuit

Truth Table

Table 7: $Z = \neg((B2 \wedge B1 \wedge B0) \vee A)$

B2	B1	B0	A	Z
0	X	X	0	1
1	1	1	X	0
X	0	X	0	1
X	X	0	0	1
X	X	X	1	0

Usage
Fan-in / Fan-out
Layout
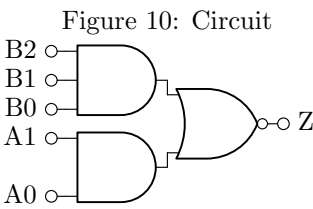Files
See also

 AOI21 - a 2-1-input AND-OR-Invert gate [Page 8]

CELL

AOI32 - a 3-2-input AND-OR-Invert gate

SYNOPSYS

AOI32(Z, B2, B1, B0, A1, A0)
AOI32(Z, B2, B1, B0, A1, A0, Vdd, Gnd)

DESCRIPTION

Figure 10: Circuit

B2 o—
B1 o—
B0 o—
A1 o—

A0 o—

Z

TRUTH TABLE

Table 8: $Z = \neg((B2 \wedge B1 \wedge B0) \vee (A1 \wedge A0))$

B2	B1	B0	A1	A0	Z
0	X	X	0	X	1
0	X	X	X	0	1
1	1	1	X	X	0
X	0	X	0	X	1
X	0	X	X	0	1
X	X	0	0	X	1
X	X	0	X	0	1
X	X	X	1	1	0

USAGE
FAN-IN / FAN-OUT
LAYOUT
FILES
SEE ALSO

AOI22 - a 2-2-input AND-OR-Invert gate [Page 9]
AOI33 - a 3-3-input AND-OR-Invert gate [Page 12]

AOI33 - a 3-3-input AND-OR-Invert gate

Synopsys

AOI33(Z, B2, B1, B0, A2, A1, A0)
AOI33(Z, B2, B1, B0, A2, A1, A0, Vdd, Gnd)

Description

Figure 11: Circuit

Truth Table

Table 9: $Z = \neg((B2 \wedge B1 \wedge B0) \vee (A2 \wedge A1 \wedge A0))$

B2	B1	B0	A2	A1	A0	Z
0	X	X	0	X	X	1
0	X	X	X	0	X	1
0	X	X	X	X	0	1
1	1	1	X	X	X	0
X	0	X	0	X	X	1
X	0	X	X	0	X	1
X	0	X	X	X	0	1
X	X	0	0	X	X	1
X	X	0	X	0	X	1
X	X	0	X	X	0	1
X	X	X	1	1	1	0

Usage
Fan-in / Fan-out
Layout
Files
See also

AOI22 - a 2-2-input AND-OR-Invert gate [Page 9]
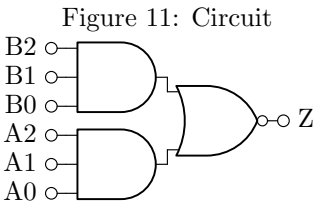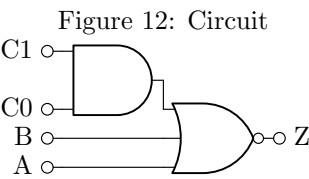AOI32 - a 3-2-input AND-OR-Invert gate [Page 11]

AOI211 - a 2-1-1-input AND-OR-Invert gate

Synopsys

AOI211(Z, C1, C0, B, A)
AOI211(Z, C1, C0, B, A, Vdd, Gnd)

Description

Figure 12: Circuit

Truth Table

Table 10: $Z = \neg((C1 \wedge C0) \vee B \vee A)$

C1	C0	B	A	Z
0	X	0	0	1
1	1	X	X	0
X	0	0	0	1
X	X	1	X	0
X	X	X	1	0

Usage
Fan-in / Fan-out
Layout
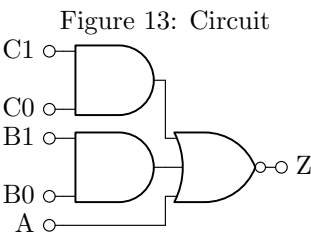Files
See also

AOI311 - a 3-1-1-input AND-OR-Invert gate [Page 16]

AOI221 - a 2-2-1-input AND-OR-Invert gate

Synopsys

AOI221(Z, C1, C0, B1, B0, A)
AOI221(Z, C1, C0, B1, B0, A, Vdd, Gnd)

Description

Figure 13: Circuit

C1 ○──
C0 ○──
B1 ○──
B0 ○──
A ○──

○ Z

Truth Table

Table 11: $Z = \neg((C1 \wedge C0) \vee (B1 \wedge B0) \vee A)$

C1	C0	B1	B0	A	Z
0	X	0	X	0	1
0	X	X	0	0	1
1	1	X	X	X	0
X	0	0	X	0	1
X	0	X	0	0	1
X	X	1	1	X	0
X	X	X	X	1	0

Usage
Fan-in / Fan-out
Layout
Files
See also

AOI321 - a 3-2-1-input AND-OR-Invert gate [Page 17]
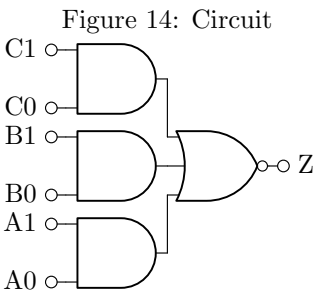AOI331 - a 3-3-1-input AND-OR-Invert gate [Page 20]

AOI222 - a 2-2-2-input AND-OR-Invert gate

Synopsys

AOI222(Z, C1, C0, B1, B0, A1, A0)
AOI222(Z, C1, C0, B1, B0, A1, A0, Vdd, Gnd)

Description

Figure 14: Circuit

Truth Table

Table 12: $Z = \neg((C1 \wedge C0) \vee (B1 \wedge B0) \vee (A1 \wedge A0))$

C1	C0	B1	B0	A1	A0	Z
0	X	0	X	0	X	1
0	X	0	X	X	0	1
0	X	X	0	0	X	1
0	X	X	0	X	0	1
1	1	X	X	X	X	0
X	0	0	X	0	X	1
X	0	0	X	X	0	1
X	0	X	0	0	X	1
X	0	X	0	X	0	1
X	X	1	1	X	X	0
X	X	X	X	1	1	0

Usage
Fan-in / Fan-out
Layout
Files
See also

AOI322 - a 3-2-2-input AND-OR-Invert gate [Page 18]
AOI332 - a 3-3-2-input AND-OR-Invert gate [Page 21]
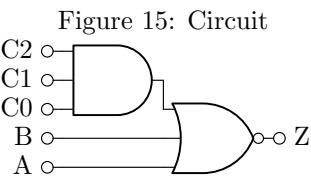AOI333 - a 3-3-3-input AND-OR-Invert gate [Page 23]

CELL

AOI311 - a 3-1-1-input AND-OR-Invert gate

SYNOPSYS

AOI311(Z, C2, C1, C0, B, A)
AOI311(Z, C2, C1, C0, B, A, Vdd, Gnd)

DESCRIPTION

Figure 15: Circuit

TRUTH TABLE

Table 13: $Z = \neg((C2 \wedge C1 \wedge C0) \vee B \vee A)$

C2	C1	C0	B	A	Z
0	X	X	0	0	1
1	1	1	X	X	0
X	0	X	0	0	1
X	X	0	0	0	1
X	X	X	1	X	0
X	X	X	X	1	0

USAGE
FAN-IN / FAN-OUT
LAYOUT
FILES
SEE ALSO
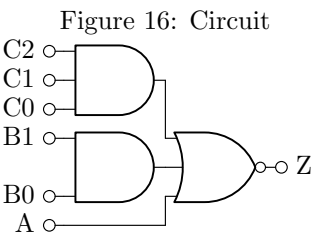
AOI211 - a 2-1-1-input AND-OR-Invert gate [Page 13]

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AOI321 - a 3-2-1-input AND-OR-Invert gate

SYNOPSYS

AOI321(Z, C2, C1, C0, B1, B0, A)
AOI321(Z, C2, C1, C0, B1, B0, A, Vdd, Gnd)

DESCRIPTION

Figure 16: Circuit

TRUTH TABLE

Table 14: $Z = \neg((C2 \wedge C1 \wedge C0) \vee (B1 \wedge B0) \vee A)$

C2	C1	C0	B1	B0	A	Z
0	X	X	0	X	0	1
0	X	X	X	0	0	1
1	1	1	X	X	X	0
X	0	X	0	X	0	1
X	0	X	X	0	0	1
X	X	0	0	X	0	1
X	X	0	X	0	0	1
X	X	X	1	1	X	0
X	X	X	X	X	1	0

USAGE
FAN-IN / FAN-OUT
LAYOUT
FILES
SEE ALSO

AOI311 - a 3-1-1-input AND-OR-Invert gate [Page 16]
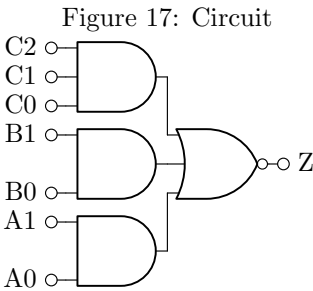AOI331 - a 3-3-1-input AND-OR-Invert gate [Page 20]

AOI322 - a 3-2-2-input AND-OR-Invert gate

Synopsys

AOI322(Z, C2, C1, C0, B1, B0, A1, A0)
AOI322(Z, C2, C1, C0, B1, B0, A1, A0, Vdd, Gnd)

Description

Figure 17: Circuit

Truth Table

Table 15: $Z = \neg((C2 \wedge C1 \wedge C0) \vee (B1 \wedge B0) \vee (A1 \wedge A0))$

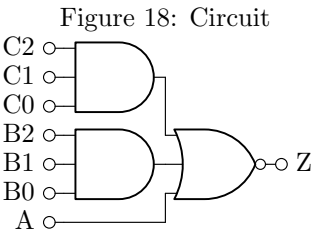| C2	C1	C0	B1	B0	A1	A0	Z
0	X	X	0	X	0	X	1
0	X	X	0	X	X	0	1
0	X	X	X	0	0	X	1
0	X	X	X	0	X	0	1
1	1	1	X	X	X	X	0
X	0	X	0	X	0	X	1
X	0	X	0	X	X	0	1
X	0	X	X	0	0	X	1
X	0	X	X	0	X	0	1
X	X	0	0	X	0	X	1
X	X	0	0	X	X	0	1
X	X	0	X	0	0	X	1
X	X	0	X	0	X	0	1
X	X	X	1	1	X	X	0
X	X	X	X	X	1	1	0

Usage
Fan-in / Fan-out
Layout
Files
See also

AOI331 - a 3-3-1-input AND-OR-Invert gate

Synopsys

AOI331(Z, C2, C1, C0, B2, B1, B0, A)
AOI331(Z, C2, C1, C0, B2, B1, B0, A, Vdd, Gnd)

Description

Figure 18: Circuit

Truth Table

Table 16: $Z = \neg((C2 \wedge C1 \wedge C0) \vee (B2 \wedge B1 \wedge B0) \vee A)$

C2	C1	C0	B2	B1	B0	A	Z
0	X	X	0	X	X	0	1
0	X	X	X	0	X	0	1
0	X	X	X	X	0	0	1
1	1	1	X	X	X	X	0
X	0	X	0	X	X	0	1
X	0	X	X	0	X	0	1
X	0	X	X	X	0	0	1
X	X	0	0	X	X	0	1
X	X	0	X	0	X	0	1
X	X	0	X	X	0	0	1
X	X	X	1	1	1	X	0
X	X	X	X	X	X	1	0

Usage
Fan-in / Fan-out
Layout
Files
See also

AOI221 - a 2-2-1-input AND-OR-Invert gate [Page 14]
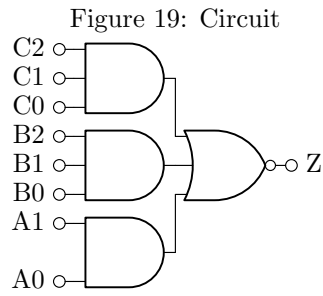AOI321 - a 3-2-1-input AND-OR-Invert gate [Page 17]

AOI332 - a 3-3-2-input AND-OR-Invert gate

Synopsys

AOI332(Z, C2, C1, C0, B2, B1, B0, A1, A0)
AOI332(Z, C2, C1, C0, B2, B1, B0, A1, A0, Vdd, Gnd)

Description

Figure 19: Circuit

Truth Table

Table 17: $Z = \neg((C2 \land C1 \land C0) \lor (B2 \land B1 \land B0) \lor (A1 \land A0))$

C2	C1	C0	B2	B1	B0	A1	A0	Z
0	X	X	0	X	X	0	X	1
0	X	X	0	X	X	X	0	1
0	X	X	X	0	X	0	X	1
0	X	X	X	0	X	X	0	1
0	X	X	X	X	0	0	X	1
0	X	X	X	X	0	X	0	1
1	1	1	X	X	X	X	X	0
X	0	X	0	X	X	0	X	1
X	0	X	0	X	X	X	0	1
X	0	X	X	0	X	0	X	1
X	0	X	X	0	X	X	0	1
X	0	X	X	X	0	0	X	1
X	0	X	X	X	0	X	0	1
X	X	0	0	X	X	0	X	1
X	X	0	0	X	X	X	0	1
X	X	0	X	0	X	0	X	1
X	X	0	X	0	X	X	0	1
X	X	0	X	X	0	0	X	1
X	X	0	X	X	0	X	0	1
X	X	X	1	1	1	X	X	0
X	X	X	X	X	X	1	1	0

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Usage
Fan-in / Fan-out
Layout
Files
See also

AOI222 - a 2-2-2-input AND-OR-Invert gate [Page 15]
AOI322 - a 3-2-2-input AND-OR-Invert gate [Page 18]
AOI333 - a 3-3-3-input AND-OR-Invert gate [Page 23]

AOI333 - a 3-3-3-input AND-OR-Invert gate

Synopsys

AOI333(Z, C2, C1, C0, B2, B1, B0, A2, A1, A0)
AOI333(Z, C2, C1, C0, B2, B1, B0, A2, A1, A0, Vdd, Gnd)

Description

Figure 20: Circuit

Truth Table

Usage
Fan-in / Fan-out
Layout
Files
See also

AOI222 - a 2-2-2-input AND-OR-Invert gate [Page 15]
AOI322 - a 3-2-2-input AND-OR-Invert gate [Page 18]
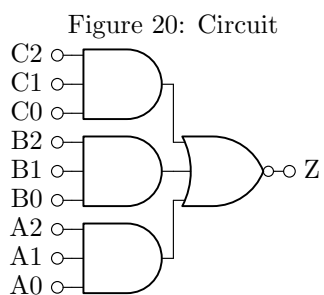AOI332 - a 3-3-2-input AND-OR-Invert gate [Page 21]

Table 18: $Z = \neg((C2 \wedge C1 \wedge C0) \vee (B2 \wedge B1 \wedge B0) \vee (A2 \wedge A1 \wedge A0))$

C2	C1	C0	B2	B1	B0	A2	A1	A0	Z
0	X	X	0	X	X	0	X	X	1
0	X	X	0	X	X	X	0	X	1
0	X	X	0	X	X	X	X	0	1
0	X	X	X	0	X	0	X	X	1
0	X	X	X	0	X	X	0	X	1
0	X	X	X	0	X	X	X	0	1
0	X	X	X	X	0	0	X	X	1
0	X	X	X	X	0	X	0	X	1
0	X	X	X	X	0	X	X	0	1
1	1	1	X	X	X	X	X	X	0
X	0	X	0	X	X	0	X	X	1
X	0	X	0	X	X	X	0	X	1
X	0	X	0	X	X	X	X	0	1
X	0	X	X	0	X	0	X	X	1
X	0	X	X	0	X	X	0	X	1
X	0	X	X	0	X	X	X	0	1
X	0	X	X	X	0	0	X	X	1
X	0	X	X	X	0	X	0	X	1
X	0	X	X	X	0	X	X	0	1
X	X	0	0	X	X	0	X	X	1
X	X	0	0	X	X	X	0	X	1
X	X	0	0	X	X	X	X	0	1
X	X	0	X	0	X	0	X	X	1
X	X	0	X	0	X	X	0	X	1
X	X	0	X	0	X	X	X	0	1
X	X	0	X	X	0	0	X	X	1
X	X	0	X	X	0	X	0	X	1
X	X	0	X	X	0	X	X	0	1
X	X	X	1	1	1	X	X	X	0
X	X	X	X	X	X	1	1	1	0

Cell

EQ2 - a 2-input Equality (or XNOR) gate

Synopsys

EQ2(Z, B, A)
EQ2(Z, B, A, Vdd, Gnd)

Description

Figure 21: Circuit

B o—
)o—o Z
A o—
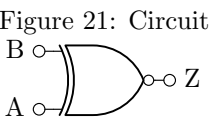
Truth Table

Table 19: $Z = \neg(B \oplus A)$

B	A	Z
0	0	1
0	1	0
1	0	0
1	1	1

Usage
Fan-in / Fan-out
Layout
Files
See also

XOR2 - a 2-input Exclusive-OR (or XOR) gate [Page 50]

NAND2 - a 2-input Not-AND (or NAND) gate

Synopsys

NAND2(Z, B, A)
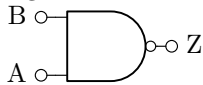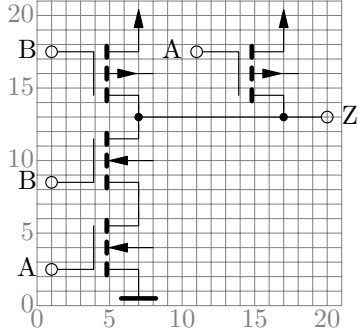NAND2(Z, B, A, Vdd, Gnd)

Description

Figure 22: Circuit

Figure 23: Schematic

Truth Table

Table 20: $Z = \neg(B \wedge A)$

B	A	Z
0	X	1
1	1	0
X	0	1

Usage
Fan-in / Fan-out
Layout
Files
See also

NAND3 - a 3-input Not-AND (or NAND) gate [Page 27]

NAND3 - a 3-input Not-AND (or NAND) gate

Synopsys

NAND3(Z, C, B, A)
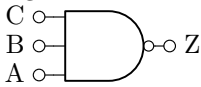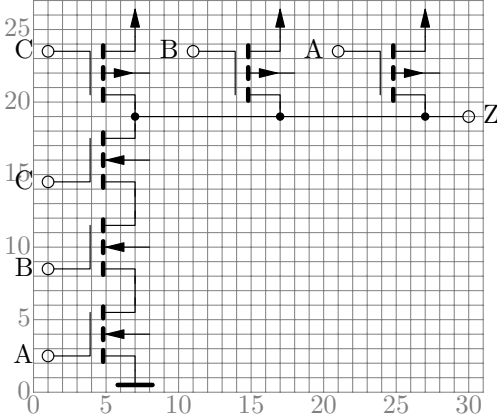NAND3(Z, C, B, A, Vdd, Gnd)

Description

Figure 24: Circuit

C ○
B ○ ⤵ ○ Z
A ○

Figure 25: Schematic

Truth Table

Table 21: $Z = \neg(C \wedge B \wedge A)$

C	B	A	Z
0	X	X	1
1	1	1	0
X	0	X	1
X	X	0	1

Usage
Fan-in / Fan-out
Layout
Files
See also

NAND2 - a 2-input Not-AND (or NAND) gate [Page 26]

27

NOR2 - a 2-input Not-OR (or NOR) gate

Synopsys

NOR2(Z, B, A)
NOR2(Z, B, A, Vdd, Gnd)

Description

Figure 26: Circuit

B ○⎯
⎯⎯⎯⎯⎯○ Z
A ○⎯

Truth Table

Table 22: $Z = \neg(B \vee A)$

B	A	Z
0	0	1
1	X	0
X	1	0

Usage
Fan-in / Fan-out
Layout
Files
See also

NOR3 - a 3-input Not-OR (or NOR) gate [Page 29]

28
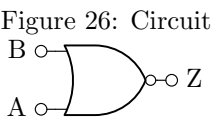
Cell

NOR3 - a 3-input Not-OR (or NOR) gate

Synopsys

NOR3(Z, C, B, A)
NOR3(Z, C, B, A, Vdd, Gnd)

Description

Figure 27: Circuit

Truth Table

Table 23: $Z = \neg(C \vee B \vee A)$

C	B	A	Z
0	0	0	1
1	X	X	0
X	1	X	0
X	X	1	0

Usage
Fan-in / Fan-out
Layout
Files
See also
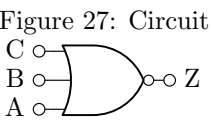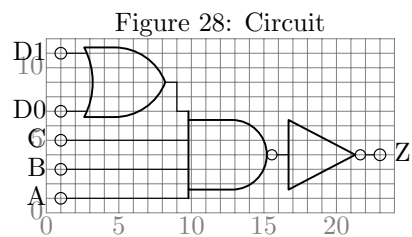
NOR2 - a 2-input Not-OR (or NOR) gate [Page 28]

CELL

OA2111 - a 2-1-1-1-input OR-AND gate

SYNOPSYS

OA2111(Z, D1, D0, C, B, A)
OA2111(Z, D1, D0, C, B, A, Vdd, Gnd)

DESCRIPTION

Figure 28: Circuit

TRUTH TABLE

Table 24: $Z = (D1 \lor D0) \land C \land B \land A$

D1	D0	C	B	A		Z
----	----	----	----	----		---
0	0	X	X	X		0
1	X	1	1	1		1
X	1	1	1	1		1
X	X	0	X	X		0
X	X	X	0	X		0
X	X	X	X	0		0

USAGE
FAN-IN / FAN-OUT
LAYOUT
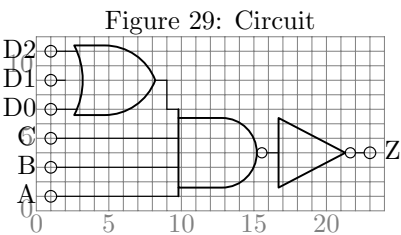FILES
SEE ALSO

OA3111 - a 3-1-1-1-input AND-OR gate [Page 31]

30

OA3111 - a 3-1-1-1-input OR-AND gate

SYNOPSYS

OA3111(Z, D2, D1, D0, C, B, A)
OA3111(Z, D2, D1, D0, C, B, A, Vdd, Gnd)

DESCRIPTION

Figure 29: Circuit

TRUTH TABLE

Table 25: $Z = (D2 \lor D1 \lor D0) \land C \land B \land A$

D2	D1	D0	C	B	A	Z
0	0	0	X	X	X	0
1	X	X	1	1	1	1
X	1	X	1	1	1	1
X	X	1	1	1	1	1
X	X	X	0	X	X	0
X	X	X	X	0	X	0
X	X	X	X	X	0	0

USAGE
FAN-IN / FAN-OUT
LAYOUT
FILES
SEE ALSO

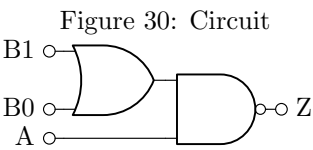OA2111 - a 2-1-1-1-input AND-OR gate [Page 30]

OAI21 - a 2-1-input OR-AND-Invert gate

Synopsys

OAI21(Z, B1, B0, A)
OAI21(Z, B1, B0, A, Vdd, Gnd)

Description

Figure 30: Circuit

Truth Table

Table 26: $Z = \neg((B1 \lor B0) \land A)$

B1	B0	A	Z
0	0	X	1
1	X	1	0
X	1	1	0
X	X	0	1

Usage
Fan-in / Fan-out
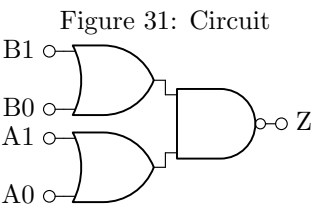Layout
Files
See also

OAI31 - a 3-1-input OR-AND-Invert gate [Page 34]

OAI22 - a 2-2-input OR-AND-Invert gate

Synopsys

OAI22(Z, B1, B0, A1, A0)
OAI22(Z, B1, B0, A1, A0, Vdd, Gnd)

Description

Figure 31: Circuit

B1 ○—
B0 ○—
A1 ○—
A0 ○—

Z

Truth Table

Table 27: $Z = \neg((B1 \vee B0) \wedge (A1 \vee A0))$

B1	B0	A1	A0	Z
0	0	X	X	1
1	X	1	X	0
1	X	X	1	0
X	1	1	X	0
X	1	X	1	0
X	X	0	0	1

Usage
Fan-in / Fan-out
Layout
Files
See also

OAI32 - a 3-2-input OR-AND-Invert gate [Page 35]
OAI33 - a 3-3-input OR-AND-Invert gate [Page 36]

OAI31 - a 3-1-input OR-AND-Invert gate

Synopsys

OAI31(Z, B2, B1, B0, A)
OAI31(Z, B2, B1, B0, A, Vdd, Gnd)

Description

Figure 32: Circuit

Truth Table

Table 28: $Z = \neg((B2 \vee B1 \vee B0) \wedge A)$

B2	B1	B0	A	Z
0	0	0	X	1
1	X	X	1	0
X	1	X	1	0
X	X	1	1	0
X	X	X	0	1

Usage
Fan-in / Fan-out
Layout
Files
See also

OAI21 - a 2-1-input OR-AND-Invert gate [Page 32]

34

OAI32 - a 3-2-input OR-AND-Invert gate

OAI32(Z, B2, B1, B0, A1, A0)
OAI32(Z, B2, B1, B0, A1, A0, Vdd, Gnd)

Description

Figure 33: Circuit

B2
B1
B0
A1

A0

Z

Truth Table

Table 29: $Z = \neg((B2 \vee B1 \vee B0) \wedge (A1 \vee A0))$

B2	B1	B0	A1	A0	Z
0	0	0	X	X	1
1	X	X	1	X	0
1	X	X	X	1	0
X	1	X	1	X	0
X	1	X	X	1	0
X	X	1	1	X	0
X	X	1	X	1	0
X	X	X	0	0	1

Usage
Fan-in / Fan-out
Layout
Files
See also

OAI22 - a 2-2-input OR-AND-Invert gate [Page 33]
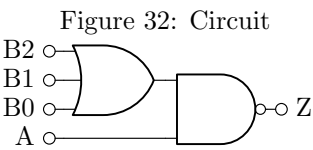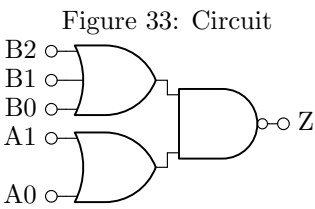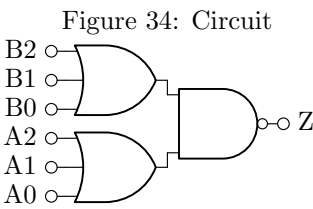OAI33 - a 3-3-input OR-AND-Invert gate [Page 36]

CELL

OAI33 - a 3-3-input OR-AND-Invert gate

SYNOPSYS

OAI33(Z, B2, B1, B0, A2, A1, A0)
OAI33(Z, B2, B1, B0, A2, A1, A0, Vdd, Gnd)

DESCRIPTION

Figure 34: Circuit

TRUTH TABLE

Table 30: $Z = \neg((B2 \lor B1 \lor B0) \land (A2 \lor A1 \lor A0))$

B2	B1	B0	A2	A1	A0	Z
0	0	0	X	X	X	1
1	X	X	1	X	X	0
1	X	X	X	1	X	0
1	X	X	X	X	1	0
X	1	X	1	X	X	0
X	1	X	X	1	X	0
X	1	X	X	X	1	0
X	X	1	1	X	X	0
X	X	1	X	1	X	0
X	X	1	X	X	1	0
X	X	X	0	0	0	1

USAGE
FAN-IN / FAN-OUT
LAYOUT
FILES
SEE ALSO

OAI22 - a 2-2-input OR-AND-Invert gate [Page 33]
OAI32 - a 3-2-input OR-AND-Invert gate [Page 35]

OAI211 - a 2-1-1-input OR-AND-Invert gate

Synopsys

OAI211(Z, C1, C0, B, A)
OAI211(Z, C1, C0, B, A, Vdd, Gnd)

Description

Figure 35: Circuit

C1 ∘—
C0 ∘—
B ∘—
A ∘—
∘ Z

Truth Table

Table 31: $Z = \neg((C1 \lor C0) \land B \land A)$

C1	C0	B	A	Z
0	0	X	X	1
1	X	1	1	0
X	1	1	1	0
X	X	0	X	1
X	X	X	0	1

Usage
Fan-in / Fan-out
Layout
Files
See also

OAI311 - a 3-1-1-input OR-AND-Invert gate [Page 40]

Cell

OAI221 - a 2-2-1-input OR-AND-Invert gate

Synopsys

OAI221(Z, C1, C0, B1, B0, A)
OAI221(Z, C1, C0, B1, B0, A, Vdd, Gnd)

Description

Figure 36: Circuit

Truth Table

Table 32: $Z = \neg((C1 \vee C0) \wedge (B1 \vee B0) \wedge A)$

C1	C0	B1	B0	A	Z
0	0	X	X	X	1
1	X	1	X	1	0
1	X	X	1	1	0
X	1	1	X	1	0
X	1	X	1	1	0
X	X	0	0	X	1
X	X	X	X	0	1

Usage
Fan-in / Fan-out
Layout
Files
See also

OAI321 - a 3-2-1-input OR-AND-Invert gate [Page 41]
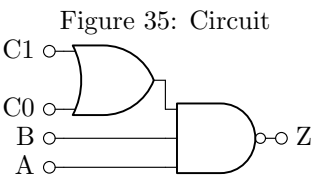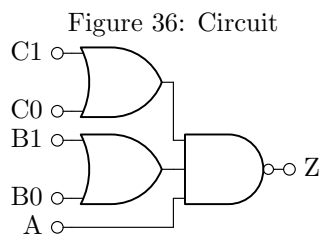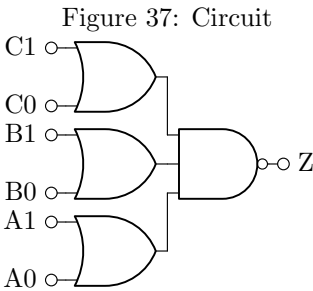OAI331 - a 3-3-1-input OR-AND-Invert gate [Page 44]

OAI222 - a 2-2-2-input OR-AND-Invert gate

Synopsys

OAI222(Z, C1, C0, B1, B0, A1, A0)
OAI222(Z, C1, C0, B1, B0, A1, A0, Vdd, Gnd)

Description

Figure 37: Circuit

Truth Table

Table 33: $Z = \neg((C1 \vee C0) \wedge (B1 \vee B0) \wedge (A1 \vee A0))$

C1	C0	B1	B0	A1	A0	Z
0	0	X	X	X	X	1
1	X	1	X	1	X	0
1	X	1	X	X	1	0
1	X	X	1	1	X	0
1	X	X	1	X	1	0
X	1	1	X	1	X	0
X	1	1	X	X	1	0
X	1	X	1	1	X	0
X	1	X	1	X	1	0
X	X	0	0	X	X	1
X	X	X	X	0	0	1

Usage
Fan-in / Fan-out
Layout
Files
See also

OAI322 - a 2-2-2-input OR-AND-Invert gate [Page 42]
OAI332 - a 3-3-2-input OR-AND-Invert gate [Page 45]
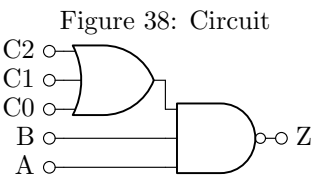OAI333 - a 3-3-3-input OR-AND-Invert gate [Page 47]

Cell

OAI311 - a 3-1-1-input OR-AND-Invert gate

Synopsys

OAI311(Z, C2, C1, C0, B, A)
OAI311(Z, C2, C1, C0, B, A, Vdd, Gnd)

Description

Figure 38: Circuit

Truth Table

Table 34: $Z = \neg((C2 \lor C1 \lor C0) \land B \land A)$

C2	C1	C0	B	A	Z
0	0	0	X	X	1
1	X	X	1	1	0
X	1	X	1	1	0
X	X	1	1	1	0
X	X	X	0	X	1
X	X	X	X	0	1

Usage
Fan-in / Fan-out
Layout
Files
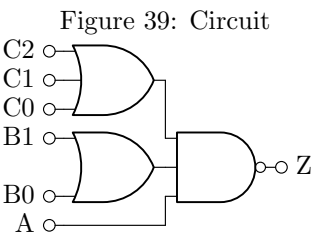See also

OAI211 - a 2-1-1-input OR-AND-Invert gate [Page 37]

OAI321 - a 3-2-1-input OR-AND-Invert gate

SYNOPSYS

OAI321(Z, C2, C1, C0, B1, B0, A)
OAI321(Z, C2, C1, C0, B1, B0, A, Vdd, Gnd)

DESCRIPTION

Figure 39: Circuit

TRUTH TABLE

Table 35: $Z = \neg((C2 \vee C1 \vee C0) \wedge (B1 \vee B0) \wedge A)$

C2	C1	C0	B1	B0	A	Z
0	0	0	X	X	X	1
1	X	X	1	X	1	0
1	X	X	X	1	1	0
X	1	X	1	X	1	0
X	1	X	X	1	1	0
X	X	1	1	X	1	0
X	X	1	X	1	1	0
X	X	X	0	0	X	1
X	X	X	X	X	0	1

USAGE
FAN-IN / FAN-OUT
LAYOUT
FILES
SEE ALSO

OAI221 - a 2-2-1-input OR-AND-Invert gate [Page 38]
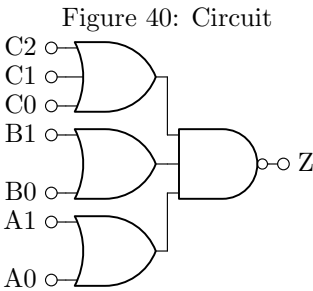OAI331 - a 3-3-1-input OR-AND-Invert gate [Page 44]

OAI322 - a 3-2-2-input OR-AND-Invert gate

Synopsys

OAI322(Z, C2, C1, C0, B1, B0, A1, A0)
OAI322(Z, C2, C1, C0, B1, B0, A1, A0, Vdd, Gnd)

Description

Figure 40: Circuit

Truth Table

Table 36: $Z = \neg((C2 \lor C1 \lor C0) \land (B1 \lor B0) \land (A1 \lor A0))$

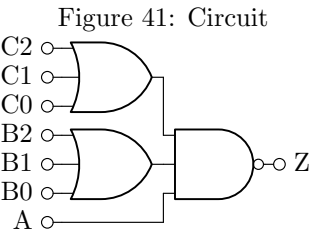| C2	C1	C0	B1	B0	A1	A0	Z
0	0	0	X	X	X	X	1
1	X	X	1	X	1	X	0
1	X	X	1	X	X	1	0
1	X	X	X	1	1	X	0
1	X	X	X	1	X	1	0
X	1	X	1	X	1	X	0
X	1	X	1	X	X	1	0
X	1	X	X	1	1	X	0
X	1	X	X	1	X	1	0
X	X	1	1	X	1	X	0
X	X	1	1	X	X	1	0
X	X	1	X	1	1	X	0
X	X	1	X	1	X	1	0
X	X	X	0	0	X	X	1
X	X	X	X	X	0	0	1

Usage
Fan-in / Fan-out
Layout
Files
See also

OAI331 - a 3-3-1-input OR-AND-Invert gate

Synopsys

OAI331(Z, C2, C1, C0, B2, B1, B0, A)
OAI331(Z, C2, C1, C0, B2, B1, B0, A, Vdd, Gnd)

Description

Figure 41: Circuit

Truth Table

Table 37: $Z = \neg((C2 \vee C1 \vee C0) \wedge (B2 \vee B1 \vee B0) \wedge A)$

C2	C1	C0	B2	B1	B0	A	Z
0	0	0	X	X	X	X	1
1	X	X	1	X	X	1	0
1	X	X	X	1	X	1	0
1	X	X	X	X	1	1	0
X	1	X	1	X	X	1	0
X	1	X	X	1	X	1	0
X	1	X	X	X	1	1	0
X	X	1	1	X	X	1	0
X	X	1	X	1	X	1	0
X	X	1	X	X	1	1	0
X	X	X	0	0	0	X	1
X	X	X	X	X	X	0	1

Usage
Fan-in / Fan-out
Layout
Files
See also

OAI221 - a 2-2-1-input OR-AND-Invert gate [Page 38]
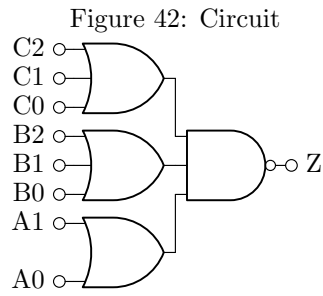OAI321 - a 3-2-1-input OR-AND-Invert gate [Page 41]

OAI332 - a 3-3-2-input OR-AND-Invert gate

Synopsys

OAI332(Z, C2, C1, C0, B2, B1, B0, A1, A0)
OAI332(Z, C2, C1, C0, B2, B1, B0, A1, A0, Vdd, Gnd)

Description

Figure 42: Circuit

Truth Table

Table 38: $Z = \neg((C2 \lor C1 \lor C0) \land (B2 \lor B1 \lor B0) \land (A1 \lor A0))$

C2	C1	C0	B2	B1	B0	A1	A0	Z
0	0	0	X	X	X	X	X	1
1	X	X	1	X	X	1	X	0
1	X	X	1	X	X	X	1	0
1	X	X	X	1	X	1	X	0
1	X	X	X	1	X	X	1	0
1	X	X	X	X	1	1	X	0
1	X	X	X	X	1	X	1	0
X	1	X	1	X	X	1	X	0
X	1	X	1	X	X	X	1	0
X	1	X	X	1	X	1	X	0
X	1	X	X	1	X	X	1	0
X	1	X	X	X	1	1	X	0
X	1	X	X	X	1	X	1	0
X	X	1	1	X	X	1	X	0
X	X	1	1	X	X	X	1	0
X	X	1	X	1	X	1	X	0
X	X	1	X	1	X	X	1	0
X	X	1	X	X	1	1	X	0
X	X	1	X	X	1	X	1	0
X	X	X	0	0	0	X	X	1
X	X	X	X	X	X	0	0	1

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USAGE
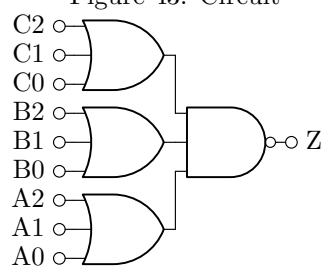FAN-IN / FAN-OUT
LAYOUT
FILES
SEE ALSO

OAI333 - a 3-3-3-input OR-AND-Invert gate

Synopsys

OAI333(Z, C2, C1, C0, B2, B1, B0, A2, A1, A0)
OAI333(Z, C2, C1, C0, B2, B1, B0, A2, A1, A0, Vdd, Gnd)

Description

Figure 43: Circuit

C2
C1
C0
B2
B1
B0
A2
A1
A0
Z

Truth Table

Usage
Fan-in / Fan-out
Layout
Files
See also

OAI222 - a 2-2-2-input OR-AND-Invert gate [Page 39]
OAI322 - a 3-2-2-input OR-AND-Invert gate [Page 42]
OAI332 - a 3-3-2-input OR-AND-Invert gate [Page 45]

Table 39: $Z = \neg((C2 \lor C1 \lor C0) \land (B2 \lor B1 \lor B0) \land (A2 \lor A1 \lor A0))$

| C2	C1	C0	B2	B1	B0	A2	A1	A0	Z
0	0	0	X	X	X	X	X	X	1
1	X	X	1	X	X	1	X	X	0
1	X	X	1	X	X	X	1	X	0
1	X	X	1	X	X	X	X	1	0
1	X	X	X	1	X	1	X	X	0
1	X	X	X	1	X	X	1	X	0
1	X	X	X	1	X	X	X	1	0
1	X	X	X	X	1	1	X	X	0
1	X	X	X	X	1	X	1	X	0
1	X	X	X	X	1	X	X	1	0
X	1	X	1	X	X	1	X	X	0
X	1	X	1	X	X	X	1	X	0
X	1	X	1	X	X	X	X	1	0
X	1	X	X	1	X	1	X	X	0
X	1	X	X	1	X	X	1	X	0
X	1	X	X	1	X	X	X	1	0
X	1	X	X	X	1	1	X	X	0
X	1	X	X	X	1	X	1	X	0
X	1	X	X	X	1	X	X	1	0
X	X	1	1	X	X	X	1	X	0
X	X	1	1	X	X	X	X	1	0
X	X	1	X	1	X	1	X	X	0
X	X	1	X	1	X	X	1	X	0
X	X	1	X	1	X	X	X	1	0
X	X	1	X	X	1	1	X	X	0
X	X	1	X	X	1	X	1	X	0
X	X	1	X	X	1	X	X	1	0
X	X	X	0	0	0	X	X	X	1
X	X	X	X	X	X	0	0	0	1

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OR4 - a 4-input OR gate

Synopsys

OR4(Z, D, C, B, A)
OR4(Z, D, C, B, A, Vdd, Gnd)

Description
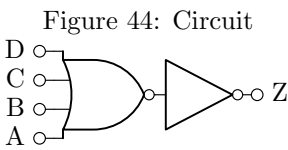
Figure 44: Circuit

Truth Table

Table 40: $Z = D \vee C \vee B \vee A$

D	C	B	A	Z
0	0	0	0	0
1	X	X	X	1
X	1	X	X	1
X	X	1	X	1
X	X	X	1	1

Usage
Fan-in / Fan-out
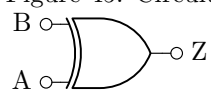Layout
Files

CELL

XOR2 - a 2-input Exclusive-OR (or XOR) gate

SYNOPSYS

XOR2(Z, B, A)
XOR2(Z, B, A, Vdd, Gnd)

DESCRIPTION

Figure 45: Circuit

TRUTH TABLE

Table 41: $Z = B \oplus A$

B	A	Z
0	0	0
0	1	1
1	0	1
1	1	0

USAGE
FAN-IN / FAN-OUT
LAYOUT
FILES
SEE ALSO

EQ2 - a 2-input Equality (or XNOR) gate [Page 25]