

# LibreSilicon's Standard Cell Library

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February 1, 2018

## Abstract

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For further clarification consult the complete documentation of the process.

Table 1: Document Revision History

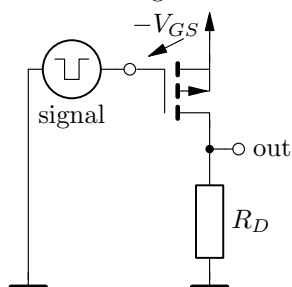
VERSION	DATE	DESCRIPTION	TRACKING NOTES
Draft 0.0	2018-01-30	START w/ empty document	-

# 1 CMOS in a nutshell

This basic initial project is dedicated to the CMOS Technology only and for this reason two types of metal-oxide-semiconductor field-effect transistors (MOSFET) are required.

Historically, the first chips with MOSFETs on the mass market were p-channel MOSFETs in enhancement-mode.

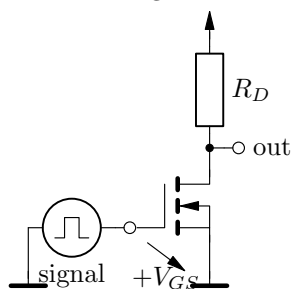
Figure 1: enhancement-mode PMOS transistor use-case



The sectional view of a PMOS transistor in silicon is being shown below

Historically later, faster chips with MOSFETs on the mass market were marked as n-channel MOSFETs in enhancement mode also.

Figure 2: enhancement-mode NMOS transistor use-case



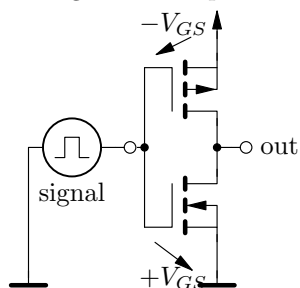
The sectional view of a NMOS transistor in silicon is being shown here also.

Both technologies, the older NMOS as the newer PMOS, have the same disadvantage. Every time, the transistor is switched on, the current between Drain and Source of the transistor is limited by the Resistor on Drain only. Higher currents here meaning higher power consumption for the chip where the transistors are integrated also. If the transistors are switched off, no currents flows between Drain and Source anymore, the power consumption of the chip also goes low.

Et voilà, the US-Patent with Number 3356858<sup>1</sup> changed the world and combines both technologies to the new complementary metal-oxide-semiconductor

(CMOS) technology. Instead of every transistor is working against a weak resistor, the transistor works against a complementary switched-off transistor. With the Eyes of our antecessor CMOS doubles the transistor count, but contemporary chips all are build in CMOS.

Figure 3: complementary PMOS and NMOS transistor couple use-case



The sectional view of a NMOS and PMOS transistors couple in silicon - building the CMOS technology - are being shown here also.

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<sup>1</sup><https://www.google.com/patents/US3356858>

**2 Design Decisions**

**3 Cell Descriptions**

CELL

**NAND2** - a 2-input NAND

SYNOPSIS

NAND2(Z, B, A)  
NAND2(Z, B, A, Vdd, Gnd)

DESCRIPTION

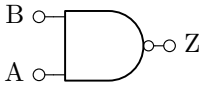


Figure 4: Circuit

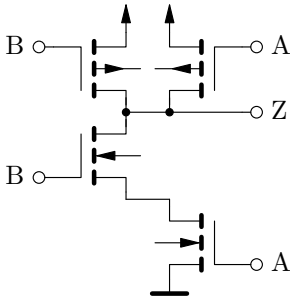


Figure 5: Schematic

TRUTH TABLE

B	A	Z
0	0	1
0	1	1
1	0	1
1	1	0

Table 2:  $Z = \neg(A \wedge B)$

USAGE

FAN-IN / FAN-OUT

LAYOUT

FILES

SEE ALSO

NAND3 - 3-input NAND