

LibreSilicon's Standard Cell Library

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Abstract

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For further clarification consult the complete documentation of the process.

Document Revision History

VERSION	DATE	DESCRIPTION	TRACKING NOTES
Draft 0.0	2018-02-01	START with empty document, ADD many cells	-

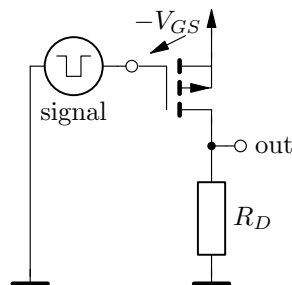
Chapter 1

CMOS in a nutshell

This basic initial project is dedicated to the CMOS Technology only and for this reason two types of metal-oxide-semiconductor field-effect transistors (MOSFET) are required.

Historically, the first chips with MOSFETs on the mass market were p-channel MOSFETs in enhancement-mode.

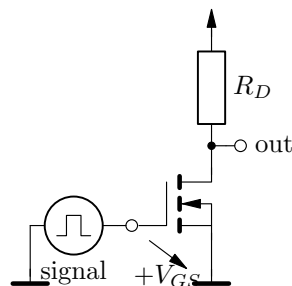
enhancement-mode PMOS transistor use-case



The sectional view of a PMOS transistor in silicon is being shown below

Historically later, faster chips with MOSFETs on the mass market were marked as n-channel MOSFETs in enhancement mode also.

enhancement-mode NMOS transistor use-case



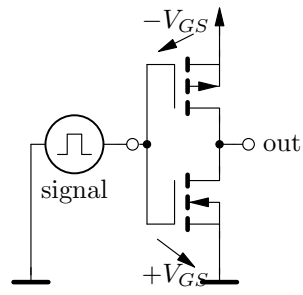
The sectional view of a NMOS transistor in silicon is being shown here also.

Both technologies, the older NMOS as the newer PMOS, have the same disadvantage. Every time, the transistor is switched on, the current between Drain and Source of the transistor is limited by the Resistor on Drain only. Higher currents here meaning higher power consumption for the chip where the transistors are integrated also. If the transistors are switched off, no currents flows between Drain and Source anymore, the power consumption of the chip also goes low.

Et voilà, the US-Patent with Number 3356858¹ changed the world and combines both technologies to the new complementary metal-oxide-semiconductor (CMOS) technology. Instead of every transistor is working against a weak resistor, the transistor works against a complementary switched-off transistor. With the Eyes of our antecessor CMOS doubles the transistor count, but contemporary chips all are build in CMOS.

complementary PMOS and NMOS transistor couple use-case

¹<https://www.google.com/patents/US3356858>



The sectional view of a NMOS and PMOS transistors couple in silicon - building the CMOS technology - are being shown here also.

Chapter 2

Considerations

Chapter 3

Logical Cells

3.1 AND4

Cell

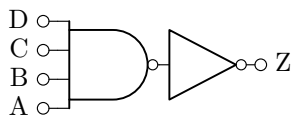
AND4 - a 4-input AND gate

Synopsys

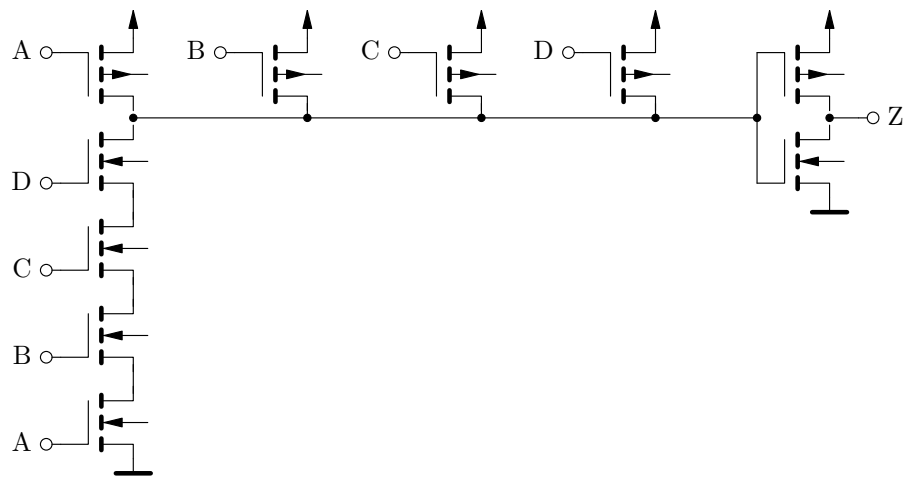
AND4(Z, D, C, B, A)

Description

Circuit



Schematic (two stages, $1T_p/4T_n$ stacked, 10T total)



Truth Table

$$Z = D \wedge C \wedge B \wedge A$$

D	C	B	A	Z
0	X	X	X	0
X	0	X	X	0
X	X	0	X	0
X	X	X	0	0
1	1	1	1	1

Usage

Fan-in / Fan-out

Layout

Files

See also

OR4 - a 4-input OR gate

3.2 AO2111

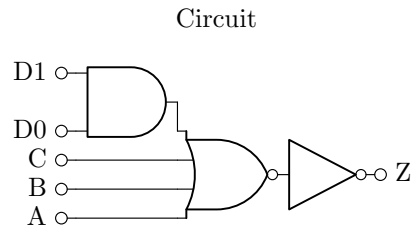
Cell

AO2111 - a 2-1-1-1-input AND-OR gate

Synopsys

AO2111(Z, D1, D0, C, B, A)

Description



Truth Table

$$Z = (D1 \wedge D0) \vee C \vee B \vee A$$

D1	D0	C	B	A	Z
0	X	0	0	0	0
0	X	1	X	X	1
0	X	X	1	X	1
0	X	X	X	1	1
X	0	0	0	0	0
X	0	1	X	X	1
X	0	X	1	X	1
X	0	X	X	1	1
1	1	X	X	X	1

Usage

Fan-in / Fan-out

Layout

Files

See also

AO3111 - a 3-1-1-1-input AND-OR gate

3.3 AO3111

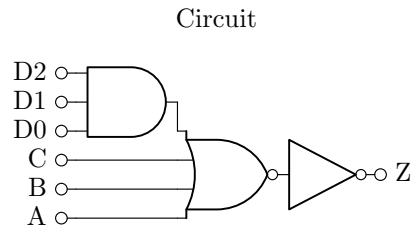
Cell

AO3111 - a 3-1-1-1-input AND-OR gate

Synopsys

AO3111(Z, D2, D1, D0, C, B, A)

Description



Truth Table

$Z = (D2 \wedge D1 \wedge D0) \vee C \vee B \vee A$

D2	D1	D0	C	B	A	Z
0	X	X	0	0	0	0
0	X	X	1	X	X	1
0	X	X	X	1	X	1
0	X	X	X	X	1	1
X	0	X	0	0	0	0
X	0	X	1	X	X	1
X	0	X	X	1	X	1
X	0	X	X	X	1	1
X	X	0	0	0	0	0
X	X	0	1	X	X	1
X	X	0	X	1	X	1
X	X	0	X	X	1	1
1	1	1	X	X	X	1

Usage

Fan-in / Fan-out

Layout

Files

See also

AO2111 - a 2-1-1-1-input AND-OR gate

3.4 AOI21

Cell

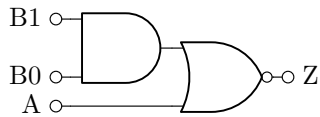
AOI21 - a 2-1-input AND-OR-Invert gate

Synopsys

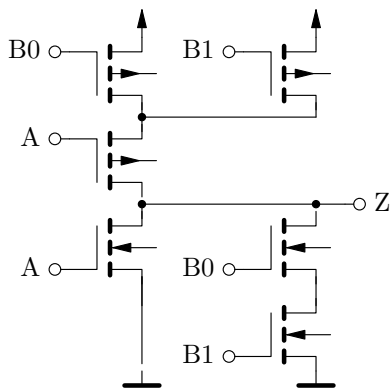
AOI21(Z, B1, B0, A)

Description

Circuit



Schematic (one stage, $2T_p/2T_n$ stacked, 6T total)



Truth Table

$$Z = \neg((B1 \wedge B0) \vee A)$$

B1	B0	A	Z
0	X	0	1
1	1	X	0
X	0	0	1
X	X	1	0

Usage

Fan-in / Fan-out

Layout

Files

See also

AOI31 - a 3-1-input AND-OR-Invert gate

3.5 AOI22

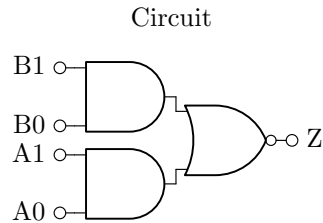
Cell

AOI22 - a 2-2-input AND-OR-Invert gate

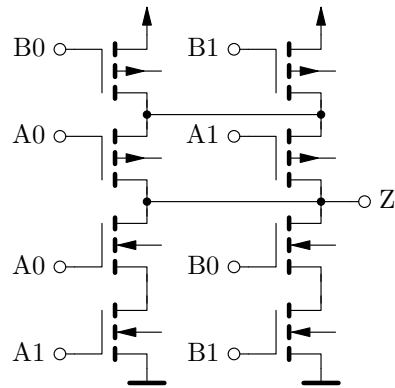
Synopsys

AOI22(Z, B1, B0, A1, A0)

Description



Schematic (one stage, $2T_p/2T_n$ stacked, 8T total)



Truth Table

$$Z = \neg((B1 \wedge B0) \vee (A1 \wedge A0))$$

B1	B0	A1	A0	Z
0	X	0	X	1
0	X	X	0	1
1	1	X	X	0
X	0	0	X	1
X	0	X	0	1
X	X	1	1	0

Usage

Fan-in / Fan-out

Layout

Files

See also

AOI33 - a 3-3-input AND-OR-Invert gate

3.6 AOI31

Cell

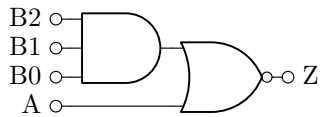
AOI31 - a 3-1-input AND-OR-Invert gate

Synopsys

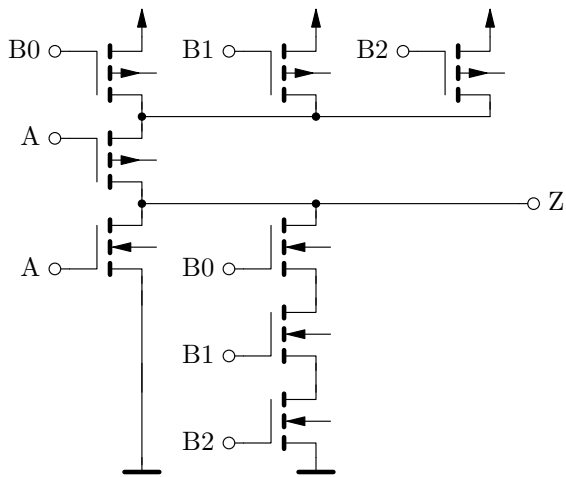
AOI31(Z, B2, B1, B0, A)

Description

Circuit



Schematic (one stage, $2T_p/3T_n$ stacked, 8T total)



Truth Table

$$Z = \neg((B2 \wedge B1 \wedge B0) \vee A)$$

B2	B1	B0	A	Z
0	X	X	0	1
1	1	1	X	0
X	0	X	0	1
X	X	0	0	1
X	X	X	1	0

Usage

Fan-in / Fan-out

Layout

Files

See also

AOI21 - a 2-1-input AND-OR-Invert gate

3.7 AOI32

Cell

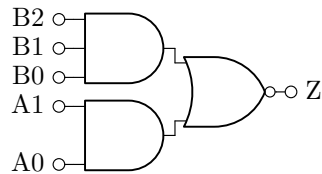
AOI32 - a 3-2-input AND-OR-Invert gate

Synopsys

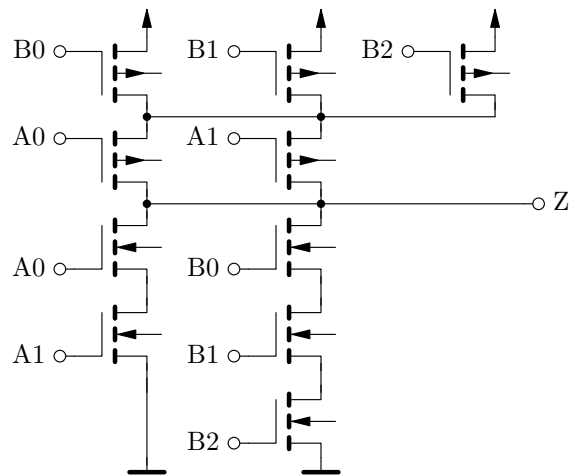
AOI32(Z, B2, B1, B0, A1, A0)

Description

Circuit



Schematic (one stage, $2T_p/3T_n$ stacked, 10T total)



Truth Table

$$Z = \neg((B2 \wedge B1 \wedge B0) \vee (A1 \wedge A0))$$

B2	B1	B0	A1	A0	Z
0	X	X	0	X	1
0	X	X	X	0	1
1	1	1	X	X	0
X	0	X	0	X	1
X	0	X	X	0	1
X	X	0	0	X	1
X	X	0	X	0	1
X	X	X	1	1	0

Usage

Fan-in / Fan-out

Layout

Files

See also

- AOI22 - a 2-2-input AND-OR-Invert gate
- AOI33 - a 3-3-input AND-OR-Invert gate

3.8 AOI33

Cell

AOI33 - a 3-3-input AND-OR-Invert gate

Synopsys

AOI33(Z, B2, B1, B0, A2, A1, A0)

Description

Fan-in / Fan-out

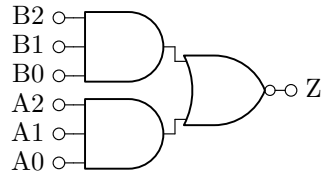
Layout

Files

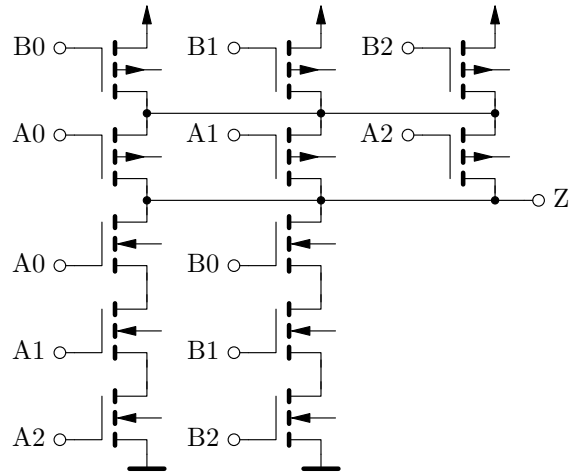
See also

AOI22 - a 2-2-input AND-OR-Invert gate
AOI32 - a 3-2-input AND-OR-Invert gate

Circuit



Schematic (one stage, $2T_p/3T_n$ stacked, 12T total)



Truth Table

$$Z = \neg((B2 \wedge B1 \wedge B0) \vee (A2 \wedge A1 \wedge A0))$$

B2	B1	B0	A2	A1	A0	Z
0	X	X	0	X	X	1
0	X	X	X	0	X	1
0	X	X	X	X	0	1
1	1	1	X	X	X	0
X	0	X	0	X	X	1
X	0	X	X	0	X	1
X	0	X	X	X	0	1
X	X	0	0	X	X	1
X	X	0	X	0	X	1
X	X	0	X	X	0	1
X	X	X	1	1	1	0

Usage

3.9 AOI211

Cell

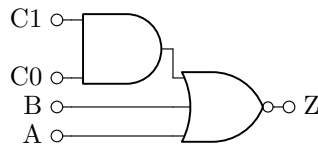
AOI211 - a 2-1-1-input AND-OR-Invert gate

Synopsys

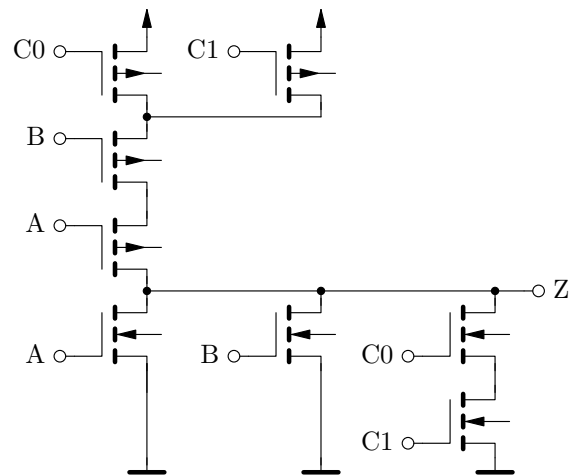
AOI211(Z, C1, C0, B, A)

Description

Circuit



Schematic (one stage, $3T_p/2T_n$ stacked, 8T total)



Truth Table

$$Z = \neg((C1 \wedge C0) \vee B \vee A)$$

C1	C0	B	A	Z
0	X	0	0	1
1	1	X	X	0
X	0	0	0	1
X	X	1	X	0
X	X	X	1	0

Usage

Fan-in / Fan-out

Layout

Files

See also

AOI311 - a 3-1-1-input AND-OR-Invert gate

3.10 AOI221

Cell

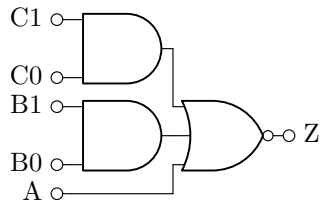
AOI221 - a 2-2-1-input AND-OR-Invert gate

Synopsys

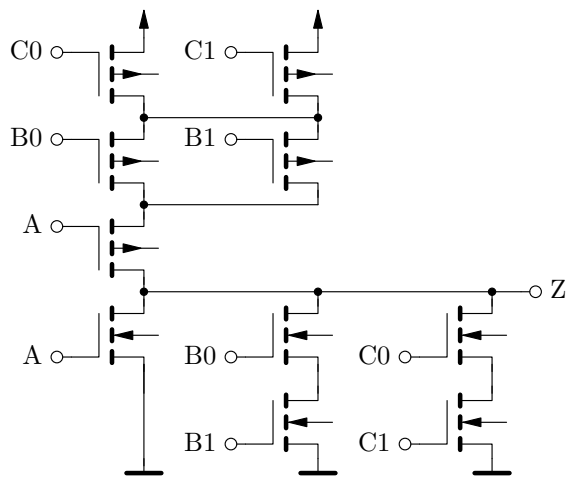
AOI221(Z, C1, C0, B1, B0, A)

Description

Circuit



Schematic (one stage, $3T_p/2T_n$ stacked, 10T total)



Truth Table

$$Z = \neg((C1 \wedge C0) \vee (B1 \wedge B0) \vee A)$$

C1	C0	B1	B0	A	Z
0	X	0	X	0	1
0	X	X	0	0	1
1	1	X	X	X	0
X	0	0	X	0	1
X	0	X	0	0	1
X	X	1	1	X	0
X	X	X	X	1	0

Usage

Fan-in / Fan-out

Layout

Files

See also

AOI321 - a 3-2-1-input AND-OR-Invert gate
AOI331 - a 3-3-1-input AND-OR-Invert gate

3.11 AOI222

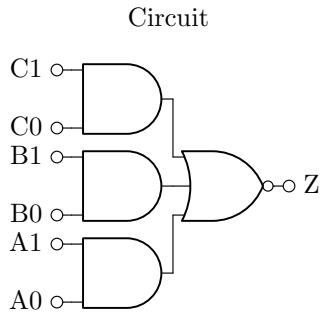
Cell

AOI222 - a 2-2-2-input AND-OR-Invert gate

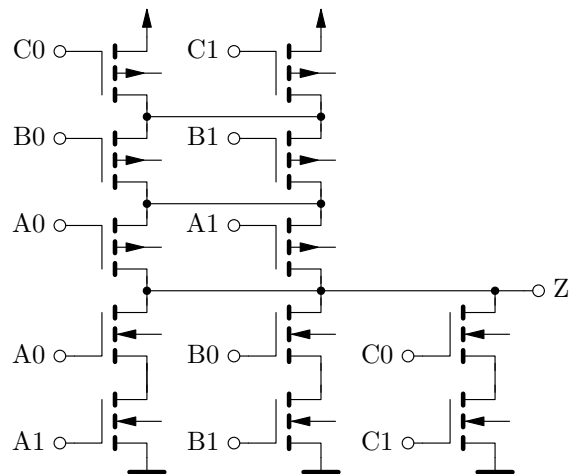
Synopsys

AOI222(Z, C1, C0, B1, B0, A1, A0)

Description



Schematic (one stage, $3T_p/2T_n$ stacked, 12T total)



C1	C0	B1	B0	A1	A0	Z
0	X	0	X	0	X	1
0	X	0	X	X	0	1
0	X	X	0	0	X	1
0	X	X	0	X	0	1
1	1	X	X	X	X	0
X	0	0	X	0	X	1
X	0	0	X	X	0	1
X	0	X	0	0	X	1
X	0	X	0	X	0	1
X	X	1	1	X	X	0
X	X	X	X	1	1	0

Truth Table

$$Z = \neg((C1 \wedge C0) \vee (B1 \wedge B0) \vee (A1 \wedge A0))$$

Usage

Fan-in / Fan-out

Layout

Files

See also

- AOI322 - a 3-2-2-input AND-OR-Invert gate
- AOI332 - a 3-3-2-input AND-OR-Invert gate
- AOI333 - a 3-3-3-input AND-OR-Invert gate

3.12 AOI311

Cell

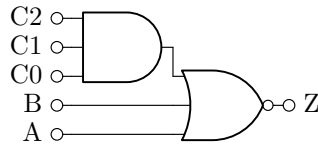
AOI311 - a 3-1-1-input AND-OR-Invert gate

Synopsys

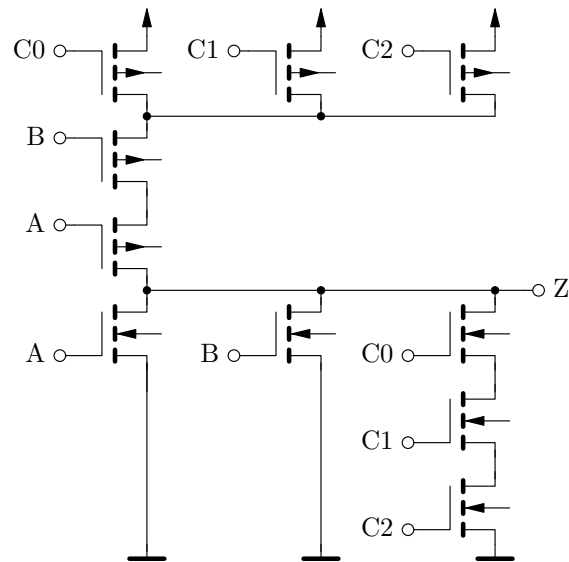
AOI311(Z, C2, C1, C0, B, A)

Description

Circuit



Schematic (one stage, $3T_p/3T_n$ stacked, 10T total)



Truth Table

$$Z = \neg((C2 \wedge C1 \wedge C0) \vee B \vee A)$$

C2	C1	C0	B	A	Z
0	X	X	0	0	1
1	1	1	X	X	0
X	0	X	0	0	1
X	X	0	0	0	1
X	X	X	1	X	0
X	X	X	X	1	0

Usage

Fan-in / Fan-out

Layout

Files

See also

AOI211 - a 2-1-1-input AND-OR-Invert gate

3.13 AOI321

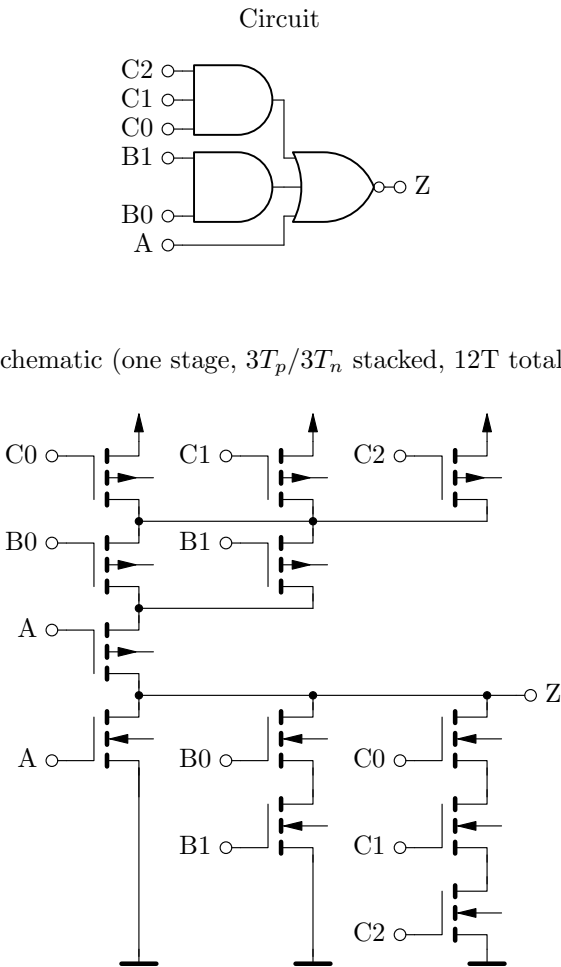
Cell

AOI321 - a 3-2-1-input AND-OR-Invert gate

Synopsys

AOI321(Z, C2, C1, C0, B1, B0, A)

Description



C2	C1	C0	B1	B0	A	Z
0	X	X	0	X	0	1
0	X	X	X	0	0	1
1	1	1	X	X	X	0
X	0	X	0	X	0	1
X	0	X	X	0	0	1
X	X	0	0	X	0	1
X	X	0	X	0	0	1
X	X	X	1	1	X	0
X	X	X	X	X	1	0

Truth Table

$$Z = \neg((C2 \wedge C1 \wedge C0) \vee (B1 \wedge B0) \vee A)$$

Usage

Fan-in / Fan-out

Layout

Files

See also

- AOI311 - a 3-1-1-input AND-OR-Invert gate
- AOI331 - a 3-3-1-input AND-OR-Invert gate

3.14 AOI322

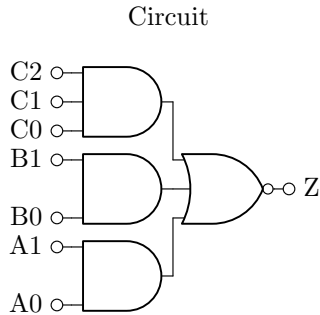
Cell

AOI322 - a 3-2-2-input AND-OR-Invert gate

Synopsys

AOI322(Z, C2, C1, C0, B1, B0, A1, A0)

Description

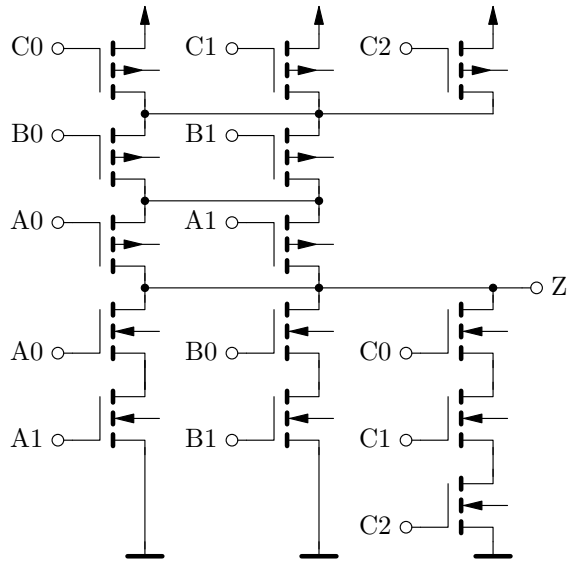


C2	C1	C0	B1	B0	A1	A0	Z
0	X	X	0	X	0	X	1
0	X	X	0	X	X	0	1
0	X	X	X	0	0	X	1
0	X	X	X	0	X	0	1
1	1	1	X	X	X	X	0
X	0	X	0	X	0	X	1
X	0	X	0	X	X	0	1
X	0	X	X	0	0	X	1
X	0	X	X	0	X	0	1
X	X	0	0	X	0	X	1
X	X	0	0	X	X	0	1
X	X	0	X	0	0	X	1
X	X	0	X	0	X	0	1
X	X	X	1	1	X	X	0
X	X	X	X	X	1	1	0

See also

- AOI222 - a 2-2-2-input AND-OR-Invert gate
- AOI332 - a 3-2-2-input AND-OR-Invert gate
- AOI333 - a 3-3-3-input AND-OR-Invert gate

Schematic (one stage, $3T_p/3T_n$ stacked, 14T total)



Truth Table

$$Z = \neg((C2 \wedge C1 \wedge C0) \vee (B1 \wedge B0) \vee (A1 \wedge A0))$$

Usage

Fan-in / Fan-out

Layout

Files

3.15 AOI331

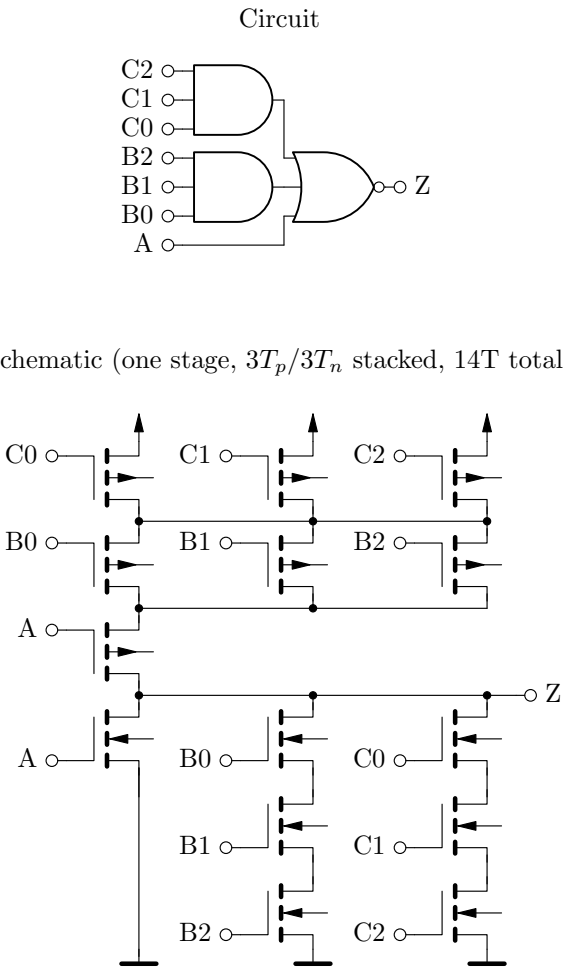
Cell

AOI331 - a 3-3-1-input AND-OR-Invert gate

Synopsys

AOI331(Z, C2, C1, C0, B2, B1, B0, A)

Description



C2	C1	C0	B2	B1	B0	A	Z
0	X	X	0	X	X	0	1
0	X	X	X	0	X	0	1
0	X	X	X	X	0	0	1
1	1	1	X	X	X	X	0
X	0	X	0	X	X	0	1
X	0	X	X	0	X	0	1
X	0	X	X	X	0	0	1
X	X	0	0	X	X	0	1
X	X	0	X	0	X	0	1
X	X	0	X	X	0	0	1
X	X	X	1	1	1	X	0
X	X	X	X	X	X	1	0

Truth Table

$$Z = \neg((C2 \wedge C1 \wedge C0) \vee (B2 \wedge B1 \wedge B0) \vee A)$$

Usage

Fan-in / Fan-out

Layout

Files

See also

- AOI221 - a 2-2-1-input AND-OR-Invert gate
- AOI321 - a 3-2-1-input AND-OR-Invert gate

3.16 AOI332

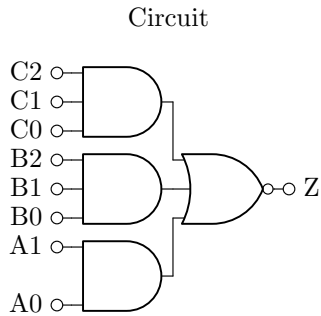
Cell

AOI332 - a 3-3-2-input AND-OR-Invert gate

Synopsis

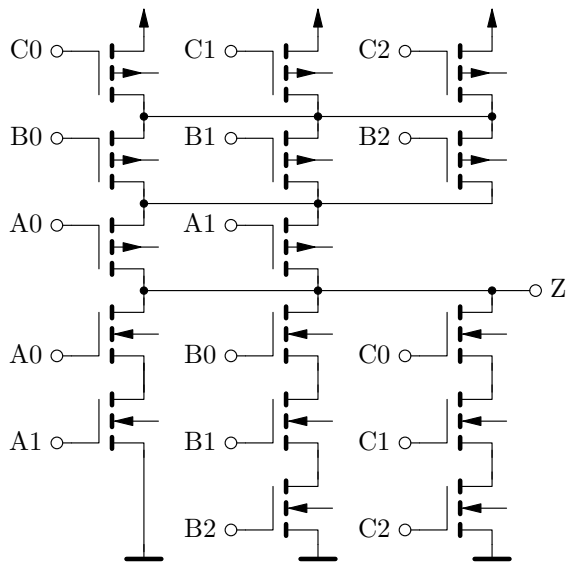
AOI332(Z, C2, C1, C0, B2, B1, B0, A1, A0)

Description



C2	C1	C0	B2	B1	B0	A1	A0	Z
0	X	X	0	X	X	0	X	1
0	X	X	0	X	X	X	0	1
0	X	X	X	0	X	0	X	1
0	X	X	X	0	X	X	0	1
0	X	X	X	X	0	0	X	1
0	X	X	X	X	0	X	0	1
1	1	1	X	X	X	X	X	0
X	0	X	0	X	X	0	X	1
X	0	X	0	X	X	X	0	1
X	0	X	X	0	X	0	X	1
X	0	X	X	0	X	X	0	1
X	0	X	X	X	0	0	X	1
X	0	X	X	X	0	X	0	1
X	X	0	0	X	X	0	X	1
X	X	0	0	X	X	X	0	1
X	X	0	X	0	X	0	X	1
X	X	0	X	0	X	X	0	1
X	X	0	X	X	0	0	X	1
X	X	0	X	X	0	X	0	1
X	X	X	1	1	1	X	X	0
X	X	X	X	X	X	1	1	0

Schematic (one stage, $3T_p/3T_n$ stacked, 16T total)



Truth Table

$$Z = \neg((C2 \wedge C1 \wedge C0) \vee (B2 \wedge B1 \wedge B0) \vee (A1 \wedge A0))$$

Usage

Fan-in / Fan-out

Layout

Files

See also

AOI222 - a 2-2-2-input AND-OR-Invert gate

AOI322 - a 3-2-2-input AND-OR-Invert gate

AOI333 - a 3-3-3-input AND-OR-Invert gate

3.17 AOI333

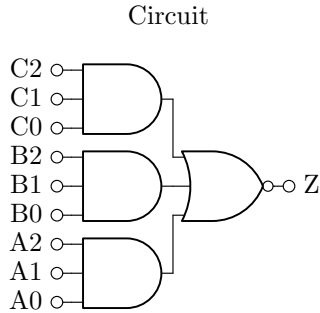
Cell

AOI333 - a 3-3-3-input AND-OR-Invert gate

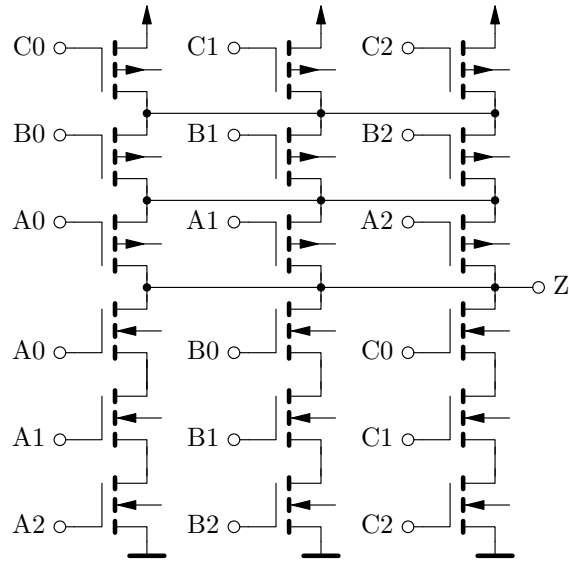
Synopsys

AOI333(Z, C2, C1, C0, B2, B1, B0, A2, A1, A0)

Description



Schematic (one stage, $3T_p/3T_n$ stacked, 18T total)



Truth Table

$$Z = \neg((C2 \wedge C1 \wedge C0) \vee (B2 \wedge B1 \wedge B0) \vee (A2 \wedge A1 \wedge A0))$$

Usage

Fan-in / Fan-out

Layout

Files

C2	C1	C0	B2	B1	B0	A2	A1	A0	Z
0	X	X	0	X	X	0	X	X	1
0	X	X	0	X	X	X	0	X	1
0	X	X	0	X	X	X	X	0	1
0	X	X	X	0	X	0	X	X	1
0	X	X	X	0	X	X	0	X	1
0	X	X	X	0	X	X	X	0	1
0	X	X	X	X	0	0	X	X	1
0	X	X	X	X	0	X	0	X	1
0	X	X	X	X	0	X	X	0	1
1	1	1	X	X	X	X	X	X	0
X	0	X	0	X	X	0	X	X	1
X	0	X	0	X	X	X	0	X	1
X	0	X	0	X	X	X	X	0	1
X	0	X	X	0	X	0	X	X	1
X	0	X	X	0	X	X	0	X	1
X	0	X	X	0	X	X	X	0	1
X	0	X	X	X	0	0	X	X	1
X	0	X	X	X	0	X	0	X	1
X	0	X	X	X	0	X	X	0	1
X	X	0	0	X	X	0	X	X	1
X	X	0	0	X	X	X	0	X	1
X	X	0	0	X	X	X	X	0	1
X	X	0	X	0	X	0	X	X	1
X	X	0	X	0	X	X	0	X	1
X	X	0	X	X	0	0	X	X	1
X	X	0	X	X	0	X	0	X	1
X	X	0	X	X	0	X	X	0	1
X	X	X	1	1	1	X	X	X	0
X	X	X	X	X	X	1	1	1	0

See also

- AOI222 - a 2-2-2-input AND-OR-Invert gate
- AOI322 - a 3-2-2-input AND-OR-Invert gate
- AOI332 - a 3-3-2-input AND-OR-Invert gate

3.18 BUF

Cell

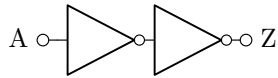
BUF - a Buffer gate

Synopsys

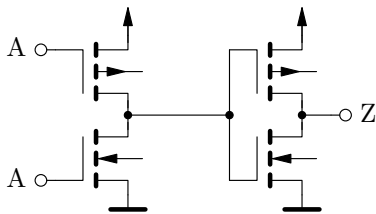
BUF(Z, A)

Description

Circuit



Schematic (two stages, $1T_p/1T_n$ stacked, 4T total)



Truth Table

$$Z = A$$

A	Z
0	0
1	1

Usage

Fan-in / Fan-out

Layout

Files

See also

INV - a Not (or Inverter) gate

3.19 EQ2

Cell

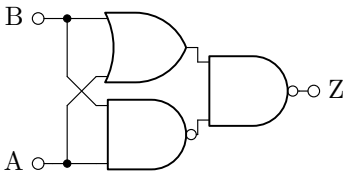
EQ2 - a 2-input Equality (or XNOR) gate

Synopsys

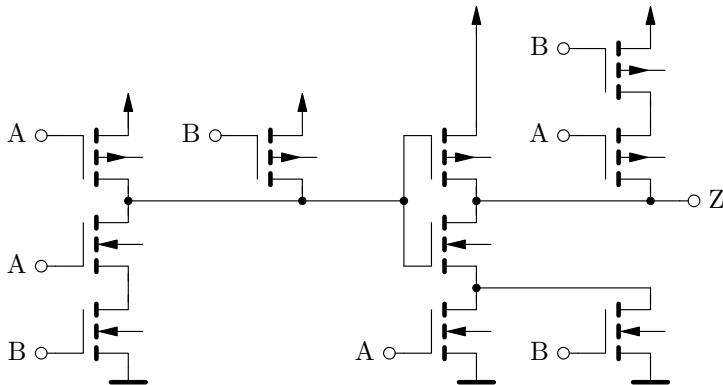
EQ2(Z, B, A)

Description

Circuit



Schematic (two stages, $2T_p/2T_n$ stacked, 10T total)



Truth Table

$Z = \neg(B \oplus A)$

B	A	Z
0	0	1
0	1	0
1	0	0
1	1	1

Usage

Fan-in / Fan-out

Layout

Files

Simulation

- ./Sources/verilog/EQ2.v - Verilog-95 Cell Model
- ./Sources/verilog/EQ2_switch.v - Verilog-2001 Switch-Level Model
- ./TBench/verilog/tb_EQ2.v - Verilog-2001 Self-checking Testbench

Physical Layout

- ?

See also

XOR2 - a 2-input Exclusive-OR (or XOR) gate

3.20 INV

Cell

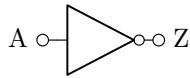
INV - a Not (or Inverter) gate

Synopsys

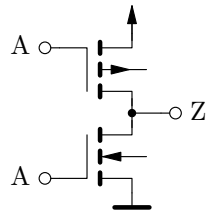
INV(Z, A)

Description

Circuit



Schematic (one stage, $1T_p/1T_n$ stacked, 2T total)



Truth Table

$$Z = \neg A$$

A	Z
0	1
1	0

Usage

Fan-in / Fan-out

Layout

Files

See also

BUF - a Buffer gate

3.21 NAND2

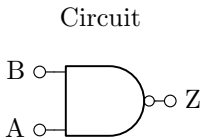
Cell

NAND2 - a 2-input Not-AND (or NAND) gate

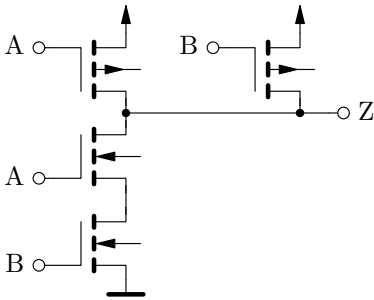
Synopsys

NAND2(Z, B, A)

Description



Schematic (one stage, $1T_p/2T_n$ stacked, 4T total)



Truth Table

$$Z = \neg(B \wedge A)$$

B	A	Z
0	X	1
1	1	0
X	0	1

Usage

Fan-in / Fan-out

Layout

Files

See also

NAND3 - a 3-input Not-AND (or NAND) gate

3.22 NAND3

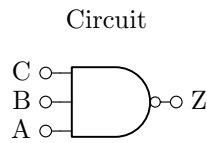
Cell

NAND3 - a 3-input Not-AND (or NAND) gate

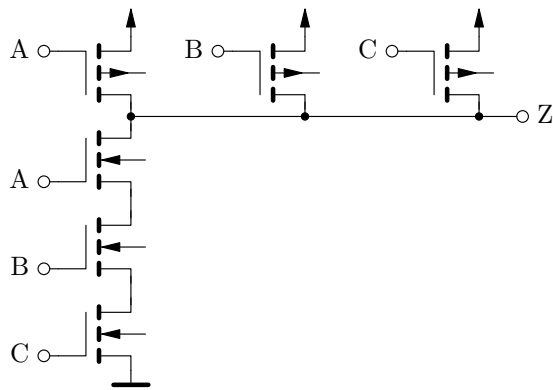
Synopsys

NAND3(Z, C, B, A)

Description



Schematic (one stage, $1T_p/3T_n$ stacked, 6T total)



Truth Table

$$Z = \neg(C \wedge B \wedge A)$$

C	B	A	Z
0	X	X	1
1	1	1	0
X	0	X	1
X	X	0	1

Usage

Fan-in / Fan-out

Layout

Files

See also

NAND2 - a 2-input Not-AND (or NAND) gate

3.23 NOR2

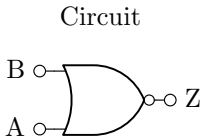
Cell

NOR2 - a 2-input Not-OR (or NOR) gate

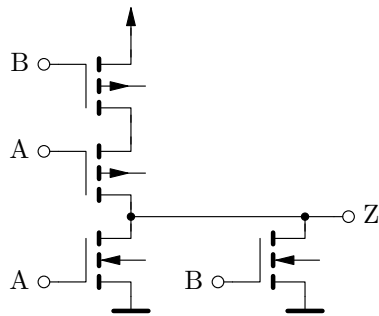
Synopsys

NOR2(Z, B, A)

Description



Schematic (one stage, $2T_p/1T_n$ stacked, 4T total)



Truth Table

$$Z = \neg(B \vee A)$$

B	A	Z
0	0	1
1	X	0
X	1	0

Usage

Fan-in / Fan-out

Layout

Files

See also

NOR3 - a 3-input Not-OR (or NOR) gate

3.24 NOR3

Cell

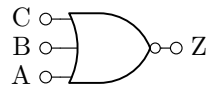
NOR3 - a 3-input Not-OR (or NOR) gate

Synopsys

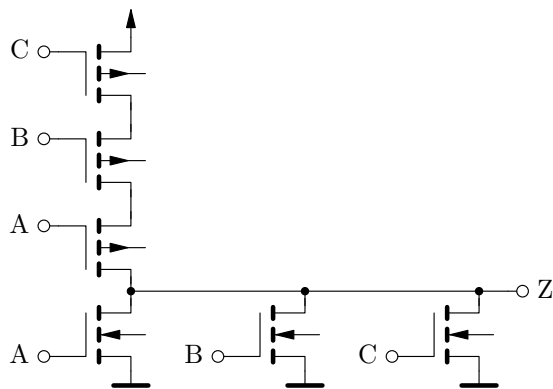
NOR3(Z, C, B, A)

Description

Circuit



Schematic (one stage, $3T_p/1T_n$ stacked, 6T total)



Truth Table

$$Z = \neg(C \vee B \vee A)$$

C	B	A	Z
0	0	0	1
1	X	X	0
X	1	X	0
X	X	1	0

Usage

Fan-in / Fan-out

Layout

Files

See also

NOR2 - a 2-input Not-OR (or NOR) gate

3.25 OA2111

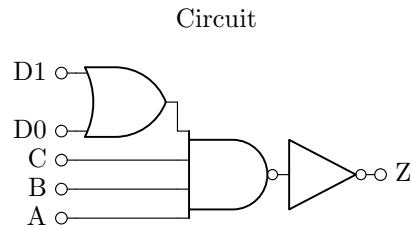
Cell

OA2111 - a 2-1-1-1-input OR-AND gate

Synopsys

OA2111(Z, D1, D0, C, B, A)

Description



Truth Table

$$Z = (D1 \vee D0) \wedge C \wedge B \wedge A$$

D1	D0	C	B	A	Z
0	0	X	X	X	0
1	X	1	1	1	1
X	1	1	1	1	1
X	X	0	X	X	0
X	X	X	0	X	0
X	X	X	X	0	0

Usage

Fan-in / Fan-out

Layout

Files

See also

OA3111 - a 3-1-1-1-input AND-OR gate

3.26 OA3111

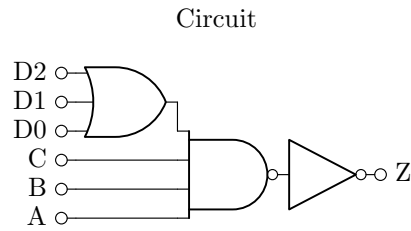
Cell

OA3111 - a 3-1-1-1-input OR-AND gate

Synopsys

OA3111(Z, D2, D1, D0, C, B, A)

Description



Truth Table

$$Z = (D2 \vee D1 \vee D0) \wedge C \wedge B \wedge A$$

D2	D1	D0	C	B	A	Z
0	0	0	X	X	X	0
1	X	X	1	1	1	1
X	1	X	1	1	1	1
X	X	1	1	1	1	1
X	X	X	0	X	X	0
X	X	X	X	0	X	0
X	X	X	X	X	0	0

Usage

Fan-in / Fan-out

Layout

Files

See also

OA2111 - a 2-1-1-1-input AND-OR gate

3.27 OAI21

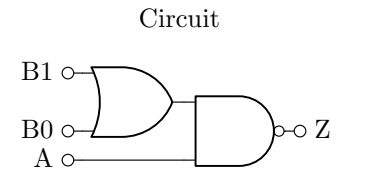
Cell

OAI21 - a 2-1-input OR-AND-Invert gate

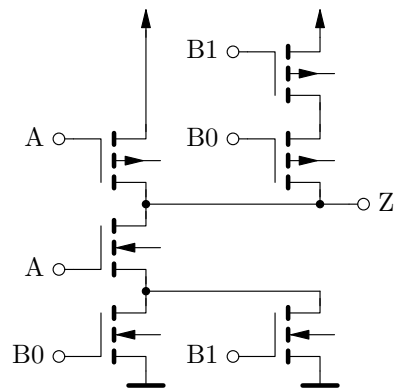
Synopsys

OAI21(Z, B1, B0, A)

Description



Schematic (one stage, $2T_p/2T_n$ stacked, 6T total)



Truth Table

$$Z = \neg((B1 \vee B0) \wedge A)$$

B1	B0	A	Z
0	0	X	1
1	X	1	0
X	1	1	0
X	X	0	1

Usage

Fan-in / Fan-out

Layout

Files

See also

OAI31 - a 3-1-input OR-AND-Invert gate

3.28 OAI22

Cell

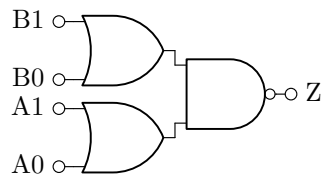
OAI22 - a 2-2-input OR-AND-Invert gate

Synopsys

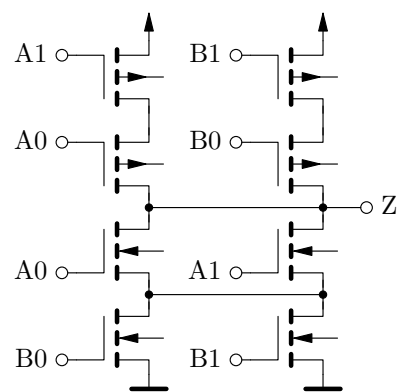
OAI22(Z, B1, B0, A1, A0)

Description

Circuit



Schematic (one stage, $2T_p/2T_n$ stacked, 8T total)



Truth Table

$$Z = \neg((B1 \vee B0) \wedge (A1 \vee A0))$$

B1	B0	A1	A0	Z
0	0	X	X	1
1	X	1	X	0
1	X	X	1	0
X	1	1	X	0
X	1	X	1	0
X	X	0	0	1

Usage

Fan-in / Fan-out

Layout

Files

See also

- OAI32 - a 3-2-input OR-AND-Invert gate
- OAI33 - a 3-3-input OR-AND-Invert gate

3.29 OAI31

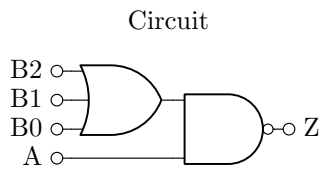
Cell

OAI31 - a 3-1-input OR-AND-Invert gate

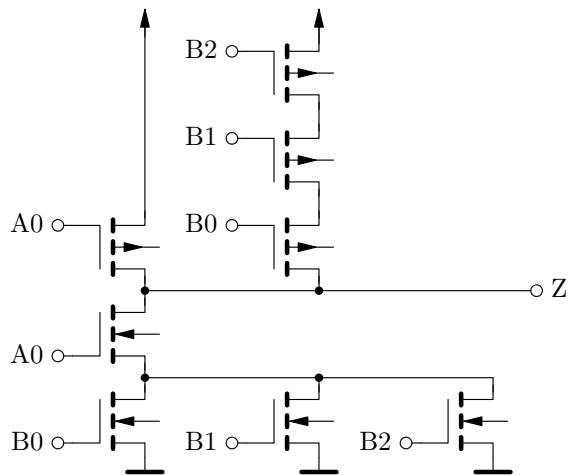
Synopsys

OAI31(Z, B2, B1, B0, A)

Description



Schematic (one stage, $3T_p/2T_n$ stacked, 8T total)



Truth Table

$$Z = \neg((B2 \vee B1 \vee B0) \wedge A)$$

B2	B1	B0	A	Z
0	0	0	X	1
1	X	X	1	0
X	1	X	1	0
X	X	1	1	0
X	X	X	0	1

Usage

Fan-in / Fan-out

Layout

Files

See also

OAI21 - a 2-1-input OR-AND-Invert gate

3.30 OAI32

Cell

OAI32 - a 3-2-input OR-AND-Invert gate

Synopsys

OAI32(Z, B2, B1, B0, A1, A0)

Layout

Files

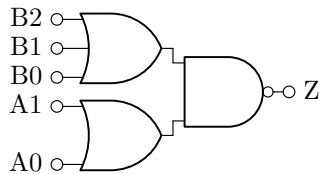
See also

OAI22 - a 2-2-input OR-AND-Invert gate

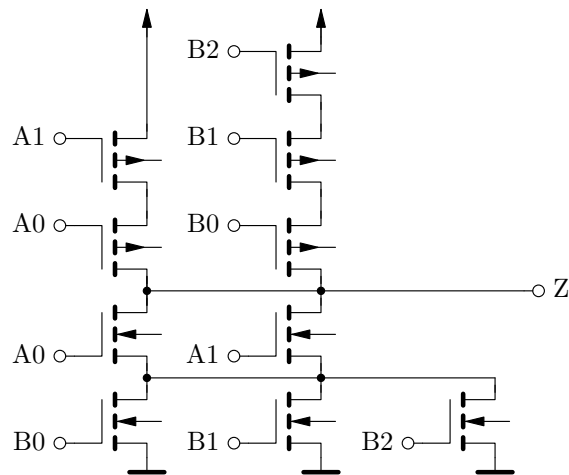
OAI33 - a 3-3-input OR-AND-Invert gate

Description

Circuit



Schematic (one stage, $3T_p/2T_n$ stacked, 10T total)



Truth Table

$$Z = \neg((B2 \vee B1 \vee B0) \wedge (A1 \vee A0))$$

B2	B1	B0	A1	A0	Z
0	0	0	X	X	1
1	X	X	1	X	0
1	X	X	X	1	0
X	1	X	1	X	0
X	1	X	X	1	0
X	X	1	1	X	0
X	X	1	X	1	0
X	X	X	0	0	1

Usage

Fan-in / Fan-out

3.31 OAI33

Cell

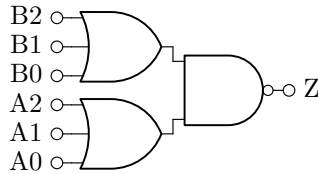
OAI33 - a 3-3-input OR-AND-Invert gate

Synopsys

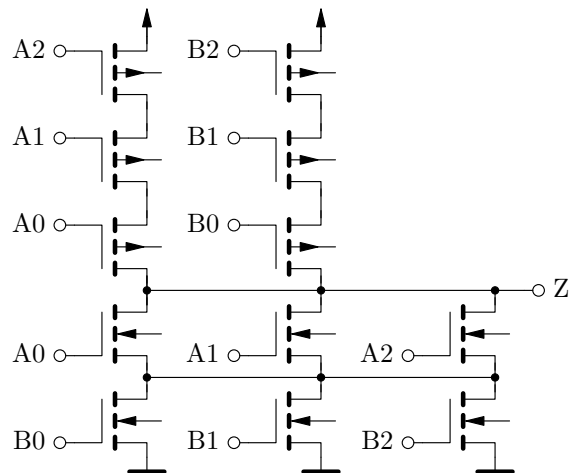
OAI33(Z, B2, B1, B0, A2, A1, A0)

Description

Circuit



Schematic (one stage, $3T_p/2T_n$ stacked, 12T total)



Truth Table

$$Z = \neg((B2 \vee B1 \vee B0) \wedge (A2 \vee A1 \vee A0))$$

B2	B1	B0	A2	A1	A0	Z
0	0	0	X	X	X	1
1	X	X	1	X	X	0
1	X	X	X	1	X	0
1	X	X	X	X	1	0
X	1	X	1	X	X	0
X	1	X	X	1	X	0
X	1	X	X	X	1	0
X	X	1	1	X	X	0
X	X	1	X	1	X	0
X	X	1	X	X	1	0
X	X	X	0	0	0	1

Usage

Fan-in / Fan-out

Layout

Files

See also

- OAI22 - a 2-2-input OR-AND-Invert gate
- OAI32 - a 3-2-input OR-AND-Invert gate

3.32 OAI211

Cell

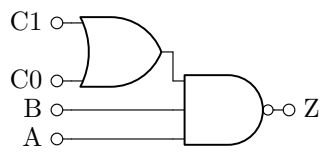
OAI211 - a 2-1-1-input OR-AND-Invert gate

Synopsys

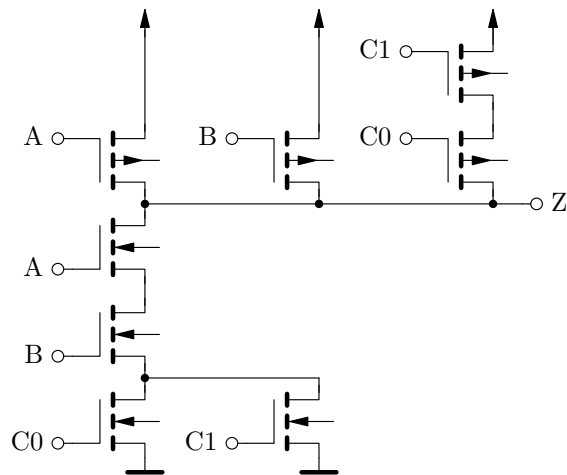
OAI211(Z, C1, C0, B, A)

Description

Circuit



Schematic (one stage, $2T_p/3T_n$ stacked, 8T total)



Truth Table

$$Z = \neg((C1 \vee C0) \wedge B \wedge A)$$

C1	C0	B	A	Z
0	0	X	X	1
1	X	1	1	0
X	1	1	1	0
X	X	0	X	1
X	X	X	0	1

Usage

Fan-in / Fan-out

Layout

Files

See also

OAI311 - a 3-1-1-input OR-AND-Invert gate

3.33 OAI221

Cell

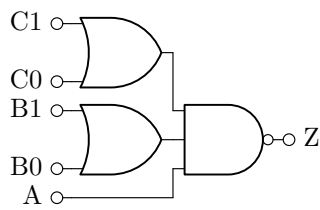
OAI221 - a 2-2-1-input OR-AND-Invert gate

Synopsys

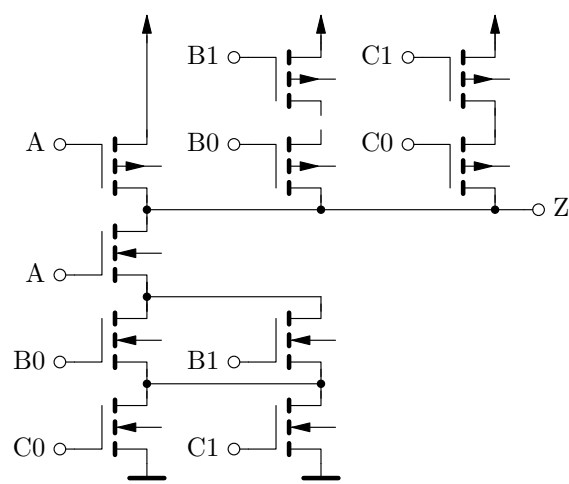
OAI221(Z, C1, C0, B1, B0, A)

Description

Circuit



Schematic (one stage, $2T_p/3T_n$ stacked, 10T total)



Truth Table

$$Z = \neg((C1 \vee C0) \wedge (B1 \vee B0) \wedge A)$$

C1	C0	B1	B0	A	Z
0	0	X	X	X	1
1	X	1	X	1	0
1	X	X	1	1	0
X	1	1	X	1	0
X	1	X	1	1	0
X	X	0	0	X	1
X	X	X	X	0	1

Usage

Fan-in / Fan-out

Layout

Files

See also

- OAI321 - a 3-2-1-input OR-AND-Invert gate
- OAI331 - a 3-3-1-input OR-AND-Invert gate

3.34 OAI222

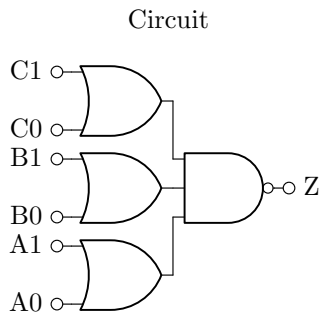
Cell

OAI222 - a 2-2-2-input OR-AND-Invert gate

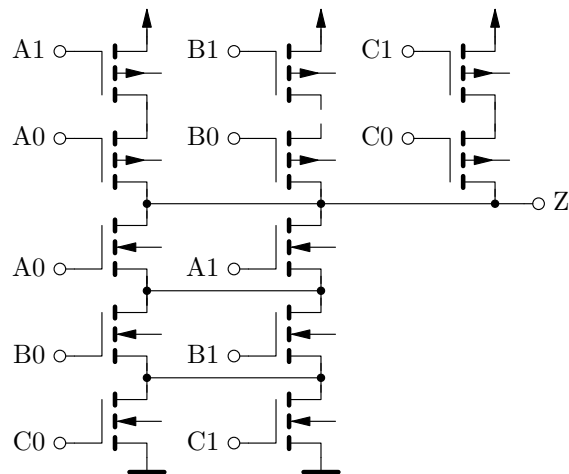
Synopsys

OAI222(Z, C1, C0, B1, B0, A1, A0)

Description



Schematic (one stage, $2T_p/3T_n$ stacked, 12T total)



C1	C0	B1	B0	A1	A0	Z
0	0	X	X	X	X	1
1	X	1	X	1	X	0
1	X	1	X	X	1	0
1	X	X	1	1	X	0
1	X	X	1	X	1	0
X	1	1	X	1	X	0
X	1	1	X	X	1	0
X	1	X	1	1	X	0
X	1	X	1	X	1	0
X	X	0	0	X	X	1
X	X	X	X	0	0	1

Truth Table

$$Z = \neg((C1 \vee C0) \wedge (B1 \vee B0) \wedge (A1 \vee A0))$$

Usage

Fan-in / Fan-out

Layout

Files

See also

- OAI322 - a 2-2-2-input OR-AND-Invert gate
- OAI332 - a 3-3-2-input OR-AND-Invert gate
- OAI333 - a 3-3-3-input OR-AND-Invert gate

3.35 OAI311

Cell

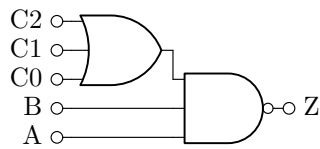
OAI311 - a 3-1-1-input OR-AND-Invert gate

Synopsys

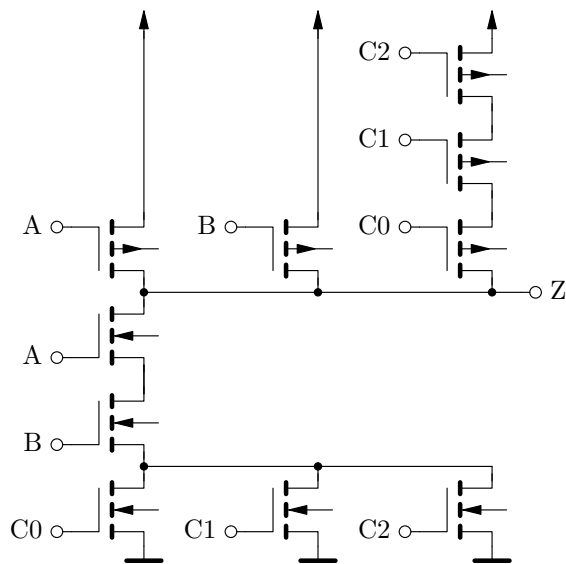
OAI311(Z, C2, C1, C0, B, A)

Description

Circuit



Schematic (one stage, $3T_p/3T_n$ stacked, 10T total)



Truth Table

$$Z = \neg((C2 \vee C1 \vee C0) \wedge B \wedge A)$$

C2	C1	C0	B	A	Z
0	0	0	X	X	1
1	X	X	1	1	0
X	1	X	1	1	0
X	X	1	1	1	0
X	X	X	0	X	1
X	X	X	X	0	1

Usage

Fan-in / Fan-out

Layout

Files

See also

OAI211 - a 2-1-1-input OR-AND-Invert gate

3.36 OAI321

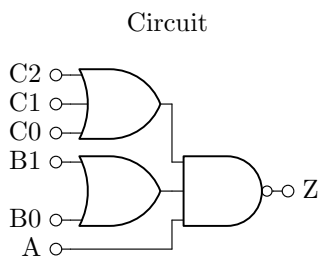
Cell

OAI321 - a 3-2-1-input OR-AND-Invert gate

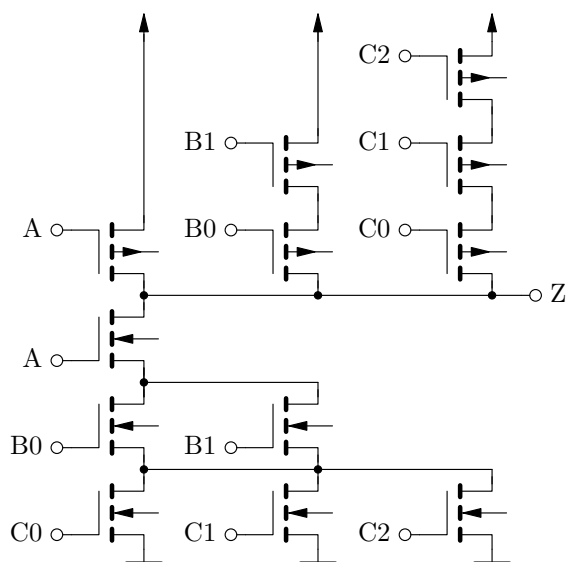
Synopsys

OAI321(Z, C2, C1, C0, B1, B0, A)

Description



Schematic (one stage, $3T_p/3T_n$ stacked, 12T total)



C2	C1	C0	B1	B0	A	Z
0	0	0	X	X	X	1
1	X	X	1	X	1	0
1	X	X	X	1	1	0
X	1	X	1	X	1	0
X	1	X	X	1	1	0
X	X	1	1	X	1	0
X	X	1	X	1	1	0
X	X	X	0	0	X	1
X	X	X	X	X	0	1

Truth Table

$$Z = \neg((C2 \vee C1 \vee C0) \wedge (B1 \vee B0) \wedge A)$$

Usage

Fan-in / Fan-out

Layout

Files

See also

OAI221 - a 2-2-1-input OR-AND-Invert gate

OAI331 - a 3-3-1-input OR-AND-Invert gate

3.37 OAI322

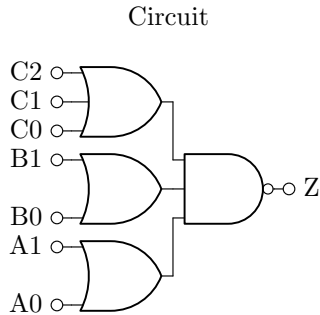
Cell

OAI322 - a 3-2-2-input OR-AND-Invert gate

Synopsys

OAI322(Z, C2, C1, C0, B1, B0, A1, A0)

Description

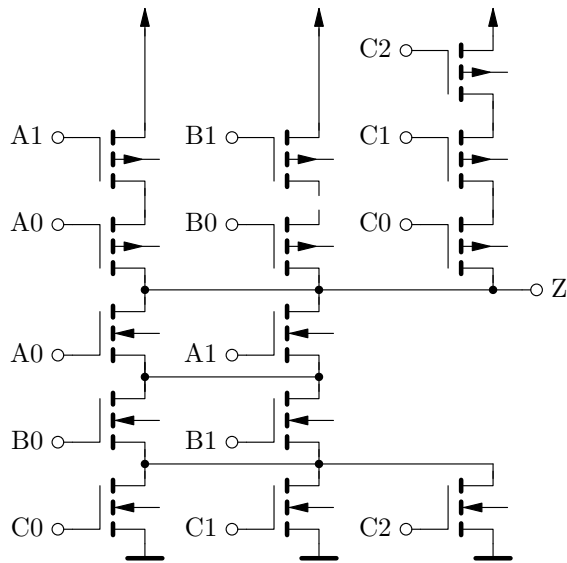


C2	C1	C0	B1	B0	A1	A0	Z
0	0	0	X	X	X	X	1
1	X	X	1	X	1	X	0
1	X	X	1	X	X	1	0
1	X	X	X	1	1	X	0
1	X	X	X	1	X	1	0
X	1	X	1	X	1	X	0
X	1	X	1	X	X	1	0
X	1	X	X	1	1	X	0
X	1	X	X	1	X	1	0
X	X	1	1	X	1	X	0
X	X	1	1	X	X	1	0
X	X	1	X	1	1	X	0
X	X	1	X	1	X	1	0
X	X	X	0	0	X	X	1
X	X	X	X	X	0	0	1

See also

- OAI222 - a 2-2-2-input OR-AND-Invert gate
- OAI332 - a 3-3-2-input OR-AND-Invert gate
- OAI333 - a 3-3-3-input OR-AND-Invert gate

Schematic (one stage, $3T_p/3T_n$ stacked, 14T total)



Truth Table

$$Z = \neg((C2 \vee C1 \vee C0) \wedge (B1 \vee B0) \wedge (A1 \vee A0))$$

Usage

Fan-in / Fan-out

Layout

Files

3.38 OAI331

Cell

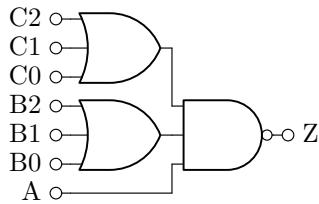
OAI331 - a 3-3-1-input OR-AND-Invert gate

Synopsys

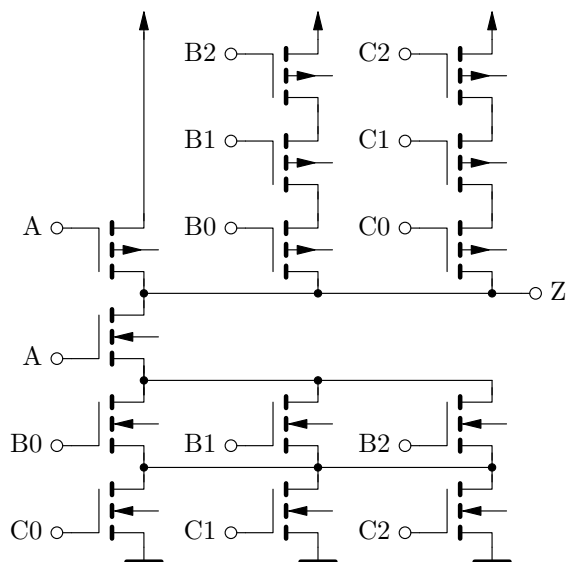
OAI331(Z, C2, C1, C0, B2, B1, B0, A)

Description

Circuit



Schematic (one stage, $3T_p/3T_n$ stacked, 14T total)



C2	C1	C0	B2	B1	B0	A	Z
0	0	0	X	X	X	X	1
1	X	X	1	X	X	1	0
1	X	X	X	1	X	1	0
1	X	X	X	X	1	1	0
X	1	X	1	X	X	1	0
X	1	X	X	1	X	1	0
X	1	X	X	X	1	1	0
X	X	1	1	X	X	1	0
X	X	1	X	1	X	1	0
X	X	1	X	X	1	1	0
X	X	X	0	0	0	X	1
X	X	X	X	X	X	0	1

Truth Table

$$Z = \neg((C2 \vee C1 \vee C0) \wedge (B2 \vee B1 \vee B0) \wedge A)$$

Usage

Fan-in / Fan-out

Layout

Files

See also

OAI221 - a 2-2-1-input OR-AND-Invert gate

OAI321 - a 3-2-1-input OR-AND-Invert gate

3.39 OAI332

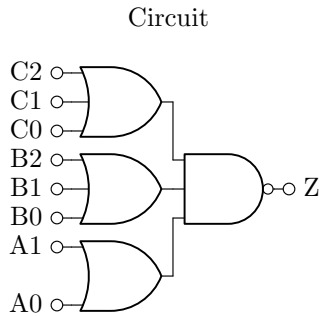
Cell

OAI332 - a 3-3-2-input OR-AND-Invert gate

Synopsys

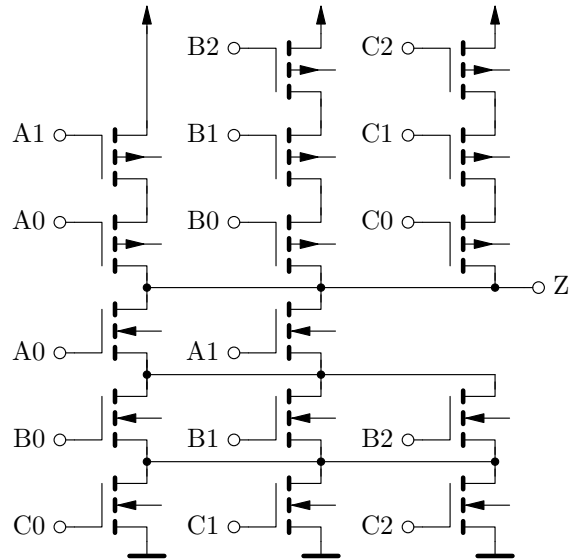
OAI332(Z, C2, C1, C0, B2, B1, B0, A1, A0)

Description



C2	C1	C0	B2	B1	B0	A1	A0	Z
0	0	0	X	X	X	X	X	1
1	X	X	1	X	X	1	X	0
1	X	X	1	X	X	X	1	0
1	X	X	X	1	X	1	X	0
1	X	X	X	1	X	X	1	0
1	X	X	X	X	1	1	X	0
1	X	X	X	X	1	X	1	0
X	1	X	1	X	X	1	X	0
X	1	X	1	X	X	X	1	0
X	1	X	X	1	X	1	X	0
X	1	X	X	1	X	X	1	0
X	1	X	X	X	1	1	X	0
X	1	X	X	X	1	X	1	0
X	X	1	1	X	X	1	X	0
X	X	1	1	X	X	X	1	0
X	X	1	X	1	X	1	X	0
X	X	1	X	1	X	X	1	0
X	X	1	X	X	1	1	X	0
X	X	1	X	X	1	X	1	0
X	X	X	0	0	0	X	X	1
X	X	X	X	X	X	0	0	1

Schematic (one stage, $3T_p/3T_n$ stacked, 16T total)



Truth Table

$$Z = \neg((C2 \vee C1 \vee C0) \wedge (B2 \vee B1 \vee B0) \wedge (A1 \vee A0))$$

Usage

Fan-in / Fan-out

Layout

Files

See also

- OAI222 - a 2-2-2-input OR-AND-Invert gate
- OAI322 - a 3-2-2-input OR-AND-Invert gate
- OAI333 - a 3-3-3-input OR-AND-Invert gate

3.40 OAI333

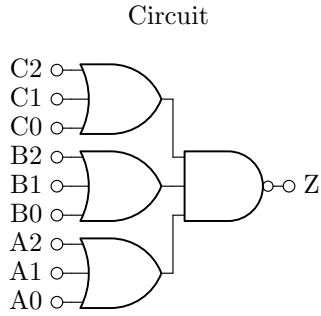
Cell

OAI333 - a 3-3-3-input OR-AND-Invert gate

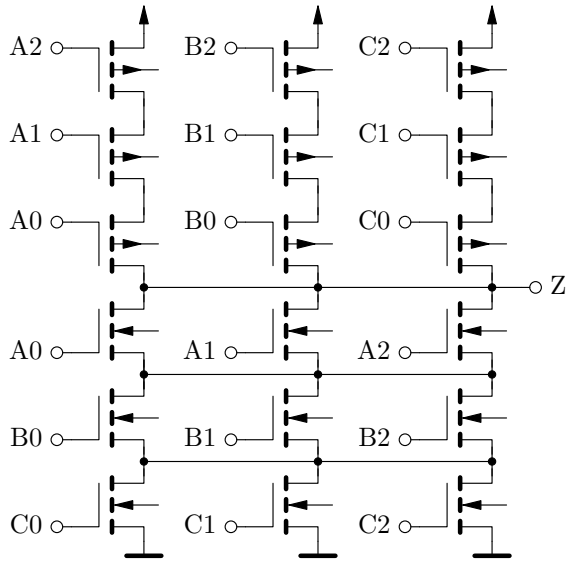
Synopsys

OAI333(Z, C2, C1, C0, B2, B1, B0, A2, A1, A0)

Description



Schematic (one stage, $3T_p/3T_n$ stacked, 18T total)



Truth Table

$$Z = \neg((C2 \vee C1 \vee C0) \wedge (B2 \vee B1 \vee B0) \wedge (A2 \vee A1 \vee A0))$$

Usage

Fan-in / Fan-out

Layout

Files

C2	C1	C0	B2	B1	B0	A2	A1	A0	Z
0	0	0	X	X	X	X	X	X	1
1	X	X	1	X	X	1	X	X	0
1	X	X	1	X	X	X	1	X	0
1	X	X	1	X	X	X	X	1	0
1	X	X	X	1	X	1	X	X	0
1	X	X	X	1	X	X	1	X	0
1	X	X	X	1	X	X	X	1	0
1	X	X	X	X	1	1	X	X	0
1	X	X	X	X	1	X	1	X	0
1	X	X	X	X	1	X	X	1	0
X	1	X	1	X	X	1	X	X	0
X	1	X	1	X	X	X	1	X	0
X	1	X	1	X	X	X	X	1	0
X	1	X	X	1	X	1	X	X	0
X	1	X	X	1	X	X	1	X	0
X	1	X	X	1	X	X	X	1	0
X	1	X	X	X	1	1	X	X	0
X	1	X	X	X	1	X	1	X	0
X	1	X	X	X	1	X	X	1	0
X	X	1	1	X	X	X	1	X	0
X	X	1	1	X	X	X	X	1	0
X	X	1	X	1	X	1	X	X	0
X	X	1	X	1	X	X	1	X	0
X	X	1	X	X	1	1	X	X	0
X	X	1	X	X	1	X	1	X	0
X	X	1	X	X	1	X	X	1	0
X	X	X	0	0	0	X	X	X	1
X	X	X	X	X	X	0	0	0	1

See also

OAI222 - a 2-2-2-input OR-AND-Invert gate

OAI322 - a 3-2-2-input OR-AND-Invert gate

OAI332 - a 3-3-2-input OR-AND-Invert gate

3.41 OR4

Cell

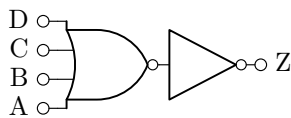
OR4 - a 4-input OR gate

Synopsys

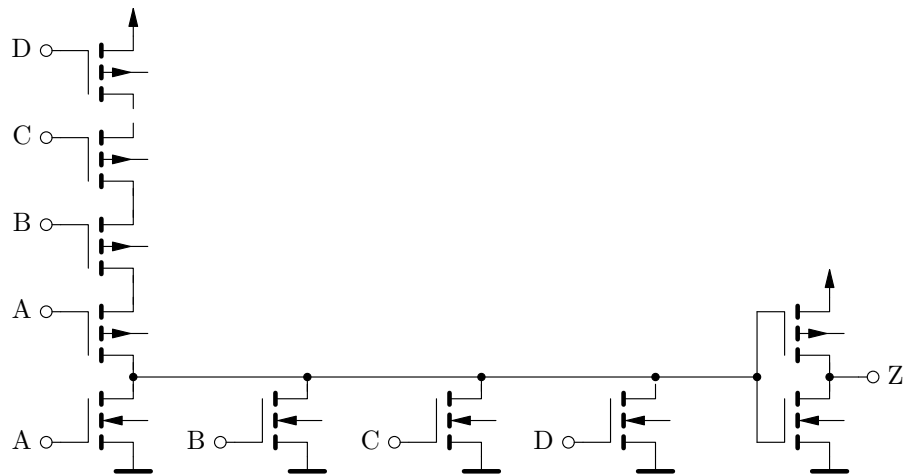
OR4(Z, D, C, B, A)

Description

Circuit



Schematic (two stages, $4T_p/1T_n$ stacked, 10T total)



Truth Table

$$Z = D \vee C \vee B \vee A$$

D	C	B	A	Z
0	0	0	0	0
1	X	X	X	1
X	1	X	X	1
X	X	1	X	1
X	X	X	1	1

Usage

Fan-in / Fan-out

Layout

Files

See also

AND4 - a 4-input AND gate

3.42 XOR2

Files

Cell

Simulation

XOR2 - a 2-input Exclusive-OR (or XOR) gate

- ./Sources/verilog/**XOR2.v** - Verilog-95 Cell Model
- ./Sources/verilog/**XOR2_switch.v** - Verilog-2001 Switch-Level Model
- ./TBench/verilog/**tb_XOR2.v** - Verilog-2001 Self-checking Testbench

Synopsys

XOR2(Z, B, A)

Physical Layout

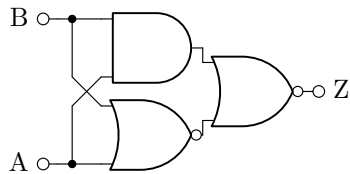
Description

- ?

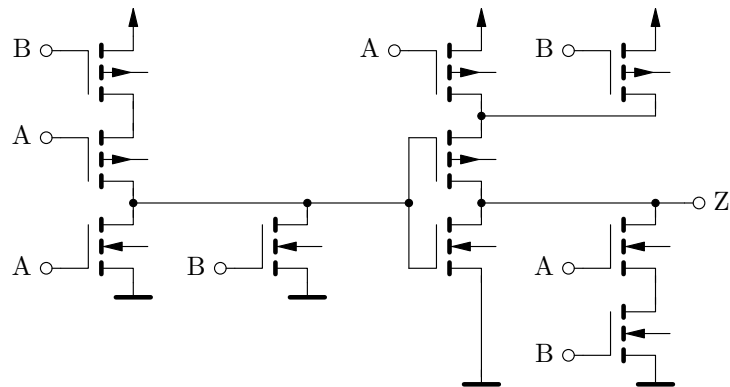
See also

EQ2 - a 2-input Equality (or XNOR) gate

Circuit



Schematic (two stages, $2T_p/2T_n$ stacked, 10T total)



Truth Table

$$Z = B \oplus A$$

B	A	Z
0	0	0
0	1	1
1	0	1
1	1	0

Usage

Fan-in / Fan-out

Keep attention - Fan-in is doubled

Layout

Chapter 4

Physical Cells

4.1 TIE0

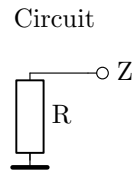
Cell

TIE0 - a Tie-low (or pull-down) cell

Synopsys

TIE0(Z)

Description



Truth Table

$Z = 0$

Z
0

Usage

Fan-in / Fan-out

Layout

Files

See also

TIE1 - a Tie-high (or pull-up) cell

4.2 TIE1

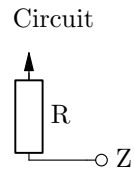
Cell

TIE1 - a Tie-high (or pull-up) cell

Synopsys

TIE1(Z)

Description



Truth Table

$Z = 1$

Z
1

Usage

Fan-in / Fan-out

Layout

Files

See also

TIE0 - a Tie-low (or pull-down) cell

4.3 FILL

Cell

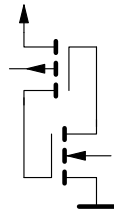
FILL - a Filler cell with capacitance

Synopsys

FILL

Description

Schematic (one stage, 2T total)



Truth Table

No Truth Table applicable.

Usage

Fan-in / Fan-out

Layout

Files

See also

VDDIO
GND
ANA

