Libre Silicon 180nm Standard Cell Library

Hagen Sankowski

January 26, 2018

1 Design Decisions

2 Common Combinatorial Gates

2.1 AND2

2-input AND gate

2.2 AND3

3-input AND gate

2.3 EQ2

2-input Equality gate (aka XNOR)

2.4 EQ3

3-input Equality gate (aka XNOR)

2.5 OR2

2-input OR gate

2.6 OR3

3-input OR gate

2.7 NAND2

2-input NAND

2.8 NAND3

3-input NAND

2.9 NOR2

2-input NOR

2.10 NOR3

3-input NOR

2.11 XOR2

2-input Exclusive-OR

2.12 XOR3

3-input Exclusive-OR

3 Complex Logic Gates

3.1 AOI21

2-1-input AND-OR-Invert complex gate

3.2 AOI211

2-1-1-input AND-OR-Invert complex gate

3.3 AOI22

2-2-input AND-OR-Invert complex gate

3.4 AOI221

2-2-1-input AND-OR-Invert complex gate

3.5 AOI222

2-2-2-input AND-OR-Invert complex gate

3.6 AOI31

3-1-input AND-OR-Invert complex gate

3.7 AOI311

3-1-1-input AND-OR-Invert complex gate

3.8 AOI32

3-2-input AND-OR-Invert complex gate

3.9 AOI321

3-2-1-input AND-OR-Invert complex gate

3.10 AOI322

3-2-2-input AND-OR-Invert complex gate

3.11 AOI33

3-3-input AND-OR-Invert complex gate

3.12 AOI331

3-3-1-input AND-OR-Invert complex gate

3.13 AOI332

3-3-2-input AND-OR-Invert complex gate

3.14 AOI333

3-3-3-input AND-OR-Invert complex gate

3.15 OAI21

2-1-input OR-AND-Invert complex gate

3.16 OAI211

2-1-1-input OR-AND-Invert complex gate

3.17 OAI22

2-2-input OR-AND-Invert complex gate

3.18 OAI221

2-2-1-input OR-AND-Invert complex gate

3.19 OAI222

2-2-2-input OR-AND-Invert complex gate

3.20 OAI31

3-1-input OR-AND-Invert complex gate

3.21 OAI311

3-1-1-input OR-AND-Invert complex gate

3.22 OAI32

3-2-input OR-AND-Invert complex gate

3.23 OAI321

3-2-1-input OR-AND-Invert complex gate

3.24 OAI322

3-2-2-input OR-AND-Invert complex gate

3.25 OAI33

3-3-input OR-AND-Invert complex gate

3.26 OAI331

3-3-1-input OR-AND-Invert complex gate

3.27 OAI332

3-3-2-input OR-AND-Invert complex gate

3.28 OAI333

3-3-3-input OR-AND-Invert complex gate

4 Dedicated Function Gates

4.1 MUX2

2-input Multipexer

4.2 MUX4

4-input Multipexer

4.3 FA2

2-input Full Adder

4.4 HA2

2-input Half Adder

5 Inverter

5.1 INV

Inverter

5.2 INV2

Inverter with strength 2

5.3 INV4

Inverter with strength 4

5.4 INV8

Inverter with strength 8

5.5 INV16

Inverter with strength 16

6 Additionals

6.1 TIE0

Tie-to-Zero cell

6.2 TIE1

Tie-to-One cell

6.3 BUF

non-inverting Buffer

6.4 BUF2

non-inverting Buffer with strength 2

6.5 BUF4

non-inverting Buffer with strength 4

6.6 BUF8

non-inverting Buffer with strength 8

6.7 BUF16

non-inverting Buffer with strength 16

7 Global Clock-/Long Line Buffer

7.1 GBUF

Global Buffer

7.2 GBUF2

Global Buffer with strength 2

7.3 GBUF4

Global Buffer with strength 4

7.4 GBUF8

Global Buffer with strength 8

7.5 GBUF16

Global Buffer with strength 16

8 Sequentials

8.1 SFFR

Scanable D-FlipFlop with Reset

8.2 SFFS

Scanable D-FlipFlop with Set

8.3 SLAR

Scanable D-Latch with Reset

8.4 SLAS

Scanable D-Latch with Set

9 Core Layout Additives

9.1 FILL1

Filler Cell with capacitance

9.2 FILL2

Filler Cell with capacitance

9.3 FILL4

Filler Cell with capacitance

9.4 FILL8

Filler Cell with capacitance

9.5 FILL16

Filler Cell with capacitance

10 Boundary Layout Cells

10.1 PADIN

Boundary Scan Input Pad

10.2 PADOUT

Boundary Scan Output Pad

10.3 PADIO

Boundary Scan (bi-directional) Input/Output Pad

10.4 PADVDD

Power Supply Input Pad

10.5 PADGND

Power Supply Ground Pad

10.6 IOGAP1

IO-Ring Gap cell

10.7 IOGAP2

IO-Ring Gap cell

10.8 IOCORNER

IO-Ring Corner cell