LibreSilicon's Standard Cell Library

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Abstract

Table 1: Document Revision History

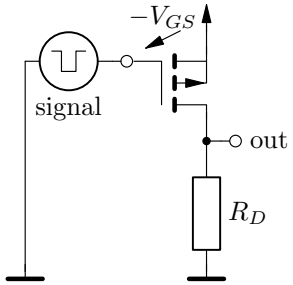
VERSION	DATE	DESCRIPTION	TRACKING NOTES
Draft 0.0	2018-02-01	START w/ empty document	-

0.1 CMOS in a nutshell

This basic initial project is dedicated to the CMOS Technology only and for this reason two types of metal–oxide–semiconductor field-effect transistors (MOSFET) are required.

Historicaly, the first chips with MOSFETs on the mass market were p-channel MOSFETs in enhancement-mode.

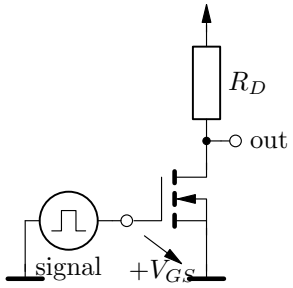
Figure 1: enhancement-mode PMOS transistor use-case



The sectional view of a PMOS transistor in silicon is being shown below

Historicaly later, faster chips with MOSFETs on the mass market were marked as n-channel MOSFETs in enhancement mode also.

Figure 2: enhancement-mode NMOS transistor use-case



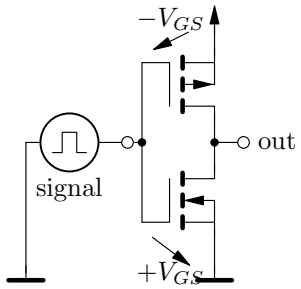
The sectional view of a NMOS transistor in silicon is being shown here also.

Both technologies, the older NMOS as the newer PMOS, have the same disadvantage. Every time, the transistor is switched on, the current between Drain and Source of the transistor is limited by the Resistor on Drain only. Higher currents here meaning higher power consumption for the chip where the transistors are integrated also. If the transistors are switched off, no currents flows between Drain and Source anymore, the power consumption of the chip also goes low.

Et violà, the US-Patent with Number 3356858[1]changed the world and combines both technologies to the new complementary metal-oxide-semiconductor

(CMOS) technology. Instead of every transistor is working against a weak resistor, the transistor works against a complementary switched-off transistor. With the Eyes of our antecessor CMOS doubles the transistor count, but contemporary chips all are build in CMOS.

Figure 3: complementary PMOS and NMOS transistor couple use-case



The sectional view of a NMOS and PMOS transistors couple in silicon - building the CMOS technology - are being shown here also.

[1] https://www.google.com/patents/US3356858

0.2 Design Decisions

0.3 Cell Descriptions

Cell

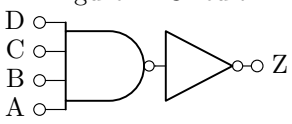
AND4 - a 4-input AND gate

Synopsys

AND4(Z, D, C, B, A)
AND4(Z, D, C, B, A, Vdd, Gnd)

Description

Figure 4: Circuit



Truth Table

Table 2: $Z = D \wedge C \wedge B \wedge A$

D	C	B	A	Z
0	X	X	X	0
X	0	X	X	0
X	X	0	X	0
X	X	X	0	0
1	1	1	1	1

Usage
Fan-in / Fan-out
Layout
Files

Cell

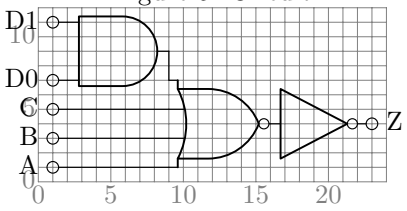
AO2111 - a 2-1-1-1-input AND-OR gate

Synopsys

AO2111(Z, D1, D0, C, B, A)
AO2111(Z, D1, D0, C, B, A, Vdd, Gnd)

Description

Figure 5: Circuit



Truth Table

Table 3: $Z = (D1 \wedge D0) \vee C \vee B \vee A$

D1	D0	C	B	A	Z
0	X	0	0	0	0
0	X	1	X	X	1
0	X	X	1	X	1
0	X	X	X	1	1
X	0	0	0	0	0
X	0	1	X	X	1
X	0	X	1	X	1
X	0	X	X	1	1
1	1	X	X	X	1

Usage
Fan-in / Fan-out
Layout
Files
See also

AO3111 - a 3-1-1-1-input AND-OR gate [Page 7]

Cell

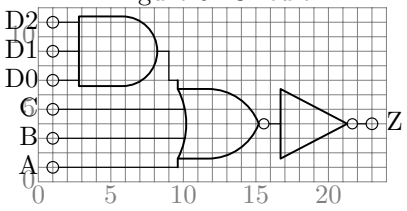
AO3111 - a 3-1-1-1-input AND-OR gate

Synopsys

AO3111(Z, D2, D1, D0, C, B, A)
AO3111(Z, D2, D1, D0, C, B, A, Vdd, Gnd)

Description

Figure 6: Circuit



Truth Table

Table 4: $Z = (D2 \wedge D1 \wedge D0) \vee C \vee B \vee A$

D2	D1	D0	C	B	A	Z
0	X	X	0	0	0	0
0	X	X	1	X	X	1
0	X	X	X	1	X	1
0	X	X	X	X	1	1
X	0	X	0	0	0	0
X	0	X	1	X	X	1
X	0	X	X	1	X	1
X	0	X	X	X	1	1
X	X	0	0	0	0	0
X	X	0	1	X	X	1
X	X	0	X	1	X	1
X	X	0	X	X	1	1
1	1	1	X	X	X	1

Usage
Fan-in / Fan-out
Layout
Files
See also

AO2111 - a 2-1-1-1-input AND-OR gate [Page 6]

Cell

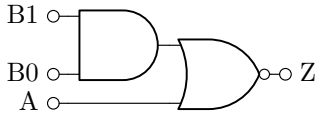
AOI21 - a 2-1-input AND-OR-Invert gate

Synopsys

AOI21(Z, B1, B0, A)
AOI21(Z, B1, B0, A, Vdd, Gnd)

Description

Figure 7: Circuit



Truth Table

Table 5: $Z = \neg((B1 \wedge B0) \vee A)$

B1	B0	A	Z
0	X	0	1
1	1	X	0
X	0	0	1
X	X	1	0

Usage
Fan-in / Fan-out
Layout
Files
See also

AOI31 - a 3-1-input AND-OR-Invert gate [Page 11]

Cell

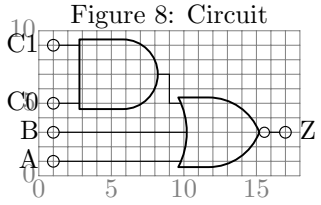
AOI211 - a 2-1-1-input AND-OR-Invert gate

Synopsys

AOI211(Z, C1, C0, B, A)
AOI211(Z, C1, C0, B, A, Vdd, Gnd)

Description

Figure 8: Circuit



Truth Table

Table 6: $Z = \neg((C1 \wedge C0) \vee B \vee A)$

C1	C0	B	A	Z
0	X	0	0	1
1	1	X	X	0
X	0	0	0	1
X	X	1	X	0
X	X	X	1	0

Usage
Fan-in / Fan-out
Layout
Files
See also

AOI311 - a 3-1-1-input AND-OR-Invert gate [Page 12]

Cell

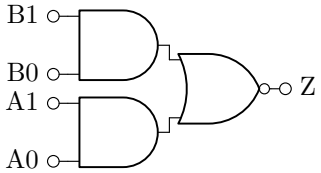
AOI22 - a 2-2-input AND-OR-Invert gate

Synopsys

AOI22(Z, B1, B0, A1, A0)
AOI22(Z, B1, B0, A1, A0, Vdd, Gnd)

Description

Figure 9: Circuit



Truth Table

Table 7: $Z = \neg((B1 \wedge B0) \vee (A1 \wedge A0))$

B1	B0	A1	A0	Z
0	X	0	X	1
0	X	X	0	1
1	1	X	X	0
X	0	0	X	1
X	0	X	0	1
X	X	1	1	0

Usage
Fan-in / Fan-out
Layout
Files
See also

AOI33 - a 3-3-input AND-OR-Invert gate [Page 14]

Cell

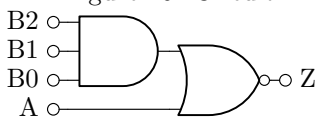
AOI31 - a 3-1-input AND-OR-Invert gate

Synopsys

AOI31(Z, B2, B1, B0, A)
AOI31(Z, B2, B1, B0, A, Vdd, Gnd)

Description

Figure 10: Circuit



Truth Table

Table 8: $Z = \neg((B2 \wedge B1 \wedge B0) \vee A)$

B2	B1	B0	A	Z
0	X	X	0	1
1	1	1	X	0
X	0	X	0	1
X	X	0	0	1
X	X	X	1	0

Usage
Fan-in / Fan-out
Layout
Files
See also

AOI21 - a 2-1-input AND-OR-Invert gate [Page 8]

Cell

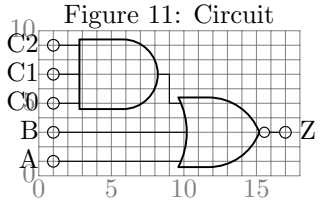
AOI311 - a 3-1-1-input AND-OR-Invert gate

Synopsys

AOI311(Z, C2, C1, C0, B, A)
AOI311(Z, C2, C1, C0, B, A, Vdd, Gnd)

Description

Figure 11: Circuit



Truth Table

Table 9: $Z = \neg((C2 \wedge C1 \wedge C0) \vee B \vee A)$

C2	C1	C0	B	A	Z
0	X	X	0	0	1
1	1	1	X	X	0
X	0	X	0	0	1
X	X	0	0	0	1
X	X	X	1	X	0
X	X	X	X	1	0

Usage
Fan-in / Fan-out
Layout
Files
See also

AOI211 - a 2-1-1-input AND-OR-Invert gate [Page 9]

Cell

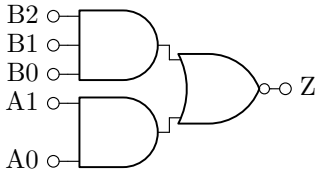
AOI32 - a 3-2-input AND-OR-Invert gate

Synopsys

AOI32(Z, B2, B1, B0, A1, A0)
AOI32(Z, B2, B1, B0, A1, A0, Vdd, Gnd)

Description

Figure 12: Circuit



Truth Table

Table 10: $Z = \neg((B2 \wedge B1 \wedge B0) \vee (A1 \wedge A0))$

B2	B1	B0	A1	A0	Z
0	X	X	0	X	1
0	X	X	X	0	1
1	1	1	X	X	0
X	0	X	0	X	1
X	0	X	X	0	1
X	X	0	0	X	1
X	X	0	X	0	1
X	X	X	1	1	0

Usage
Fan-in / Fan-out
Layout
Files
See also

AOI22 - a 2-2-input AND-OR-Invert gate [Page 10]
AOI33 - a 3-3-input AND-OR-Invert gate [Page 14]

Cell

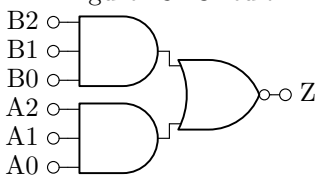
AOI33 - a 3-3-input AND-OR-Invert gate

Synopsys

AOI33(Z, B2, B1, B0, A2, A1, A0)
AOI33(Z, B2, B1, B0, A2, A1, A0, Vdd, Gnd)

Description

Figure 13: Circuit



Truth Table

Table 11: $Z = \neg((B2 \wedge B1 \wedge B0) \vee (A2 \wedge A1 \wedge A0))$

B2	B1	B0	A2	A1	A0	Z
0	X	X	0	X	X	1
0	X	X	X	0	X	1
0	X	X	X	X	0	1
1	1	1	X	X	X	0
X	0	X	0	X	X	1
X	0	X	X	0	X	1
X	0	X	X	X	0	1
X	X	0	0	X	X	1
X	X	0	X	0	X	1
X	X	0	X	X	0	1
X	X	X	1	1	1	0

Usage
Fan-in / Fan-out
Layout
Files
See also

AOI22 - a 2-2-input AND-OR-Invert gate [Page 10]
AOI32 - a 3-2-input AND-OR-Invert gate [Page 13]

Cell

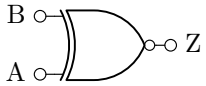
EQ2 - a 2-input Equality (or XNOR) gate

Synopsys

EQ2(Z, B, A)
EQ2(Z, B, A, Vdd, Gnd)

Description

Figure 14: Circuit



Truth Table

Table 12: $Z = \neg(B \oplus A)$

B	A	Z
0	0	1
0	1	0
1	0	0
1	1	1

Usage
Fan-in / Fan-out
Layout
Files
See also

XOR2 - a 2-input Exclusive-OR (or XOR) gate [Page 28]

Cell

NAND2 - a 2-input Not-AND (or NAND) gate

Synopsys

NAND2(Z, B, A)
NAND2(Z, B, A, Vdd, Gnd)

Description

Figure 15: Circuit

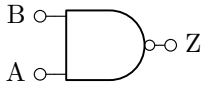
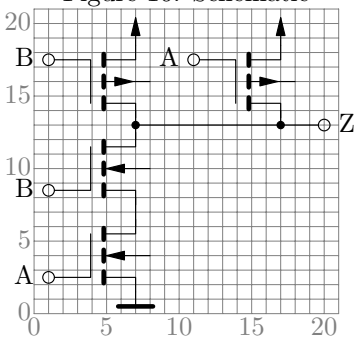


Figure 16: Schematic



Truth Table

Table 13: $Z = \neg(B \wedge A)$

B	A	Z
0	X	1
1	1	0
X	0	1

Usage
Fan-in / Fan-out
Layout
Files
See also

NAND3 - a 3-input Not-AND (or NAND) gate [Page 17]

Cell

NAND3 - a 3-input Not-AND (or NAND) gate

Synopsys

NAND3(Z, C, B, A)
NAND3(Z, C, B, A, Vdd, Gnd)

Description

Figure 17: Circuit

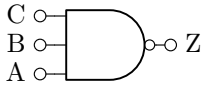
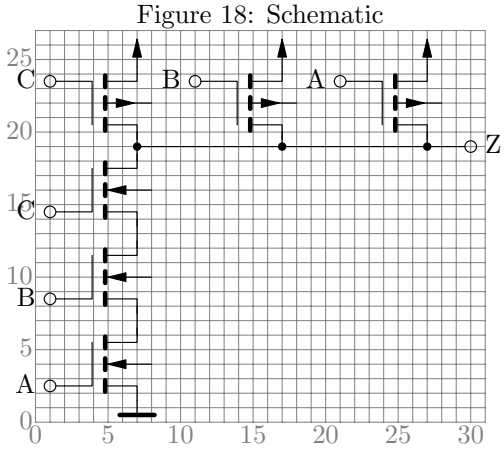


Figure 18: Schematic



Truth Table

Table 14: $Z = \neg(C \wedge B \wedge A)$

C	B	A	Z
0	X	X	1
1	1	1	0
X	0	X	1
X	X	0	1

Usage
Fan-in / Fan-out
Layout
Files
See also

NAND2 - a 2-input Not-AND (or NAND) gate [Page 16]

Cell

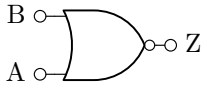
NOR2 - a 2-input Not-OR (or NOR) gate

Synopsys

NOR2(Z, B, A)
NOR2(Z, B, A, Vdd, Gnd)

Description

Figure 19: Circuit



Truth Table

Table 15: $Z = \neg(B \vee A)$

B	A	Z
0	0	1
1	X	0
X	1	0

Usage
Fan-in / Fan-out
Layout
Files
See also

NOR3 - a 3-input Not-OR (or NOR) gate [Page 19]

Cell

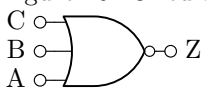
NOR3 - a 3-input Not-OR (or NOR) gate

Synopsys

NOR3(Z, C, B, A)
NOR3(Z, C, B, A, Vdd, Gnd)

Description

Figure 20: Circuit



Truth Table

Table 16: $Z = \neg(C \vee B \vee A)$

C	B	A	Z
0	0	0	1
1	X	X	0
X	1	X	0
X	X	1	0

Usage
Fan-in / Fan-out
Layout
Files
See also

NOR2 - a 2-input Not-OR (or NOR) gate [Page 18]

Cell

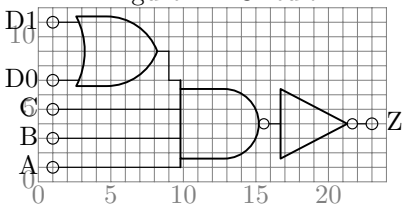
OA2111 - a 2-1-1-1-input OR-AND gate

Synopsys

OA2111(Z, D1, D0, C, B, A)
OA2111(Z, D1, D0, C, B, A, Vdd, Gnd)

Description

Figure 21: Circuit



Truth Table

Table 17: $Z = (D1 \vee D0) \wedge C \wedge B \wedge A$

D1	D0	C	B	A	Z
0	0	X	X	X	0
1	X	1	1	1	1
X	1	1	1	1	1
X	X	0	X	X	0
X	X	X	0	X	0
X	X	X	X	0	0

Usage
Fan-in / Fan-out
Layout
Files
See also

OA3111 - a 3-1-1-1-input AND-OR gate [Page 21]

Cell

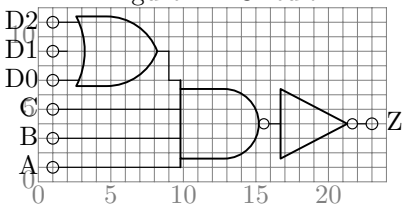
OA3111 - a 3-1-1-1-input OR-AND gate

Synopsys

OA3111(Z, D2, D1, D0, C, B, A)
OA3111(Z, D2, D1, D0, C, B, A, Vdd, Gnd)

Description

Figure 22: Circuit



Truth Table

Table 18: $Z = (D2 \vee D1 \vee D0) \wedge C \wedge B \wedge A$

D2	D1	D0	C	B	A	Z
0	0	0	X	X	X	0
1	X	X	1	1	1	1
X	1	X	1	1	1	1
X	X	1	1	1	1	1
X	X	X	0	X	X	0
X	X	X	X	0	X	0
X	X	X	X	X	0	0

Usage
Fan-in / Fan-out
Layout
Files
See also

OA2111 - a 2-1-1-1-input AND-OR gate [Page 20]

Cell

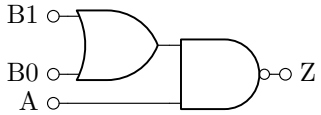
OAI21 - a 2-1-input OR-AND-Invert gate

Synopsys

OAI21(Z, B1, B0, A)
OAI21(Z, B1, B0, A, Vdd, Gnd)

Description

Figure 23: Circuit



Truth Table

Table 19: $Z = \neg((B1 \vee B0) \wedge A)$

B1	B0	A	Z
0	0	X	1
1	X	1	0
X	1	1	0
X	X	0	1

Usage
Fan-in / Fan-out
Layout
Files
See also

OAI31 - a 3-1-input OR-AND-Invert gate [Page 24]

Cell

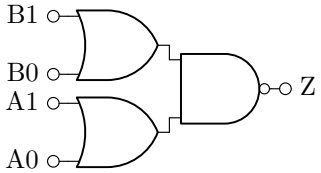
OAI22 - a 2-2-input OR-AND-Invert gate

Synopsys

OAI22(Z, B1, B0, A1, A0)
OAI22(Z, B1, B0, A1, A0, Vdd, Gnd)

Description

Figure 24: Circuit



Truth Table

Table 20: $Z = \neg((B1 \vee B0) \wedge (A1 \vee A0))$

B1	B0	A1	A0	Z
0	0	X	X	1
1	X	1	X	0
1	X	X	1	0
X	1	1	X	0
X	1	X	1	0
X	X	0	0	1

Usage
Fan-in / Fan-out
Layout
Files
See also

OAI32 - a 3-2-input OR-AND-Invert gate [Page 25]
OAI33 - a 3-3-input OR-AND-Invert gate [Page 26]

Cell

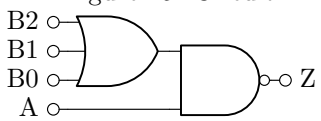
OAI31 - a 3-1-input OR-AND-Invert gate

Synopsys

OAI31(Z, B2, B1, B0, A)
OAI31(Z, B2, B1, B0, A, Vdd, Gnd)

Description

Figure 25: Circuit



Truth Table

Table 21: $Z = \neg((B2 \vee B1 \vee B0) \wedge A)$

B2	B1	B0	A	Z
0	0	0	X	1
1	X	X	1	0
X	1	X	1	0
X	X	1	1	0
X	X	X	0	1

Usage
Fan-in / Fan-out
Layout
Files
See also

OAI21 - a 2-1-input OR-AND-Invert gate [Page 22]

Cell

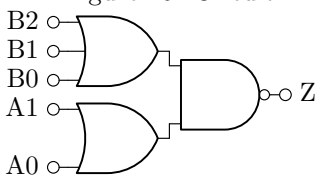
OAI32 - a 3-2-input AND-OR-Invert gate

Synopsys

OAI32(Z, B2, B1, B0, A1, A0)
OAI32(Z, B2, B1, B0, A1, A0, Vdd, Gnd)

Description

Figure 26: Circuit



Truth Table

Table 22: $Z = \neg((B2 \vee B1 \vee B0) \wedge (A1 \vee A0))$

B2	B1	B0	A1	A0	Z
0	0	0	X	X	1
1	X	X	1	X	0
1	X	X	X	1	0
X	1	X	1	X	0
X	1	X	X	1	0
X	X	1	1	X	0
X	X	1	X	1	0
X	X	X	0	0	1

Usage
Fan-in / Fan-out
Layout
Files
See also

OAI22 - a 2-2-input AND-OR-Invert gate [Page 23]
OAI33 - a 3-3-input AND-OR-Invert gate [Page 26]

Cell

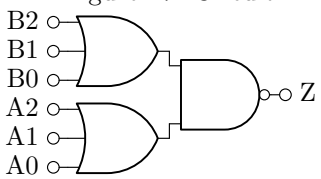
OAI33 - a 3-3-input AND-OR-Invert gate

Synopsys

OAI33(Z, B2, B1, B0, A2, A1, A0)
OAI33(Z, B2, B1, B0, A2, A1, A0, Vdd, Gnd)

Description

Figure 27: Circuit



Truth Table

Table 23: $Z = \neg((B2 \vee B1 \vee B0) \wedge (A2 \vee A1 \vee A0))$

B2	B1	B0	A2	A1	A0	Z
0	0	0	X	X	X	1
1	X	X	1	X	X	0
1	X	X	X	1	X	0
1	X	X	X	X	1	0
X	1	X	1	X	X	0
X	1	X	X	1	X	0
X	1	X	X	X	1	0
X	X	1	1	X	X	0
X	X	1	X	1	X	0
X	X	1	X	X	1	0
X	X	X	0	0	0	1

Usage
Fan-in / Fan-out
Layout
Files
See also

OAI22 - a 2-2-input AND-OR-Invert gate [Page 23]
OAI32 - a 3-2-input AND-OR-Invert gate [Page 25]

Cell

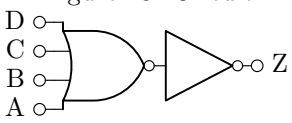
OR4 - a 4-input OR gate

Synopsys

OR4(Z, D, C, B, A)
OR4(Z, D, C, B, A, Vdd, Gnd)

Description

Figure 28: Circuit



Truth Table

Table 24: $Z = D \vee C \vee B \vee A$

D	C	B	A	Z
0	0	0	0	0
1	X	X	X	1
X	1	X	X	1
X	X	1	X	1
X	X	X	1	1

Usage
Fan-in / Fan-out
Layout
Files

Cell

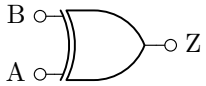
XOR2 - a 2-input Exclusive-OR (or XOR) gate

Synopsys

XOR2(Z, B, A)
XOR2(Z, B, A, Vdd, Gnd)

Description

Figure 29: Circuit



Truth Table

Table 25: $Z = B \oplus A$

B	A	Z
0	0	0
0	1	1
1	0	1
1	1	0

Usage
Fan-in / Fan-out
Layout
Files
See also

EQ2 - a 2-input Equality (or XNOR) gate [Page 15]