# CMPE 240 Spring 2022 Experiment 3 (Implementation of a Boolean Expression)

1 Aim

In this experiment, your knowledge to minimize the number of gates by using decoder and multiplexer gate.

2 Problem

The seven segment displays are used for showing numbers, letter and symbols. They have 7 LEDs and the data can be displayed with the ON/OFF combination of these LEDs (A,B,C,D,E,F,G).
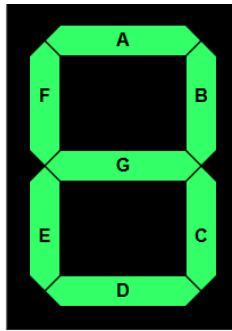
In this experiment, we will use only 5 of the these LEDs. The five inputs denoted as denoted as a, b, c, d, and e. This circuit has only one output *alarm*. The output will be HIGH value when the specific codes are displayed on the 7 Segment Display otherwise the output should be LOW. The codes are as shown in the following figure:
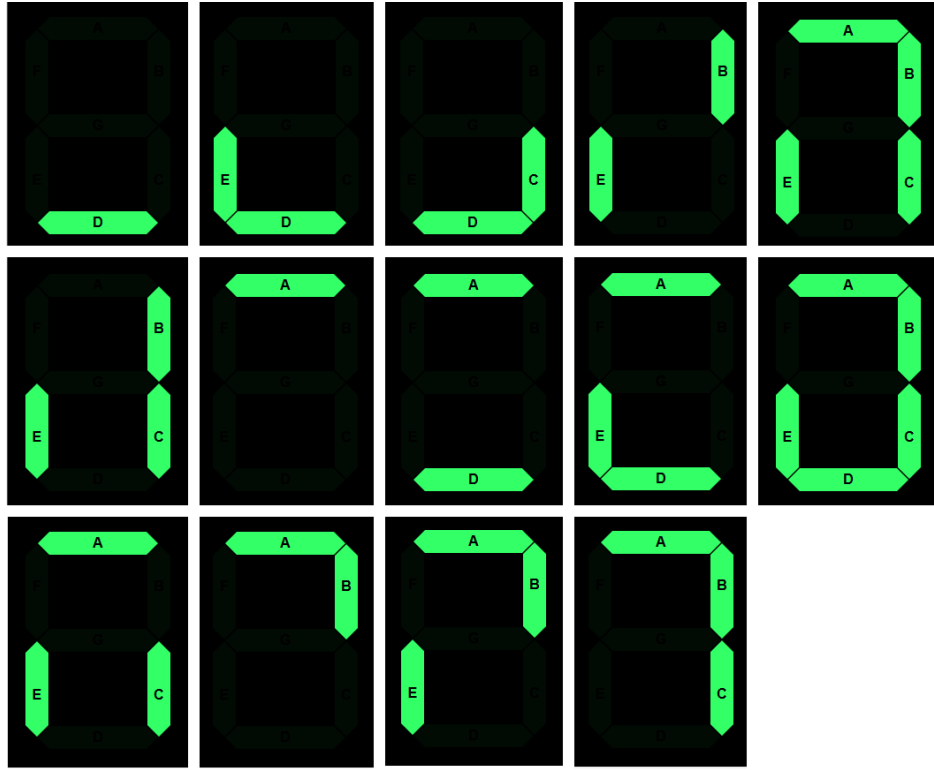
In the implementation, you are only allowed to use one Decoder, one Multiplexer, two binary logic gates (standard gates like AND, OR, XOR, XNOR, NAND, NOR) and NOT gates (as many as needed). Multiplexer can have at most 8 input (i.e. 8 way mux), and decoder can have at most 3 input (i.e. 3 to 8 decoder).

3   Preliminary Work

Before the experiment, you should prepare following materials:

1. Fill the truth table.

2. Analyze the expression and make your design using the allowed components to implement the expression. Then, draw the circuit of your design. If you will use other components than the allowed ones or more than the allowed numbers, you will lose point.

3. Write a verilog code for the circuit drawn in the previous step. Verilog code should have two components. At the first part, you have to write **behavioural level** verilog code which implements the functionality of multiplexer and/or decoder. At the second part, you have to write the **gate level** verilog code for your circuitry which uses the implemented components and additional **built-in** gates (i.e. *AND*, *OR*, *NAND*, *NOR*, *XOR*, or *XNOR*).

4. Write the verilog code for the testbench in order to test all possible input combinations.

Then, follow the steps described in Lab Handbook to submit your preliminary work.