Memory Map

This sections describes the memory map for the device.

2.1 ARM Cortex-A8 Memory Map

Table 2-1. L3 Memory Map

Block Name	Start_address (hex)	End_address (hex)	Size	Description
GPMC (External Memory)	0x0000_0000[1]	0x1FFF_FFFF	512MB	8-/16-bit External Memory (Ex/R/W)[2]
Reserved	0x2000_0000	0x3FFF_FFFF	512MB	Reserved
Boot ROM	0x4000_0000	0x4001_FFFF	128KB	
	0x4002_0000	0x4002_BFFF	48KB	32-bit Ex/R[2] – Public
Reserved	0x4002_C000	0x400F_FFFF	848KB	Reserved
Reserved	0x4010_0000	0x401F_FFFF	1MB	Reserved
Reserved	0x4020_0000	0x402E_FFFF	960KB	Reserved
Reserved	0x402F_0000	0x402F_03FF	64KB	Reserved
SRAM internal	0x402F_0400	0x402F_FFFF		32-bit Ex/R/W[2]
L3 OCMC0	0x4030_0000	0x4030_FFFF	64KB	32-bit Ex/R/W[2] OCMC SRAM
Reserved	0x4031_0000	0x403F_FFFF	960KB	Reserved
Reserved	0x4040_0000	0x4041_FFFF	128KB	Reserved
Reserved	0x4042_0000	0x404F_FFFF	896KB	Reserved
Reserved	0x4050_0000	0x405F_FFFF	1MB	Reserved
Reserved	0x4060_0000	0x407F_FFFF	2MB	Reserved
Reserved	0x4080_0000	0x4083_FFFF	256KB	Reserved
Reserved	0x4084_0000	0x40DF_FFFF	5888KB	Reserved
Reserved	0x40E0_0000	0x40E0_7FFF	32KB	Reserved
Reserved	0x40E0_8000	0x40EF_FFFF	992KB	Reserved
Reserved	0x40F0_0000	0x40F0_7FFF	32KB	Reserved
Reserved	0x40F0_8000	0x40FF_FFFF	992KB	Reserved
Reserved	0x4100_0000	0x41FF_FFFF	16MB	Reserved
Reserved	0x4200_0000	0x43FF_FFFF	32MB	Reserved
L3F CFG Regs	0x4400_0000	0x443F_FFFF	4MB	L3Fast configuration registers
Reserved	0x4440_0000	0x447F_FFFF	4MB	Reserved
L3S CFG Regs	0x4480_0000	0x44BF_FFFF	4MB	L3Slow configuration registers
L4_WKUP	0x44C0_0000	0x44FF_FFFF	4MB	L4_WKUP
Reserved	0x4500_0000	0x45FF_FFFF	16MB	Reserved
McASP0 Data	0x4600_0000	0x463F_FFFF	4MB	McASP0 Data Registers
McASP1 Data	0x4640_0000	0x467F_FFFF	4MB	McASP1 Data Registers
Reserved	0x4680_0000	0x46FF_FFFF	8MB	Reserved
Reserved	0x4700_0000	0x473F_FFFF	4MB	Reserved

(1) The first 1MB of address space 0x0-0xFFFFF is inaccessible externally.
(2) Ex/R/W – Execute/Read/Write.

Table 2-1. L3 Memory Map (continued)

Block Name	Start_address (hex)	End_address (hex)	Size	Description
USBSS	0x4740_0000	0x4740_0FFF	20KB	USB Subsystem Registers
USB0	0x4740_1000	0x4740_12FF		USB0 Controller Registers
USB0_PHY	0x4740_1300	0x4740_13FF		USB0 PHY Registers
USB0 Core	0x4740_1400	0x4740_17FF		USB0 Core Registers
USB1	0x4740_1800	0x4740_1AFF		USB1 Controller Registers
USB1_PHY	0x4740_1B00	0x4740_1BFF		USB1 PHY Registers
USB1 Core	0x4740_1C00	0x4740_1FFF		USB1 Core Registers
USB CPPI DMA Controller	0x4740_2000	0x4740_2FFF		USB CPPI DMA Controller Registers
USB CPPI DMA Scheduler	0x4740_3000	0x4740_3FFF		USB CPPI DMA Scheduler Registers
USB Queue Manager	0x4740_4000	0x4740_4FFF		USB Queue Manager Registers
Reserved	0x4740_5000	0x477F_FFFF	4MB-20KB	Reserved
Reserved	0x4780_0000	0x4780_FFFF	64KB	Reserved
MMCHS2	0x4781_0000	0x4781_FFFF	64KB	MMCHS2
Reserved	0x4782_0000	0x47BF_FFFF	4MB-128KB	Reserved
Reserved	0x47C0_0000	0x47FF_FFFF	4MB	Reserved
L4_PER	0x4800_0000	0x48FF_FFFF	16MB	L4 Peripheral (see L4_PER table)
TPCC (EDMA3CC)	0x4900_0000	0x490F_FFFF	1MB	EDMA3 Channel Controller Registers
Reserved	0x4910_0000	0x497F_FFFF	7MB	Reserved
TPTC0 (EDMA3TC0)	0x4980_0000	0x498F_FFFF	1MB	EDMA3 Transfer Controller 0 Registers
TPTC1 (EDMA3TC1)	0x4990_0000	0x499F_FFFF	1MB	EDMA3 Transfer Controller 1 Registers
TPTC2 (EDMA3TC2)	0x49A0_0000	0x49AF_FFFF	1MB	EDMA3 Transfer Controller 2 Registers
Reserved	0x49B0_0000	0x49BF_FFFF	1MB	Reserved
Reserved	0x49C0_0000	0x49FF_FFFF	4MB	Reserved
L4_FAST	0x4A00_0000	0x4AFF_FFFF	16MB	L4_FAST
Reserved	0x4B00_0000	0x4B13_FFFF	1280KB	Reserved
Reserved	0x4B14_0000	0x4B15_FFFF	128KB	Reserved
DebugSS_DRM	0x4B16_0000	0x4B16_0FFF	4KB	Debug Subsystem: Debug Resource Manager
DebugSS_ETB	0x4B16_2000	0x4B16_2FFF	4KB	Debug Subsystem: Embedded Trace Buffer
Reserved	0x4B16_3000	0x4BFF_FFFF	15MB-396KB	Reserved
EMIF0	0x4C00_0000	0x4CFF_FFFF	16MB	EMIF0 Configuration registers
Reserved	0x4D00_0000	0x4DFF_FFFF	16MB	Reserved
Reserved	0x4E00_0000	0x4FFF_FFFF	32MB	Reserved
GPMC	0x5000_0000	0x50FF_FFFF	16MB	GPMC Configuration registers
Reserved	0x5100_0000	0x52FF_FFFF	32MB	Reserved
Reserved	0x5300_0000	0x530F_FFFF	1MB	Reserved
	0x5310_0000	0x531F_FFFF	1MB	Reserved
Reserved	0x5320_0000	0x533F_FFFF	2MB	Reserved
Reserved	0x5340_0000	0x534F_FFFF	1MB	Reserved
	0x5350_0000	0x535F_FFFF	1MB	Reserved
Reserved	0x5360_0000	0x54BF_FFFF	22MB	Reserved
ADC_TSC DMA	0x54C0_0000	0x54FF_FFFF	4MB	ADC_TSC DMA Port
Reserved	0x5500_0000	0x55FF_FFFF	16MB	Reserved

Table 2-1. L3 Memory Map (continued)

Block Name	Start_address (hex)	End_address (hex)	Size	Description
SGX530	0x5600_0000	0x56FF_FFFF	16MB	SGX530 Slave Port
Reserved	0x5700_0000	0x57FF_FFFF	16MB	Reserved
Reserved	0x5800_0000	0x58FF_FFFF	16MB	Reserved
Reserved	0x5900_0000	0x59FF_FFFF	16MB	Reserved
Reserved	0x5A00_0000	0x5AFF_FFFF	16MB	Reserved
Reserved	0x5B00_0000	0x5BFF_FFFF	16MB	Reserved
Reserved	0x5C00_0000	0x5DFF_FFFF	32MB	Reserved
Reserved	0x5E00_0000	0x5FFF_FFFF	32MB	Reserved
Reserved	0x6000_0000	0x7FFF_FFFF	512MB	Reserved
EMIF0 SDRAM	0x8000_0000	0xBFFF_FFFF	1GB	8-/16-bit External Memory (Ex/R/W)(3)
Reserved	0xC000_0000	0xFFFF_FFFF	1GB	Reserved

(3) Ex/R/W – Execute/Read/Write.

Table 2-2. L4_WKUP Peripheral Memory Map

Region Name	Start Address (hex)	End Address (hex)	Size	Description
L4_WKUP configuration	0x44C0_0000	0x44C0_07FF	2KB	Address/Protection (AP)
	0x44C0_0800	0x44C0_0FFF	2KB	Link Agent (LA)
	0x44C0_1000	0x44C0_13FF	1KB	Initiator Port (IP0)
	0x44C0_1400	0x44C0_17FF	1KB	Initiator Port (IP1)
Reserved	0x44C0_1800	0x44C0_1FFF	2KB	Reserved (IP2 – IP3)
Reserved	0x44C0_2000	0x44CF_FFFF	1MB-8KB	Reserved
Reserved	0x44D0_0000	0x44D0_3FFF	16KB	Reserved
	0x44D0_4000	0x44D0_4FFF	4KB	Reserved
Reserved	0x44D0_5000	0x44D7_FFFF	492KB	Reserved
Reserved	0x44D8_0000	0x44D8_1FFF	8KB	Reserved
	0x44D8_2000	0x44D8_2FFF	4KB	Reserved
Reserved	0x44D8_3000	0x44DF_FFFF	500KB	Reserved
CM_PER	0x44E0_0000	0x44E0_3FFF	1KB	Clock Module Peripheral Registers
CM_WKUP	0x44E0_0400	0x44E0_04FF	256 Bytes	Clock Module Wakeup Registers
CM_DPLL	0x44E0_0500	0x44E0_05FF	256 Bytes	Clock Module PLL Registers
CM_MPU	0x44E0_0600	0x44E0_06FF	256 Bytes	Clock Module MPU Registers
CM_DEVICE	0x44E0_0700	0x44E0_07FF	256 Bytes	Clock Module Device Registers
CM_RTC	0x44E0_0800	0x44E0_08FF	256 Bytes	Clock Module RTC Registers
CM_GFX	0x44E0_0900	0x44E0_09FF	256 Bytes	Clock Module Graphics Controller Registers
CM_CEFUSE	0x44E0_0A00	0x44E0_0AFF	256 Bytes	Clock Module Efuse Registers
PRM_IRQ	0x44E0_0B00	0x44E0_0BFF	256 Bytes	Power Reset Module Interrupt Registers
PRM_PER	0x44E0_0C00	0x44E0_0CFF	256 Bytes	Power Reset Module Peripheral Registers
PRM_WKUP	0x44E0_0D00	0x44E0_0DFF	256 Bytes	Power Reset Module Wakeup Registers
PRM_MPU	0x44E0_0E00	0x44E0_0EFF	256 Bytes	Power Reset Module MPU Registers
PRM_DEV	0x44E0_0F00	0x44E0_0FFF	256 Bytes	Power Reset Module Device Registers
PRM_RTC	0x44E0_1000	0x44E0_10FF	256 Bytes	Power Reset Module RTC Registers

Table 2-2. L4_WKUP Peripheral Memory Map (continued)

Region Name	Start Address (hex)	End Address (hex)	Size	Description
PRM_GFX	0x44E0_1100	0x44E0_11FF	256 Bytes	Power Reset Module Graphics Controller Registers
PRM_CEFUSE	0x44E0_1200	0x44E0_12FF	256 Bytes	Power Reset Module Efuse Registers
Reserved	0x44E0_3000	0x44E0_3FFF	4KB	Reserved
	0x44E0_4000	0x44E0_4FFF	4KB	Reserved
DMTIMER0	0x44E0_5000	0x44E0_5FFF	4KB	DMTimer0 Registers
	0x44E0_6000	0x44E0_6FFF	4KB	Reserved
GPIO0	0x44E0_7000	0x44E0_7FFF	4KB	GPIO Registers
	0x44E0_8000	0x44E0_8FFF	4KB	Reserved
UART0	0x44E0_9000	0x44E0_9FFF	4KB	UART Registers
	0x44E0_A000	0x44E0_AFFF	4KB	Reserved
I2C0	0x44E0_B000	0x44E0_BFFF	4KB	I2C Registers
	0x44E0_C000	0x44E0_CFFF	4KB	Reserved
ADC_TSC	0x44E0_D000	0x44E0_EFFF	8KB	ADC_TSC Registers
	0x44E0_F000	0x44E0_FFFF	4KB	Reserved
Control Module	0x44E1_0000	0x44E1_1FFF	128KB	Control Module Registers
DDR2/3/mDDR PHY	0x44E1_2000	0x44E1_23FF		DDR2/3/mDDR PHY Registers
Reserved	0x44E1_2400	0x44E3_0FFF	4KB	Reserved
DMTIMER1_1MS (Accurate 1ms timer)	0x44E3_1000	0x44E3_1FFF	4KB	DMTimer1 1ms Registers
	0x44E3_2000	0x44E3_2FFF	4KB	Reserved
Reserved	0x44E3_3000	0x44E3_3FFF	4KB	Reserved
	0x44E3_4000	0x44E3_4FFF	4KB	Reserved
WDT1	0x44E3_5000	0x44E3_5FFF	4KB	Watchdog Timer Registers
	0x44E3_6000	0x44E3_6FFF	4KB	Reserved
SmartReflex0	0x44E3_7000	0x44E3_7FFF	4KB	L3 Registers
	0x44E3_8000	0x44E3_8FFF	4KB	Reserved
SmartReflex1	0x44E3_9000	0x44E3_9FFF	4KB	L3 Registers
	0x44E3_A000	0x44E3_AFFF	4KB	Reserved
Reserved	0x44E3_B000	0x44E3_DFFF	12KB	Reserved
RTCSS	0x44E3_E000	0x44E3_EFFF	4KB	RTC Registers
	0x44E3_F000	0x44E3_FFFF	4KB	Reserved
DebugSS Instrumentation HWMaster1 Port	0x44E4_0000	0x44E7_FFFF	256KB	Debug Registers
	0x44E8_0000	0x44E8_0FFF	4KB	Reserved
Reserved	0x44E8_1000	0x44EF_FFFF	508KB	Reserved
Reserved	0x44F0_0000	0x44FF_FFFF	1MB	Reserved

Table 2-3. L4_PER Peripheral Memory Map

Device Name	Start_address (hex)	End_address (hex)	Size	Description
Reserved	0x4800_0000	0x4800_07FF	2KB	Reserved
	0x4800_0800	0x4800_0FFF	2KB	Reserved
	0x4800_1000	0x4800_13FF	1KB	Reserved
	0x4800_1400	0x4800_17FF	1KB	Reserved
	0x4800_1800	0x4800_1BFF	1KB	Reserved
	0x4800_1C00	0x4800_1FFF	1KB	Reserved

Table 2-3. L4_PER Peripheral Memory Map (continued)

Device Name	Start_address (hex)	End_address (hex)	Size	Description
Reserved	0x4800_2000	0x4800_3FFF	8KB	Reserved
Reserved	0x4800_4000	0x4800_7FFF	16KB	Reserved
Reserved	0x4800_8000	0x4800_8FFF	4KB	Reserved
	0x4800_9000	0x4800_9FFF	4KB	Reserved
Reserved	0x4800_A000	0x4800_FFFF	24KB	Reserved
Reserved	0x4801_0000	0x4801_0FFF	4KB	Reserved
	0x4801_1000	0x4801_1FFF	4KB	Reserved
Reserved	0x4801_2000	0x4801_3FFF	8KB	Reserved
Reserved	0x4801_4000	0x4801_FFFF	48KB	Reserved
Reserved	0x4802_0000	0x4802_0FFF	4KB	Reserved
	0x4802_1000	0x4802_1FFF	4KB	Reserved
UART1	0x4802_2000	0x4802_2FFF	4KB	UART1 Registers
	0x4802_3000	0x4802_3FFF	4KB	Reserved
UART2	0x4802_4000	0x4802_4FFF	4KB	UART2 Registers
	0x4802_5000	0x4802_5FFF	4KB	Reserved
Reserved	0x4802_6000	0x4802_7FFF	8KB	Reserved
Reserved	0x4802_8000	0x4802_8FFF	4KB	Reserved
	0x4802_9000	0x4802_9FFF	4KB	Reserved
I2C1	0x4802_A000	0x4802_AFFF	4KB	I2C1 Registers
	0x4802_B000	0x4802_BFFF	4KB	Reserved
Reserved	0x4802_C000	0x4802_CFFF	4KB	Reserved
	0x4802_D000	0x4802_DFFF	4KB	Reserved
Reserved	0x4802_E000	0x4802_EFFF	4KB	Reserved
	0x4802_F000	0x4802_FFFF	4KB	Reserved
McSPI0	0x4803_0000	0x4803_0FFF	4KB	McSPI0 Registers
	0x4803_1000	0x4803_1FFF	4KB	Reserved
Reserved	0x4803_2000	0x4803_2FFF	4KB	Reserved
	0x4803_3000	0x4803_3FFF	4KB	Reserved
Reserved	0x4803_4000	0x4803_4FFF	4KB	Reserved
	0x4803_5000	0x4803_5FFF	4KB	Reserved
Reserved	0x4803_6000	0x4803_6FFF	4KB	Reserved
	0x4803_7000	0x4803_7FFF	4KB	Reserved
McASP0 CFG	0x4803_8000	0x4803_9FFF	8KB	McASP0 CFG Registers
	0x4803_A000	0x4803_AFFF	4KB	Reserved
Reserved	0x4803_B000	0x4803_BFFF	4KB	Reserved
McASP1 CFG	0x4803_C000	0x4803_DFFF	8KB	McASP1 CFG Registers
	0x4803_E000	0x4803_EFFF	4KB	Reserved
Reserved	0x4803_F000	0x4803_FFFF	4KB	Reserved
DMTIMER2	0x4804_0000	0x4804_0FFF	4KB	DMTimer2 Registers
	0x4804_1000	0x4804_1FFF	4KB	Reserved
DMTIMER3	0x4804_2000	0x4804_2FFF	4KB	DMTimer3 Registers
	0x4804_3000	0x4804_3FFF	4KB	Reserved
DMTIMER4	0x4804_4000	0x4804_4FFF	4KB	DMTimer4 Registers
	0x4804_5000	0x4804_5FFF	4KB	Reserved
DMTIMER5	0x4804_6000	0x4804_6FFF	4KB	DMTimer5 Registers
	0x4804_7000	0x4804_7FFF	4KB	Reserved
DMTIMER6	0x4804_8000	0x4804_8FFF	4KB	DMTimer6 Registers

Table 2-3. L4_PER Peripheral Memory Map (continued)

Device Name	Start_address (hex)	End_address (hex)	Size	Description
	0x4804_9000	0x4804_9FFF	4KB	L4 Interconnect
DMTIMER7	0x4804_A000	0x4804_AFFF	4KB	DMTimer7 Registers
	0x4804_B000	0x4804_BFFF	4KB	Reserved
GPIO1	0x4804_C000	0x4804_CFFF	4KB	GPIO1 Registers
	0x4804_D000	0x4804_DFFF	4KB	Reserved
Reserved	0x4804_E000	0x4804_FFFF	8KB	Reserved
Reserved	0x4805_0000	0x4805_FFFF	64KB	Reserved
MMCHS0	0x4806_0000	0x4806_0FFF	4KB	MMCHS0 Registers
	0x4806_1000	0x4806_1FFF	4KB	Reserved
Reserved	0x4806_2000	0x4807_FFFF	120KB	Reserved
ELM	0x4808_0000	0x4808_FFFF	64KB	ELM Registers
	0x4809_0000	0x4809_0FFF	4KB	Reserved
Reserved	0x4809_1000	0x4809_FFFF	60KB	Reserved
Reserved	0x480A_0000	0x480A_FFFF	64KB	Reserved
	0x480B_0000	0x480B_0FFF	4KB	Reserved
Reserved	0x480B_1000	0x480B_FFFF	60KB	Reserved
Reserved	0x480C_0000	0x480C_0FFF	4KB	Reserved
	0x480C_1000	0x480C_1FFF	4KB	Reserved
Reserved	0x480C_2000	0x480C_2FFF	4KB	Reserved
	0x480C_3000	0x480C_3FFF	4KB	Reserved
Reserved	0x480C_4000	0x480C_7FFF	16KB	Reserved
Mailbox 0	0x480C_8000	0x480C_8FFF	4KB	Mailbox Registers
	0x480C_9000	0x480C_9FFF	4KB	Reserved
Spinlock	0x480C_A000	0x480C_AFFF	4KB	Spinlock Registers
	0x480C_B000	0x480C_BFFF	4KB	Reserved
Reserved	0x480C_C000	0x480F_FFFF	208KB	Reserved
Reserved	0x4810_0000	0x4811_FFFF	128KB	Reserved
	0x4812_0000	0x4812_0FFF	4KB	Reserved
Reserved	0x4812_1000	0x4812_1FFF	4KB	Reserved
Reserved	0x4812_2000	0x4812_2FFF	4KB	Reserved
	0x4812_3000	0x4812_3FFF	4KB	Reserved
Reserved	0x4812_4000	0x4813_FFFF	112KB	Reserved
Reserved	0x4814_0000	0x4815_FFFF	128KB	Reserved
	0x4816_0000	0x4816_0FFF	4K	Reserved
Reserved	0x4816_1000	0x4817_FFFF	124KB	Reserved
Reserved	0x4818_0000	0x4818_2FFF	12KB	Reserved
	0x4818_3000	0x4818_3FFF	4KB	Reserved
Reserved	0x4818_4000	0x4818_7FFF	16KB	Reserved
Reserved	0x4818_8000	0x4818_8FFF	4KB	Reserved
	0x4818_9000	0x4818_9FFF	4KB	Reserved
Reserved	0x4818_A000	0x4818_AFFF	4KB	Reserved
	0x4818_B000	0x4818_BFFF	4KB	Reserved
OCP Watchpoint	0x4818_C000	0x4818_CFFF	4KB	OCP Watchpoint Registers
	0x4818_D000	0x4818_DFFF	4KB	Reserved
Reserved	0x4818_E000	0x4818_EFFF	4KB	Reserved
	0x4818_F000	0x4818_FFFF	4KB	Reserved
Reserved	0x4819_0000	0x4819_0FFF	4KB	Reserved

Table 2-3. L4_PER Peripheral Memory Map (continued)

Device Name	Start_address (hex)	End_address (hex)	Size	Description
	0x4819_1000	0x4819_1FFF	4KB	Reserved
Reserved	0x4819_2000	0x4819_2FFF	4KB	Reserved
	0x4819_3000	0x4819_3FFF	4KB	Reserved
Reserved	0x4819_4000	0x4819_BFFF	32KB	Reserved
I2C2	0x4819_C000	0x4819_CFFF	4KB	I2C2 Registers
	0x4819_D000	0x4819_DFFF	4KB	Reserved
Reserved	0x4819_E000	0x4819_EFFF	4KB	Reserved
	0x4819_F000	0x4819_FFFF	4KB	Reserved
McSPI1	0x481A_0000	0x481A_0FFF	4KB	McSPI1 Registers
	0x481A_1000	0x481A_1FFF	4KB	Reserved
Reserved	0x481A_2000	0x481A_5FFF	16KB	Reserved
UART3	0x481A_6000	0x481A_6FFF	4KB	UART3 Registers
	0x481A_7000	0x481A_7FFF	4KB	Reserved
UART4	0x481A_8000	0x481A_8FFF	4KB	UART4 Registers
	0x481A_9000	0x481A_9FFF	4KB	Reserved
UART5	0x481A_A000	0x481A_AFFF	4KB	UART5 Registers
	0x481A_B000	0x481A_BFFF	4KB	Reserved
GPIO2	0x481A_C000	0x481A_CFFF	4KB	GPIO2 Registers
	0x481A_D000	0x481A_DFFF	4KB	Reserved
GPIO3	0x481A_E000	0x481A_EFFF	4KB	GPIO3 Registers
	0x481A_F000	0x481A_FFFF	4KB	Reserved
Reserved	0x481B_0000	0x481B_FFFF	64KB	Reserved
	0x481C_0000	0x481C_0FFF	4KB	Reserved
Reserved	0x481C_1000	0x481C_1FFF	4KB	Reserved
	0x481C_2000	0x481C_2FFF	4KB	Reserved
Reserved	0x481C_3000	0x481C_9FFF	28KB	Reserved
Reserved	0x481C_A000	0x481C_AFFF	4KB	Reserved
	0x481C_B000	0x481C_BFFF	4KB	Reserved
DCAN0	0x481C_C000	0x481C_DFFF	8KB	DCAN0 Registers
	0x481C_E000	0x481C_FFFF	8KB	Reserved
DCAN1	0x481D_0000	0x481D_1FFF	8KB	DCAN1 Registers
	0x481D_2000	0x481D_3FFF	8KB	Reserved
Reserved	0x481D_4000	0x481D_4FFF	4KB	Reserved
	0x481D_5000	0x481D_5FFF	4KB	Reserved
Reserved	0x481D_6000	0x481D_6FFF	4KB	Reserved
	0x481D_7000	0x481D_7FFF	4KB	Reserved
MMC1	0x481D_8000	0x481D_8FFF	4KB	MMC1 Registers
	0x481D_9000	0x481D_9FFF	4KB	Reserved
Reserved	0x481D_A000	0x481F_FFFF	152KB	Reserved
Interrupt controller (INTCPS)	0x4820_0000	0x4820_0FFF	4KB	Interrupt Controller Registers
Reserved	0x4820_1000	0x4823_FFFF	252KB	Reserved
MPUSS config register	0x4824_0000	0x4824_0FFF	4KB	Host ARM non-shared device mapping
Reserved	0x4824_1000	0x4827_FFFF	252KB	Reserved
Reserved	0x4828_0000	0x4828_0FFF	4KB	Reserved
Reserved	0x4828_1000	0x482F_FFFF	508KB	Reserved

Table 2-3. L4_PER Peripheral Memory Map (continued)

Device Name	Start_address (hex)	End_address (hex)	Size	Description
PWM Subsystem 0	0x4830_0000	0x4830_00FF	4KB	PWMSS0 Configuration Registers
eCAP0	0x4830_0100	0x4830_017F		PWMSS eCAP0 Registers
eQEP0	0x4830_0180	0x4830_01FF		PWMSS eQEP0 Registers
ePWM0	0x4830_0200	0x4830_025F		PWMSS ePWM0 Registers
	0x4830_0260	0x4830_1FFF	4KB	Reserved
PWM Subsystem 1	0x4830_2000	0x4830_20FF	4KB	PWMSS1 Configuration Registers
eCAP1	0x4830_2100	0x4830_217F		PWMSS eCAP1 Registers
eQEP1	0x4830_2180	0x4830_21FF		PWMSS eQEP1 Registers
ePWM1	0x4830_2200	0x4830_225F		PWMSS ePWM1 Registers
	0x4830_2260	0x4830_3FFF	4KB	Reserved
PWM Subsystem 2	0x4830_4000	0x4830_40FF	4KB	PWMSS2 Configuration Registers
eCAP2	0x4830_4100	0x4830_417F		PWMSS eCAP2 Registers
eQEP2	0x4830_4180	0x4830_41FF		PWMSS eQEP2 Registers
ePWM2	0x4830_4200	0x4830_425F		PWMSS ePWM2 Registers
	0x4830_4260	0x4830_5FFF	4KB	Reserved
Reserved	0x4830_6000	0x4830_DFFF	32KB	Reserved
LCD Controller	0x4830_E000	0x4830_EFFF	4KB	LCD Registers
	0x4830_F000	0x4830_FFFF	4KB	Reserved
Reserved	0x4831_0000	0x4831_1FFF	8KB	Reserved
	0x4831_2000	0x4831_2FFF	4KB	Reserved
Reserved	0x4831_3000	0x4831_7FFF	20KB	Reserved
Reserved	0x4831_8000	0x4831_BFFF	16KB	Reserved
	0x4831_C000	0x4831_CFFF	4KB	Reserved
Reserved	0x4831_D000	0x4831_FFFF	12KB	Reserved
Reserved	0x4832_0000	0x4832_5FFF	16KB	Reserved
Reserved	0x4832_6000	0x48FF_FFFF	13MB-152KB	Reserved

Table 2-4. L4 Fast Peripheral Memory Map

Device Name	Start_address (hex)	End_address (hex)	Size	Description
L4_Fast configuration	0x4A00_0000	0x4A00_07FF	2KB	Address/Protection (AP)
	0x4A00_0800	0x4A00_0FFF	2KB	Link Agent (LA)
	0x4A00_1000	0x4A00_13FF	1KB	Initiator Port (IP0)
	0x4A00_1400	0x4A00_17FF	1KB	Reserved
	0x4A00_1800	0x4A00_1FFF	2KB	Reserved (IP2 – IP3)
Reserved	0x4A00_2000	0x4A07_FFFF	504KB	Reserved
Reserved	0x4A08_0000	0x4A09_FFFF	128KB	Reserved
	0x4A0A_0000	0x4A0A_0FFF	4KB	Reserved
Reserved	0x4A0A_1000	0x4A0F_FFFF	380KB	Reserved
CPSW_SS	0x4A10_0000	0x4A10_7FFF	32KB	Ethernet Switch Subsystem
CPSW_PORT	0x4A10_0100	0x4A10_07FF		Ethernet Switch Port Control
CPSW_CPDMA	0x4A10_0800	0x4A10_08FF		CPPI DMA Controller Module
CPSW_STATS	0x4A10_0900	0x4A10_09FF		Ethernet Statistics
CPSW_STATERAM	0x4A10_0A00	0x4A10_0BFF		CPPI DMA State RAM
CPSW_CPTS	0x4A10_0C00	0x4A10_0CFF		Ethernet Time Sync Module

Table 2-4. L4 Fast Peripheral Memory Map (continued)

Device Name	Start_address (hex)	End_address (hex)	Size	Description
CPSW_ALE	0x4A10_0D00	0x4A10_0D7F		Ethernet Address Lookup Engine
CPSW_SL1	0x4A10_0D80	0x4A10_0DBF		Ethernet Sliver for Port 1
CPSW_SL2	0x4A10_0DC0	0x4A10_0DFF		Ethernet Sliver for Port 2
Reserved	0x4A10_0E00	0x4A10_0FFF		Reserved
MDIO	0x4A10_1000	0x4A10_10FF		Ethernet MDIO Controller
Reserved	0x4A10_1100	0x4A10_11FF		Reserved
CPSW_WR	0x4A10_1200	0x4A10_1FFF		Ethernet Subsystem Wrapper for RMII/RGMII
CPPI_RAM	0x4A10_2000	0x4A10_3FFF		Communications Port Programming Interface RAM
Reserved	0x4A10_9000	0x4A13_FFFF	220KB	Reserved
Reserved	0x4A14_0000	0x4A14_FFFF	64KB	Reserved
	0x4A15_0000	0x4A15_0FFF	4KB	Reserved
Reserved	0x4A15_1000	0x4A17_FFFF	188KB	Reserved
Reserved	0x4A18_0000	0x4A1A_1FFF	136KB	Reserved
Reserved	0x4A1A_2000	0x4A1A_3FFF	8KB	Reserved
	0x4A1A_4000	0x4A1A_4FFF	4KB	Reserved
Reserved	0x4A1A_5000	0x4A1A_5FFF	4KB	Reserved
	0x4A1A_6000	0x4A1A_6FFF	4KB	Reserved
Reserved	0x4A1A_7000	0x4A1A_7FFF	4KB	Reserved
Reserved	0x4A1A_8000	0x4A1A_9FFF	8KB	Reserved
	0x4A1A_A000	0x4A1A_AFFF	4KB	Reserved
Reserved	0x4A1A_B000	0x4A1A_BFFF	4KB	Reserved
	0x4A1A_C000	0x4A1A_CFFF	4KB	Reserved
Reserved	0x4A1A_D000	0x4A1A_DFFF	4KB	Reserved
Reserved	0x4A1A_E000	0x4A1A_FFFF	8KB	Reserved
	0x4A1B_0000	0x4A1B_0FFF	4KB	Reserved
Reserved	0x4A1B_1000	0x4A1B_1FFF	4KB	Reserved
	0x4A1B_2000	0x4A1B_2FFF	4KB	Reserved
Reserved	0x4A1B_3000	0x4A1B_3FFF	4KB	Reserved
	0x4A1B_4000	0x4A1B_4FFF	4KB	Reserved
Reserved	0x4A1B_5000	0x4A1B_5FFF	4KB	Reserved
	0x4A1B_6000	0x4A1B_6FFF	4KB	Reserved
Reserved	0x4A1B_4000	0x4A1F_FFFF	304KB	Reserved
Reserved	0x4A20_0000	0x4A2F_FFFF	1MB	Reserved
PRU_ICSS	0x4A30_0000	0x4A37_FFFF	512KB	PRU-ICSS Instruction/Data/Control Space
	0x4A38_0000	0x4A38_0FFF	4KB	Reserved
Reserved	0x4A38_1000	0x4A3F_FFFF	508KB	Reserved
Reserved	0x4A40_0000	0x4AFF_FFFF	12MB	Reserved

8.1.12 Clock Module Registers

8.1.12.1 CM_PER Registers

Table 8-29 lists the memory-mapped registers for the CM_PER. All register offset addresses not listed in Table 8-29 should be considered as reserved locations and the register contents should not be modified.

Table 8-29. CM_PER REGISTERS

Offset	Acronym	Register Name	Section
0h	CM_PER_L4LS_CLKSTCTRL		Section 8.1.12.1.1
4h	CM_PER_L3S_CLKSTCTRL		Section 8.1.12.1.2
Ch	CM_PER_L3_CLKSTCTRL		Section 8.1.12.1.3
14h	CM_PER_CPGMAC0_CLKCTRL		Section 8.1.12.1.4
18h	CM_PER_LCDC_CLKCTRL		Section 8.1.12.1.5
1Ch	CM_PER_USB0_CLKCTRL		Section 8.1.12.1.6
24h	CM_PER_TPTC0_CLKCTRL		Section 8.1.12.1.7
28h	CM_PER_EMIF_CLKCTRL		Section 8.1.12.1.8
2Ch	CM_PER_OCMCRAM_CLKCTRL		Section 8.1.12.1.9
30h	CM_PER_GPMC_CLKCTRL		Section 8.1.12.1.10
34h	CM_PER_MCASP0_CLKCTRL		Section 8.1.12.1.11
38h	CM_PER_UART5_CLKCTRL		Section 8.1.12.1.12
3Ch	CM_PER_MMC0_CLKCTRL		Section 8.1.12.1.13
40h	CM_PER_ELM_CLKCTRL		Section 8.1.12.1.14
44h	CM_PER_I2C2_CLKCTRL		Section 8.1.12.1.15
48h	CM_PER_I2C1_CLKCTRL		Section 8.1.12.1.16
4Ch	CM_PER_SPI0_CLKCTRL		Section 8.1.12.1.17
50h	CM_PER_SPI1_CLKCTRL		Section 8.1.12.1.18
60h	CM_PER_L4LS_CLKCTRL		Section 8.1.12.1.19
68h	CM_PER_MCASP1_CLKCTRL		Section 8.1.12.1.20
6Ch	CM_PER_UART1_CLKCTRL		Section 8.1.12.1.21
70h	CM_PER_UART2_CLKCTRL		Section 8.1.12.1.22
74h	CM_PER_UART3_CLKCTRL		Section 8.1.12.1.23
78h	CM_PER_UART4_CLKCTRL		Section 8.1.12.1.24
7Ch	CM_PER_TIMER7_CLKCTRL		Section 8.1.12.1.25
80h	CM_PER_TIMER2_CLKCTRL		Section 8.1.12.1.26
84h	CM_PER_TIMER3_CLKCTRL		Section 8.1.12.1.27
88h	CM_PER_TIMER4_CLKCTRL		Section 8.1.12.1.28
ACh	CM_PER_GPIO1_CLKCTRL		Section 8.1.12.1.29
B0h	CM_PER_GPIO2_CLKCTRL		Section 8.1.12.1.30
B4h	CM_PER_GPIO3_CLKCTRL		Section 8.1.12.1.31
BCh	CM_PER_TPCC_CLKCTRL		Section 8.1.12.1.32
C0h	CM_PER_DCAN0_CLKCTRL		Section 8.1.12.1.33
C4h	CM_PER_DCAN1_CLKCTRL		Section 8.1.12.1.34
CCh	CM_PER_EPWMSS1_CLKCTRL		Section 8.1.12.1.35
D4h	CM_PER_EPWMSS0_CLKCTRL		Section 8.1.12.1.36
D8h	CM_PER_EPWMSS2_CLKCTRL		Section 8.1.12.1.37
DCh	CM_PER_L3_INSTR_CLKCTRL		Section 8.1.12.1.38
E0h	CM_PER_L3_CLKCTRL		Section 8.1.12.1.39
E4h	CM_PER_IEEE5000_CLKCTRL		Section 8.1.12.1.40
E8h	CM_PER_PRU_ICSS_CLKCTRL		Section 8.1.12.1.41
ECh	CM_PER_TIMER5_CLKCTRL		Section 8.1.12.1.42

Table 8-29. CM_PER REGISTERS (continued)

Offset	Acronym	Register Name	Section
F0h	CM_PER_TIMER6_CLKCTRL		Section 8.1.12.1.43
F4h	CM_PER_MMC1_CLKCTRL		Section 8.1.12.1.44
F8h	CM_PER_MMC2_CLKCTRL		Section 8.1.12.1.45
FCh	CM_PER_TPTC1_CLKCTRL		Section 8.1.12.1.46
100h	CM_PER_TPTC2_CLKCTRL		Section 8.1.12.1.47
10Ch	CM_PER_SPINLOCK_CLKCTRL		Section 8.1.12.1.48
110h	CM_PER_MAILBOX0_CLKCTRL		Section 8.1.12.1.49
11Ch	CM_PER_L4HS_CLKSTCTRL		Section 8.1.12.1.50
120h	CM_PER_L4HS_CLKCTRL		Section 8.1.12.1.51
12Ch	CM_PER_OCPWP_L3_CLKSTCTRL		Section 8.1.12.1.52
130h	CM_PER_OCPWP_CLKCTRL		Section 8.1.12.1.53
140h	CM_PER_PRU_ICSS_CLKSTCTRL		Section 8.1.12.1.54
144h	CM_PER_CPSW_CLKSTCTRL		Section 8.1.12.1.55
148h	CM_PER_LCDC_CLKSTCTRL		Section 8.1.12.1.56
14Ch	CM_PER_CLKDIV32K_CLKCTRL		Section 8.1.12.1.57
150h	CM_PER_CLK_24MHZ_CLKSTCTRL		Section 8.1.12.1.58

8.1.12.1.58 CM_PER_CLK_24MHZ_CLKSTCTRL Register (offset = 150h) [reset = 2h]

CM_PER_CLK_24MHZ_CLKSTCTRL is shown in Figure 8-80 and described in Table 8-87.

This register enables the clock domain state transition. It controls the SW supervised clock domain state transition between ON-ACTIVE and ON-INACTIVE states. It also hold one status bit per clock input of the domain.

Figure 8-80. CM_PER_CLK_24MHZ_CLKSTCTRL Register

31	30	29	28	27	26	25	24
Reserved							
R-0h							
23	22	21	20	19	18	17	16
Reserved							
R-0h							
15	14	13	12	11	10	9	8
Reserved							
R-0h							

7	6	5	4	3	2	1	0
Reserved			CLKACTIVITY_CLK_24MHZ_GCLK	Reserved		CLKTRCTRL	
R-0h			R-0h	R-0h		R/W-2h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 8-87. CM_PER_CLK_24MHZ_CLKSTCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	Reserved	R	0h	
4	CLKACTIVITY_CLK_24MHZ_GCLK	R	0h	This field indicates the state of the 24MHz clock in the domain. 0x0 = Inact 0x1 = Act
3-2	Reserved	R	0h	
1-0	CLKTRCTRL	R/W	2h	Controls the clock state transition of the 24MHz clock domain. 0x0 = NO_SLEEP : NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x1 = SW_SLEEP : SW_SLEEP: Start a software forced sleep transition on the domain. 0x2 = SW_WKUP : SW_WKUP: Start a software forced wake-up transition on the domain. 0x3 = Reserved : Reserved.

8.1.12.2 CM_WKUP Registers

Table 8-88 lists the memory-mapped registers for the CM_WKUP. All register offset addresses not listed in Table 8-88 should be considered as reserved locations and the register contents should not be modified.

Table 8-88. CM_WKUP Registers

Offset	Acronym	Register Name	Section
0h	CM_WKUP_CLKSTCTRL		Section 8.1.12.2.1
4h	CM_WKUP_CONTROL_CLKCTRL		Section 8.1.12.2.2
8h	CM_WKUP_GPIO0_CLKCTRL		Section 8.1.12.2.3
Ch	CM_WKUP_L4WKUP_CLKCTRL		Section 8.1.12.2.4
10h	CM_WKUP_TIMER0_CLKCTRL		Section 8.1.12.2.5

Table 8-88. CM_WKUP Registers (continued)

Offset	Acronym	Register Name	Section
14h	CM_WKUP_DEBUGSS_CLKCTRL		Section 8.1.12.2.6
18h	CM_L3_AON_CLKSTCTRL		Section 8.1.12.2.7
1Ch	CM_AUTOIDLE_DPLL_MPU		Section 8.1.12.2.8
20h	CM_IDLEST_DPLL_MPU		Section 8.1.12.2.9
24h	CM_SSC_DELTAMSTEP_DPLL_MPU		Section 8.1.12.2.10
28h	CM-SSC_MODFREQDIV_DPLL_MPU		Section 8.1.12.2.11
2Ch	CM_CLKSEL_DPLL_MPU		Section 8.1.12.2.12
30h	CM_AUTOIDLE_DPLL_DDR		Section 8.1.12.2.13
34h	CM_IDLEST_DPLL_DDR		Section 8.1.12.2.14
38h	CM_SSC_DELTAMSTEP_DPLL_DDR		Section 8.1.12.2.15
3Ch	CM_SSC_MODFREQDIV_DPLL_DDR		Section 8.1.12.2.16
40h	CM_CLKSEL_DPLL_DDR		Section 8.1.12.2.17
44h	CM_AUTOIDLE_DPLL_DISP		Section 8.1.12.2.18
48h	CM_IDLEST_DPLL_DISP		Section 8.1.12.2.19
4Ch	CM_SSC_DELTAMSTEP_DPLL_DISP		Section 8.1.12.2.20
50h	CM_SSC_MODFREQDIV_DPLL_DISP		Section 8.1.12.2.21
54h	CM_CLKSEL_DPLL_DISP		Section 8.1.12.2.22
58h	CM_AUTOIDLE_DPLL_CORE		Section 8.1.12.2.23
5Ch	CM_IDLEST_DPLL_CORE		Section 8.1.12.2.24
60h	CM_SSC_DELTAMSTEP_DPLL_CORE		Section 8.1.12.2.25
64h	CM_SSC_MODFREQDIV_DPLL_CORE		Section 8.1.12.2.26
68h	CM_CLKSEL_DPLL_CORE		Section 8.1.12.2.27
6Ch	CM_AUTOIDLE_DPLL_PER		Section 8.1.12.2.28
70h	CM_IDLEST_DPLL_PER		Section 8.1.12.2.29
74h	CM_SSC_DELTAMSTEP_DPLL_PER		Section 8.1.12.2.30
78h	CM_SSC_MODFREQDIV_DPLL_PER		Section 8.1.12.2.31
7Ch	CM_CLKDCOLDO_DPLL_PER		Section 8.1.12.2.32
80h	CM_DIV_M4_DPLL_CORE		Section 8.1.12.2.33
84h	CM_DIV_M5_DPLL_CORE		Section 8.1.12.2.34
88h	CM_CLKMODE_DPLL_MPU		Section 8.1.12.2.35

Table 8-88. CM_WKUP Registers (continued)

Offset	Acronym	Register Name	Section
8Ch	CM_CLKMODE_DPLL_PER		Section 8.1.12.2.36
90h	CM_CLKMODE_DPLL_CORE		Section 8.1.12.2.37
94h	CM_CLKMODE_DPLL_DDR		Section 8.1.12.2.38
98h	CM_CLKMODE_DPLL_DISP		Section 8.1.12.2.39
9Ch	CM_CLKSEL_DPLL_PERIPH		Section 8.1.12.2.40
A0h	CM_DIV_M2_DPLL_DDR		Section 8.1.12.2.41
A4h	CM_DIV_M2_DPLL_DISP		Section 8.1.12.2.42
A8h	CM_DIV_M2_DPLL_MPU		Section 8.1.12.2.43
ACh	CM_DIV_M2_DPLL_PER		Section 8.1.12.2.44
B0h	CM_WKUP_WKUP_M3_CLKCTRL		Section 8.1.12.2.45
B4h	CM_WKUP_UART0_CLKCTRL		Section 8.1.12.2.46
B8h	CM_WKUP_I2C0_CLKCTRL		Section 8.1.12.2.47
BCh	CM_WKUP_ADC_TSC_CLKCTRL		Section 8.1.12.2.48
C0h	CM_WKUP_SMARTREFLEX0_CLKCTRL		Section 8.1.12.2.49
C4h	CM_WKUP_TIMER1_CLKCTRL		Section 8.1.12.2.50
C8h	CM_WKUP_SMARTREFLEX1_CLKCTRL		Section 8.1.12.2.51
CCh	CM_L4_WKUP_AON_CLKSTCTRL		Section 8.1.12.2.52
D4h	CM_WKUP_WDT1_CLKCTRL		Section 8.1.12.2.53
D8h	CM_DIV_M6_DPLL_CORE		Section 8.1.12.2.54

25.4 GPIO Registers

25.4.1 GPIO Registers

Table 25-5 lists the memory-mapped registers for the GPIO. All register offset addresses not listed in Table 25-5 should be considered as reserved locations and the register contents should not be modified.

Table 25-5. GPIO Registers

Offset	Acronym	Register Name	Section
0h	GPIO_REVISION		Section 25.4.1.1
10h	GPIO_SYSCONFIG		Section 25.4.1.2
20h	GPIO_EOI		Section 25.4.1.3
24h	GPIO_IRQSTATUS_RAW_0		Section 25.4.1.4
28h	GPIO_IRQSTATUS_RAW_1		Section 25.4.1.5
2Ch	GPIO_IRQSTATUS_0		Section 25.4.1.6
30h	GPIO_IRQSTATUS_1		Section 25.4.1.7
34h	GPIO_IRQSTATUS_SET_0		Section 25.4.1.8
38h	GPIO_IRQSTATUS_SET_1		Section 25.4.1.9
3Ch	GPIO_IRQSTATUS_CLR_0		Section 25.4.1.10
40h	GPIO_IRQSTATUS_CLR_1		Section 25.4.1.11
44h	GPIO_IRQWAKEN_0		Section 25.4.1.12
48h	GPIO_IRQWAKEN_1		Section 25.4.1.13
114h	GPIO_SYSSTATUS		Section 25.4.1.14
130h	GPIO_CTRL		Section 25.4.1.15
134h	GPIO_OE		Section 25.4.1.16
138h	GPIO_DATAIN		Section 25.4.1.17
13Ch	GPIO_DATAOUT		Section 25.4.1.18
140h	GPIO_LEVELDETECT0		Section 25.4.1.19
144h	GPIO_LEVELDETECT1		Section 25.4.1.20
148h	GPIO_RISINGDETECT		Section 25.4.1.21
14Ch	GPIO_FALLINGDETECT		Section 25.4.1.22
150h	GPIO_DEBOUNCENABLE		Section 25.4.1.23
154h	GPIO_DEBOUNCINGTIME		Section 25.4.1.24
190h	GPIO_CLEARDATAOUT		Section 25.4.1.25
194h	GPIO_SETDATAOUT		Section 25.4.1.26