Letter of Recommendation

-Badhrinadh Alladurgam

To: Hiring Manager

From: Christof Teuscher, Instructor, ECE 410/510 Hardware for AI/ML

Date: June 15, 2025

I am pleased to recommend Badhrinadh Alladurgam based on his exceptional performance in my ECE 410/510 "Hardware for AI/ML" course during the Spring 2025 term a rigorous, project-driven course focused on practical AI/ML hardware acceleration. He approached the course with professionalism and purpose, building a portfolio that reflects both technical strength and a deep commitment to self-driven learning. The course's self-assessment and self-grading structure motivated him to produce transparent, high-quality work, consistently refining his deliverables based on synthesis metrics and weekly progress checkpoints. His reflective approach demonstrated accountability, engineering rigor, and a strong ability to advocate for and validate his learning journey.

Badhrinadh's main contribution was a complete end-to-end Driver Drowsiness Detection System that integrates both software-based landmark detection and a hardware-accelerated inference module. After extracting facial features using Python, he trained a binary classifier to detect alert vs. drowsy states, then implemented a dense layer in SystemVerilog consisting of signed MAC operations, ReLU, and sigmoid activations. The RTL module was simulated in QuestaSim and synthesized using Synopsys Design Compiler. Despite initial mismatches, he carefully analyzed FSM behavior, signed arithmetic edge cases, and memory loading issues to produce exact output alignment with the software model.

The performance metrics highlight the value of the design: the software inference latency was ~1.48 ms, whereas the post-synthesis RTL implementation showed an 8.75 ns delay, amounting to a >160x speedup. The synthesized design met timing at 100 MHz (10 ns clock period), with a total cell area of 10,397.359200 units and total gate count around 1,160. Power analysis revealed a total dynamic power of 125.4 µW and leakage power of 18.7 µW, confirming its suitability for energy-efficient applications. Badhrinadh validated these outcomes against the constraints defined in the timing reports and corrected all violations flagged during early synthesis iterations.

A key element in his progress was the weekly codefests held as part of the course structure. These sessions acted as practical checkpoints, helping students like Badhrinadh track development stages and build incrementally toward their final project goals. He used these codefests as structured opportunities to implement and verify key milestones ensuring that each module, from input processing to final inference logic, was developed, tested, and integrated on a weekly cadence. This iterative approach ultimately contributed to a robust and validated final model.

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In addition to the capstone project, he completed all weekly challenges, including a systolic array for bubble sort, fixed-point MAC unit, and crossbar matrix-vector operations reflecting neuromorphic computing concepts. He maintained a clean and reproducible GitHub repository, which includes simulation logs, synthesis reports, and structured documentation for each module. His attention to clarity and reproducibility exceeded course expectations and helped create a learning artifact that future students could learn from.

Badhrinadh approached the self-assessment framework with sincerity and determination. As a first-time participant in such an evaluation structure, he fully embraced the process. Rather than focusing on superficial progress, he prioritized deep learning, addressed each challenge systematically, and resolved hardware-software mismatches with rigor and traceability. He took full ownership of his work, often revisiting buggy modules to optimize logic and document debug strategies.

Compared to his peers, Badhrinadh demonstrated exceptional initiative. He consistently chose to explore harder paths, debug deeper layers, and document not just success but the journey of achieving it. His ability to translate AI/ML algorithmic logic into RTL with accurate control and data path separation, verified testbenches, and synthesis validation places his work among the strongest in the course.

In conclusion, Badhrinadh Alladurgam has not only met but exceeded the expectations of ECE 410/510. He demonstrated full-stack knowledge from Python-based ML preprocessing to RTL implementation Verification and synthesis. His willingness to go beyond requirements, his engineering rigor, and his documented results form a compelling case for top performance. I strongly support his self-assigned grade of A.

Sincerely,

Christof Teuscher
Instructor, ECE 410/510 Hardware for AI/ML
Portland State University