ELECTRONICS AND COMMUNICATION ENGINEERING

MINOR DEGREE COURSES (R20)

		L	T	P	M	C
ECM001	**Analog Electronic Circuit Design**	**3**	**1**	**0**	**100**	**4**

Unit I

Diodes: Concepts of diode as a switching element, diode as Limiter, design of: Clipper, half wave & full wave rectifier, Clamper, Voltage multiplier, Capacitor filters, Concepts of Regulators: Series and shunt voltage regulator, Zener diode, Design of Zener diode regulator, Concept of junction capacitance, Varactor diode, LED.

Unit II

Transistors: Concepts of amplifier, Q point, load line analysis, Biasing of BJT, Self-Bias CE, High and low frequency –small signal models of Transistors, Expression of voltage gain, current gain, input & output impedance, Designing CE amplifier, FET fundamentals, Configurations, current-voltage characteristics, Biasing of JFET, Biasing of MOSFET FET small signal model, Design and analysis of RC coupled amplifier, Concept of Feedback, Feedback amplifier configurations, Emitter follower.

Unit III

Op-amps: Ideal OPAMP, Concept of differential amplifier, CMRR, Open & closed loop circuits, importance of feedback loop (positive & negative), inverting & non-inverting amplifiers, Voltage follower, Adder, Design and analysis of Integrator & Differentiator, Comparator, Schmitt Trigger, Instrumentation Amplifier.

Unit IV

Filter Circuits: Design and Analysis of Low pass, High pass, Bandpass, Band reject filters Design and analysis of Oscillators: Barkhausen criterion, Colpitt, Hartley‘s, RC Phase shift, Wien bridge, & Crystal oscillators.

Unit V

555 applications: Design and analysis of Monostable & Astable multi vibrators using 555 and their applications

Textbooks:

1. Muhammad H. Rashid, ―Microelectronic Circuit Analysis and Design‖, Oxford Press.

2. Sedra& Smith, ―Micro-Electronic Circuits theory and applications‖ 2nd edition, Cengage Learning.

Reference Books:

1. JacobMillman& Christos C. Halkias, ―Integrated Electronics‖, Tata -McGraw Hill, 2nd Edition,(2010).

2. Robert L. Boylestad and Louis Nashelsky, ―Electronic Devices and Circuit Theory‖, PHI. 9 th Edition.

ECM002	Information Theory and Coding	L	T	P	M	C
		3	1	0	100	4

Unit I

Introduction: Measure of information, Average information content of symbols in long independent and dependent sequences, Entropy calculation for extension of source. Mark-off statistical model for information source, Entropy and information rate of mark-off source.

Unit II

Encoding of source output Shannon‘s encoding algorithm for dependent and independent sequences. Discrete communication channels, Continuous channels. Source coding theorem, Huffman coding, discrete memory less Channels, Mutual information, Properties of mutual information, Channel Capacity. Channel coding theorem, Differential entropy and mutual information for continuous ensembles, Channel capacity Theorem

Unit III

Error Control coding: Introduction, Types of errors, examples, Types of codes Linear Block Codes: Matrix description, Error detection and correction, Standard arrays and table look up for decoding.

Unit IV

Binary cycle codes: Algebraic structures of cyclic codes, encoding using an (n-k) bit shift register, Syndrome calculation, BCH codes, RS Codes, Olay codes, Shortened cyclic codes, Burst error correcting codes. Burst and Random Error correcting codes.

Unit V

Convolution Codes: Block diagram of encoder, Impulse response of encoder, Time domain approach and Transform domain approach. State representation and state diagram, Tree diagram, trellis diagram.

Text Books

1. K. Sam Shanmugam, ―Digital and Analog communication systems‖, John Wiley, (1996).

2. Simon Haykin, ―Digital communication‖, John Wiley, (2003).

3. R Bose, ―Information Theory, Coding and Cryptography‖, TMH 2007

Reference books:

1. Elements of Information Theory by Thomas Cover, Joy Thomas

2. Channel Codes: Classical and Modern by William Ryan, Shu Lin

3. Information Theory and Reliable Communication by Robert Gallager

4. Kennedy, ―Electronic Communication systems‖, McGraw Hill, 4th Ed., 1999.

		L	T	P	M	C
ECM003	**Nano-electronics**	**3**	**1**	**0**	**100**	**4**

Unit I

Introduction to Nanoelectronics: Nanotechnology potential, Development of Microelectronics, Region of Nanostructures, Complexity Problem, Challenge initiated by Nanoelectronics, Top-down and bottom-up approach and Nanostructures.

Unit II

Quantum electron devices: From classical to quantum physics: upcoming electronic devices, Electrons in mesoscopic structure, Short channel MOS transistor, Split gate transistor, Electron wave transistor, Electron spin transistor, Quantum Cellular Automate, Quantum Dot Array.

Unit III

Nano electronics with tunnelling Devices: Tunnelling Element, Technology of RTD, digital circuit design based on RTD, Principles of Single Electron Transistor (SET), SET circuit design – comparison between FET and SET circuit designs.

Unit IV

Nanofabrication: Nano patterning of nanostructures (e-beam/X-ray, Optical lithography, STM/AFM- SEM & Softlithography).

Unit V

Memory devices and sensors: Nano ferroelectrics, Ferroelectric Random-Access Memory, circuit design, thin film properties and integration. Calorimetric sensors, Electrochemical cells, Surface and bulk acoustic devices, Gas sensitive FETs, Resistive semiconductor gas sensors, Electronic noses, Identification of hazardous solvents and gases, Semiconductor sensor array.

Text books:

1. .K. Goser, P. Glosekotter & J. Dienstuhl, ―Nanoelectronic and Nanosystems–From Transistors to Molecular Quantum Devices‖, Springer, (2004).

2. RainerWaser, ―Nanoelectronics and Information Technology: Advanced Electronic Materials Novel and Devices‖, Wiley VCH, (2005).

3. George W. Hanson, ―Fundamentals of Nanoelectronics‖, Prentice Hall, (2008). BoS

Reference Books:

1. Mick Wilson, Kamali Kannangara, Geoff smith, ―Nanotechnology: Basic Science and Emerging Technologies‖, Overseas press, (2005).

2. W.R. Fahrner, ―Nanotechnology and Nanoelectronics: Materials, Devices, Measurement Techniques‖, Springer, (2010).

ECM004	**Bio-Medical Electronics**	**L**	**T**	**P**	**M**	**C**
		3	**1**	**0**	**100**	**4**

Unit I

Introduction to the physiology of cardiac, nervous & muscular and respiratory systems. Transducers and Electrodes: Different types of transducers & their selection for biomedical applications. Electrode theory, selection criteria of electrodes & different types of electrodes such as, Ag – Ag Cl, pH, etc

Unit II

Cardiovascular measurement: The heart & the other cardiovascular systems. Measurement of Blood pressure-direct and indirect method, Cardiac output and cardiac rate. Electrocardiography-waveform-standard lead systems typical ECG amplifier, phonocardiography, Ballisto cardiography, Cardiac pacemaker –defibrillator –different types and its selection.

Unit III

EEG Instrumentation requirements –EEG electrode –frequency bands – recording systems EMG basic principle-block diagram of a recorder –pre amplifier. Bed side monitor –block diagram-measuring parameters-cardiac tachometer-Alarms-Lead fault indicator-central monitoring. Telemetry – modulation systems – choice of carrier frequency – single channel telemetry systems.

Unit IV

Instrumentation for clinical laboratory: Bio electric amplifiers-instrumentation amplifiers isolation amplifiers-chopper stabilized amplifiers –input guarding – Measurement of pH value of Blood-blood cell counting, blood flow, Respiratory transducers and instruments.

Unit V

Impedance plethysmography. Ultrasonic, X-ray and nuclear imaging. Prostheses and aids: pacemakers, defibrillators, heart-lung machine, artificial kidney, aids for the handicapped. Safety aspects.

Text Books

1. J J Carr, "Introduction to Biomedical Equipment Technology" : Pearson Education 4th e/d

Reference Books

1. K S Kandpur, "Hand book of Biomedical instrumentation", Tata McGraw Hill 2nd e/d.
2. John G Webster, "Medical Instrumentation application and design", John Wiley 3rd e/d.
3. Richard Aston, "Principle of Biomedical Instrumentation and Measurement

ECM005	**MEMS Technology**	**L**	**T**	**P**	**M**	**C**
		3	**1**	**0**	**100**	**4**

Unit I

Overview of MEMS: MEMS and Microsystems - Microsystems and microelectronics, Benefits of miniaturization, Working principle of micro system - Micro sensors, Micro actuators, MEMS with Micro actuators. Materials For MEMS, Scaling Laws in Miniaturization, MEMS Design Considerations

Unit II

Micro fabrication: Introduction, Fabrication Process - Photolithography, Ion implantation, Oxidation, Chemical vapor deposition (CVD), Physical vapor deposition, Deposition by Epitaxy,

Etching, Manufacturing Process -Bulk Micromachining, Surface Micromachining and LIGA Process.

Unit III

Microsystems design, Assembly and Packaging: Micro system Design - Design consideration, process design, Mechanical design, Mechanical design using MEMS. Mechanical packaging of Microsystems, Microsystems packaging, interfacings in Microsystems packaging, packaging technology, selection of packaging materials, signal mapping and transduction

Unit IV

Case Study of MEMS Devices: MEMS with Micro sensors: Pressure sensors, Temperature sensors, Humidity sensors, Accelerometers, Gyroscopes, Biomedical Sensors, Chemical sensors, Optical Sensors. MEMS with micro actuators: Microgrippers, Micromotors, Micro gears, Micropumps.

Unit V

RF MEMS devices: Switch parameters- Basics of switching - Mechanical Switches-Electronic switches for RF and microwave applications - Approaches for low-actuation-voltage switches, Case study of MEMS pressure sensor Packaging.

TEXT BOOKS

1.Tai-Ran Hsu, MEMS and Microsystems: Design, Manufacture, and Nanoscale Engineering, 2 nd Edition, John Wiley & Sons, Inc., Hoboken, New Jersey, 2008.

REFERENCES

1. Marc Madou, ―Fundamentals of Micro Fabrication‖ CRC Press

2. Mohamed Gad-el-Hak, ―The MEMS Handbook‖, CRC Press

3. Gabriel M Rebeiz, "RF MEMS - Theory Design and Technology", John Wiley, 2004

4. Mohamed Gad-el-Hak, ―The MEMS Handbook‖, CRC Press, 2002

5. Chang Liu, ―Foundations of MEMS‖, Pearson Indian Print, 1st Edition, 2012

ECM006	Embedded Systems	L	T	P	M	C
		3	1	0	100	4

UNIT – I

Introduction - Introduction to Embedded Systems : Processor Technology, Role of Processor Selection in Embedded Systems, Design cycle in the development phase for an Embedded System, Using of target system or its Emulator and in-Circuit emulator, Use of software tools for development of an Embedded Systems. Design Technology : Design of custom single purpose processor, optimization of custom single purpose processor, RT level - combination logic and sequential logic.

UNIT – II

RTOS and Overview: Real Time Operating Systems: Architecture of Kernel, Task, Task States and Task Scheduler, Message Queues, Event Registers, Pipes, Signals, Semaphores, Memory Management, Interrupt Routines in an RTOS environment, Basic Design Using RTOS.

UNIT – III

ARM Microcontroller Overview ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the Architecture, Debugging support, General Purpose Registers, Special Registers, Exceptions, Interrupts, Stack operation, Reset sequence

UNIT – IV

ARM Cortex M3 Microcontroller ARM Cortex M3 Instruction Sets and Programming: Assembly basics, Instruction list and description, Thumb and ARM instructions, Special instructions, Useful instructions, CMSIS, Assembly and C language Programming

UNIT – V

Networks for Embedded Systems: The I2C Bus, The CAN bus, SHARC link ports, Ethernet, Bluetooth: specification, Core protocol, IEEE 1149.1 (JTAG) Testability.

TEXT BOOKS:

1. Raj kamal “Embedded systems architecture, programming and design” Tata McGraw-Hill Publishing company Limited.

2. Embedded System Design: A Unified Hardware/Software Introduction Frank Vahid and Tony Givargis

3. Joseph Yiu, The Definitive Guide to the ARM Cortex-M3, 2nd Edition, Newnes, (Elsevier), 2010

REFERENCE BOOKS:

1. Jonathan W Valvano, Embedded Microcomputer Systems, Brooks/cole, Thompson Learning

2. David E. Simon, An Embedded Software Primer, Pearson edition.

3. KVKK Prasad, Embedded and real time systems, Dreemtech Press, 2005.

4. ARM System Developer's Guide-Designing and Optimizing System Software, Andrew N.Sloss,

HONOURS DEGREE COURSES (R20)

COMMUNICATIONS DOMAIN

ECHT101 ADVANCED COMMUNICATIONS AND NETWORKS

L	T	P	M	C
3	1	0	100	4

UNIT - I

Spread Spectrum Communications: Spreading sequences- Properties of Spreading Sequences, Pseudo- noise sequence, Gold sequences, Kasami sequences, Walsh Sequences, Orthogonal Variable Spreading Factor Sequences, Barker Sequence, Complementary Codes Direct sequence spread spectrum: DS-CDMA Model, Conventional receiver, Rake Receiver, Synchronization in CDMA, Power Control, Soft handoff, Multiuser detection – Optimum multiuser detector, Liner multiuser detection.

UNIT - II

Orthogonal Frequency Division Multiplexing: Basic Principles of Orthogonality, Single vs Multicarrier Systems, OFDM Block Diagram and Its Explanation, OFDM Signal Mathematical Representation, Selection parameter for Modulation, Pulse shaping in OFDM Signal and pectral Efficiency, Window in OFDM Signal and Spectrum, Synchronization in OFDM, Pilot Insert in OFDM Transmission and Channel Estimation, Amplitude Limitations in OFDM, FFT Point Selection Constraints in OFDM, CDMA vs OFDM, Hybrid OFDM.

UNIT - III

MIMO Systems: Introduction, Space Diversity and System Based on Space Diversity, Smart Antenna system and MIMO, MIMO Based System Architecture, MIMO Exploits Multipath, Space – Time Processing, Antenna Consideration for MIMO, MIMO Channel Modelling, MIMO Channel Measurement, MIMO Channel Capacity, Cyclic Delay Diversity (CDD), Space Time Coding, Advantages and Applications of MIMO in Present Context, MIMO Applications in 3G Wireless System and Beyond, MIMO-OFDM

UNIT - IV

Wireless LANs/IEEE 802.11x: Introduction to IEEE802.11x Technologies, Evolution of wireless LANs, IEEE 802.11 Design Issues, IEEE 802.11 Services, IEEE 802.11 MAC Layer operations, IEEE 802.11 Layer1, IEEE 802.11 a/b/g Higher Rate Standards, Wireless LAN Security, Computing Wireless Technologies, Typical WLAN Hardware.

UNIT - V

Wireless PANs/IEEE 802.15x: Introduction to IEEE 802.15x Technologies: Wireless PAN Applications and Architecture, IEEE 802.15.1 Physical Layer Details, Bluetooth Link ontrollers Basics, Bluetooth Link Controllers Operational States, IEEE 802.15.1 Protocols and Host ontrol Interface. Evaluation of IEEE 802.15 Standards Broad Band Wireless MANs/IEEE 802.16x: Introduction to WMAN/IEEE 802.16x Technology, IEEE 802.16Wireless MANs, IEEE 802.16 MAC Layer Details, IEEE 802.16 Physical Layer Details, IEEE 802.16 Physical Layer Details for 2-11 GHz, IEEE 802.16 Common System Operations.

TEXT BOOKS:

1. Gary J. Mullett, “Introduction to Wireless Telecommunications Systems and Networks”, CENGAGE
2. Upena Dalal, “Wireless Communication”, Oxford University Press, 2009

REFERENCES:

1. Ke-Lin Du & M N S Swamy, “Wireless Communication System”, Cambridge University Press,
2010
2. Gottapu Sasibhusan Rao, “Mobile Cellular Communication”, PEARSON

ECHT102	ADVANCED DIGITAL SIGNAL PROCESSING	L	T	P	M	C
		3	1	0	100	4

UNIT - I

Overview of DSP, Characterization in time and frequency, FFT Algorithms, Digital filter design and structures: Basic FIR/IIR filter design &structures, design techniques of linear phase FIR filters,IIR filters by impulse invariance, bilinear transformation, FIR/IIR Cascaded lattice structures, parallel realization of IIR.

UNIT-II

Multi rate DSP, Decimators and Interpolators, Sampling rate conversion, multistage decimator & interpolator, poly phase filters, QMF, digital filter banks, Applications in subband coding.

UNIT-III

Linear prediction & optimum linear filters, stationary random process, forward-backward linear prediction filters, solution of normal equations, AR Lattice and ARMA Lattice-Ladder Filters, Wiener Filters for Filtering and Prediction.

UNIT-IV

Adaptive Filters, Applications, Gradient Adaptive Lattice, Minimum mean square criterion, LMS algorithm, Recursive Least Square algorithm.

UNIT-V

Estimation of Spectra from Finite-Duration Observations of Signals. Nonparametric Methods for Power Spectrum Estimation, Parametric Methods for Power Spectrum Estimation, Minimum-Variance Spectral Estimation, Eigen analysis Algorithms for Spectrum Estimation.

TEXTBOOKS:

1. J. G. Proakis and D.G. Manolakis, “Digital signal processing: Principles, Algorithm and Applications”, 4th Edition, Prentice Hall, 2007.
2. N. J. Fliege, “Multirate Digital Signal Processing: Multirate Systems -Filter Banks – Wavelets”, 1st Edition, John Wiley and Sons Ltd, 1999.

REFERENCES:

1. Bruce W. Suter, “Multirate and Wavelet Signal Processing”,1st Edition, Academic Press, 1997.
2. M. H. Hayes, “Statistical Digital Signal Processing and Modeling”, John Wiley & Sons Inc., 2002.
3. S. Haykin, “Adaptive Filter Theory”, 4th Edition, Prentice Hall, 2001.
4. D. G. Manolakis, V. K. Ingle and S. M. Kogon, “Statistical and Adaptive Signal Processing”, McGraw Hill, 2000

ECHT103	IOT AND ITS APPLICATIONS	L	T	P	M	C
		3	1	0	100	4

UNIT- I

IoT & Web Technology The Internet of Things Today, Time for Convergence, Towards the IoT Universe, Internet of Things Vision, IoT Strategic Research and Innovation Directions, IoT Applications, Future Internet Technologies, Infrastructure, Networks and Communication, Processes, Data Management, Security, Privacy & Trust, Device Level Energy Issues, IoT Related Standardization, Recommendations on Research Topics.

UNIT- II

M2M to IoT – A Basic Perspective– Introduction, Some Definitions, M2M Value Chains, IoT Value Chains, An emerging industrial structure for IoT, The international driven global value chain and global information monopolies. M2M to IoT-An Architectural Overview– Building an architecture, Main design principles and needed capabilities, An IoT architecture outline, standards considerations.

UNIT- III

IoT Architecture -State of the Art – Introduction, State of the art, Architecture Reference Model- Introduction, Reference Model and architecture, IoT reference Model, IoT Reference Architecture- Introduction, Functional View, Information View, Deployment and Operational View, Other Relevant architectural views.

UNIT- IV

IoT Applications for Value Creations Introduction, IoT applications for industry: Future Factory Concepts, Brownfield IoT, Smart Objects, Smart Applications, Four Aspects in your Business to Master IoT, Value Creation from Big Data and Serialization, IoT for Retailing Industry, IoT For Oil and Gas Industry, Opinions on IoT Application and Value for Industry, Home Management, eHealth.

UNIT- V

Internet of Things Privacy, Security and Governance Introduction, Overview of Governance, Privacy and Security Issues,

TEXTBOOKS

1. Vijay Madisetti and Arshdeep Bahga, “Internet of Things (A Hands-on-Approach)”, 1st Edition, VPT, 2014.
2. Francis daCosta, “Rethinking the Internet of Things: A Scalable Approach to Connecting Everything”, 1st Edition, Apress Publications, 2013.
3. Cuno Pfister, “Getting Started with the Internet of Things”, O Reilly Media, 2011.

ECHT104 CODING THEORY AND TECHNIQUES

L	T	P	M	C
3	1	0	100	4

UNIT – I

Coding for Reliable Digital Transmission and storage: Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, Types of Errors, Error Control Strategies. Linear Block Codes Introduction to Linear Block Codes, Syndrome and Error Detection, Minimum Distance of a Block code, Error-Detecting and Error-correcting Capabilities of a Block code, Standard array and Syndrome Decoding, Probability of an undetected error for Linear Codes over a BSC, Hamming Codes. Applications of Block codes for Error control in data storage system

UNIT - II

Cyclic Codes Description, Generator and Parity-check Matrices, Encoding, Syndrome Computation and Error Detection, Decoding, Cyclic Hamming Codes, Shortened cyclic codes, Error-trapping decoding for cyclic codes, Majority logic decoding for cyclic codes.

UNIT – III

Convolutional Codes Encoding of Convolutional Codes, Structural and Distance Properties, maximum likelihood decoding, Sequential decoding, Majority- logic decoding of Convolution codes. Application of Viterbi Decoding and Sequential Decoding, Applications of Convolutional codes in ARQ system.

UNIT – IV

Turbo Codes LDPC Codes- Codes based on sparse graphs, Decoding for binary erasure channel, Log-likelihood algebra, Brief propagation, Product codes, Iterative decoding of product codes, Concatenated convolutional codes- Parallel concatenation, The UMTS Turbo code, Serial concatenation, Parallel concatenation, Turbo decoding

UNIT - V

Space-Time Codes Introduction, Digital modulation schemes, Diversity, Orthogonal space- Time Block codes, Alamouti's schemes, Extension to more than Two Transmit Antennas, Simulation Results, Spatial Multiplexing: General Concept, Iterative APP Preprocessing and Per-layer Decoding, Linear Multilayer Detection, Original BLAST Detection, QL Decomposition and Interface Cancellation, Performance of Multi – Layer Detection Schemes, Unified Description by Linear Dispersion Codes.

TEXT BOOKS

1. Error Control Coding- Fundamentals and Applications –Shu Lin, Daniel J. Costello, Jr, Prentice Hall, Inc.
2. Error Correcting Coding Theory-Man Young Rhee, McGraw-Hill, 1989.

REFERENCES

1. Digital Communications-Fundamental and Application - Bernard Sklar, PE.
2. Digital Communications- John G. Proakis, 5th ed. TMH, 2008.
3. Error Correction Coding – Mathematical Methods and Algorithms – Todd K. Moon, Wiley India, 2006.
4. Information Theory, Coding and Cryptography – Ranjan Bose, 2nd Edition, TMH, 2009

HONOURS DEGREE COURSES

VLSI DOMAIN

		L	T	P	M	C
ECHT201	**VLSI Technology and Design**	**3**	**1**	**0**	**100**	**4**

UNIT -I

Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT -II

Layout Design and Tools: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools. Logic Gates & Layouts: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT -III

Combinational Logic Networks: Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT -IV

Sequential Systems: Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT -V

Floor Planning: Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

Advanced Digital System Design

REFERENCES:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC

Press, 2011.

2. Principals of CMOS VLSI Design – N.H. E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.

ECHT202	Advanced Digital System Design	L	T	P	M	C
		3	1	0	100	4

UNIT - I

Processor Arithmetic: Two's Complement Number System - Arithmetic Operations; Fixed point Number System; Floating Point Number system - IEEE 754 format, Basic binary codes.

UNIT - II

Combinational circuits: CMOS logic design, Static and dynamic analysis of Combinational circuits, timing hazards. Functional blocks: Decoders, Encoders, Three-state devices, Multiplexers, Parity circuits, Comparators, Adders, Subtractors, Carry look-ahead adder – timing analysis. Combinational multiplier structures.

UNIT - III

Sequential Logic - Latches and Flip-Flops, Sequential logic circuits - timing analysis (Set up and hold times), State machines - Mealy & Moore machines, Analysis, FSM design using D Flip-Flops, FSM optimization and partitioning; Synchronizers and metastability. FSM Design examples: Vending machine, Traffic light controller, Washing machine.

UNIT - IV

Subsystem Design using Functional Blocks (1) - Design (including Timing Analysis) of different logical blocks of varying complexities involving mostly combinational circuits: ALU, 4-bit combinational multiplier, Barrel shifter, Simple fixed point to floating point encoder, Dual Priority encoder, Cascading comparators

UNIT - V

Subsystem Design using Functional Blocks (2) - Design, (including Timing Analysis) of different logical blocks of different complexities involving mostly sequential circuits:

Pattern (sequence) detector,Programmable Up-down counter, Round robin arbiter with 3 requesters,Process Controller FIFO

TEXT BOOKS:

1. John F. Wakerly, “Digital Design”, Prentice Hall, 3rd Edition, 2002

ECHT203	System On Chip Architecture	L	T	P	M	C
		3	1	0	100	4

UNIT – I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT – II

Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT – III

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation, SOC Memory System, Models of Simple Processor – memory interaction.

UNIT - IV

Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, InstanceSpecific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT – V

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Computer System Design System-on-Chip by Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.

2. ARM System on Chip Architecture – Steve Furber –2 nd Eed., 2000, Addison Wesley Professional.

REFERENCES:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., Springer,2004.

2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM

3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, Kluwer Academic Publishers, 2001.

ECHT204	Design of Fault Tolerant Systems	L	T	P	M	C
		3	1	0	100	4

UNIT - I

Fault Tolerant Design: Basic concepts: Reliability concepts, Failures & faults, Reliability and Failure rate, Relation between reliability and mean time between failure, maintainability and availability, reliability of series, parallel and parallel-series combinational circuits. Fault Tolerant Design: Basic concepts-static, dynamic, hybrid, triple modular redundant system (TMR), 5MR reconfiguration techniques, Data redundancy, Time redundancy and software Redundancy concepts.

UNIT - II

Self Checking circuits & Fail safe Design: Self Checking Circuits: Basic concepts of self checking circuits, Design of Totally self checking checker, Checkers using m out of n codes, Berger code, Low cost residue code. Fail Safe Design: Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, totally self checking PLA design.

UNIT - III

Design for Testability: Design for testability for combinational circuits: Basic concepts of Testability, Controllability and observability, The Reed Muller's expansion technique, use of control and syndrome testable designs. Design for testability by means of scan: Making circuits Testable, Testability Insertion, Full scan DFT technique- Full scan insertion, flip-flop Structures, Full scan design and Test, Scan Architecturesfull scan design, Shadow register DFT, Partial scan methods, multiple scan design, other scan designs.

UNIT – IV

Logic Built-in-self-test: BIST Basics-Memory-based BIST,BIST effectiveness, BIST types, Designing a BIST, Test Pattern Generation-Engaging TPGs, exhaustive counters, ring counters, twisted ring counter, Linear feedback shift register, Output Response Analysis-Engaging ORA's, One's counter, transition counter, parity checking, Serial LFSRs, Parallel Signature analysis, BIST architectures-BIST related terminologies, A centralized and separate Board-level BIST architecture, Built-in evaluation and self test(BEST), Random Test socket (RTS), LSSD On-chip self test, Self – testing using MISR and SRSG, Concurrent BIST, BILBO, Enhancing coverage, RT level BIST designCUT design, simulation and synthesis, RTS BIST insertion, Configuring the RTS BIST, incorporating configurations in BIST, Design of STUMPS, RTS and STUMPS results.

UNIT – V

Standard IEEE Test Access Methods: Boundary Scan Basics, Boundary scan architecture- Test access port, Boundary scan registers, TAP controller, the decoder unit, select and other units, Boundary scan Test Instructions-Mandatory instructions, Board level scan chain structure-One serial scan chain, multiple-scan chain with one control test port, multiple-scan chains with one TDI,TDO but multiple TMS, Multiple-scan chain, multiple access port, RT Level boundary scan-inserting boundary scan test hardware for CUT, Two module test case, virtual boundary scan tester, Boundary Scan Description language.

TEXTBOOKS:

1. Parag K. Lala, "Fault Tolerant & Fault Testable Hardware Design", 1984, PHI

2. Zainalabedin Navabi, "Digital System Test and Testable Design using HDL models and Architectures", Springer International Edition.

REFERENCES:

1. Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, "Digital Systems Testing and Testable Design", Jaico Books

2. Bushnell & Vishwani D. Agarwal, "Essentials of Electronic Testing", Springer.

3. Alfred L. Crouch, "Design for Test for Digital IC's and Embedded Core Systems", 2008, Pearson Education.