



## Laboratory Report # 1

Name: Christian Jay Y. Gallardo,

Date Completed: 8/22/2025

Laboratory Exercise Title: Design Flow of Digital Systems

### Target Course Outcomes:

**CO1:** Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

**CO2:** Verify the functionality of HDL-based components through design verification tools.

### Exercise C :

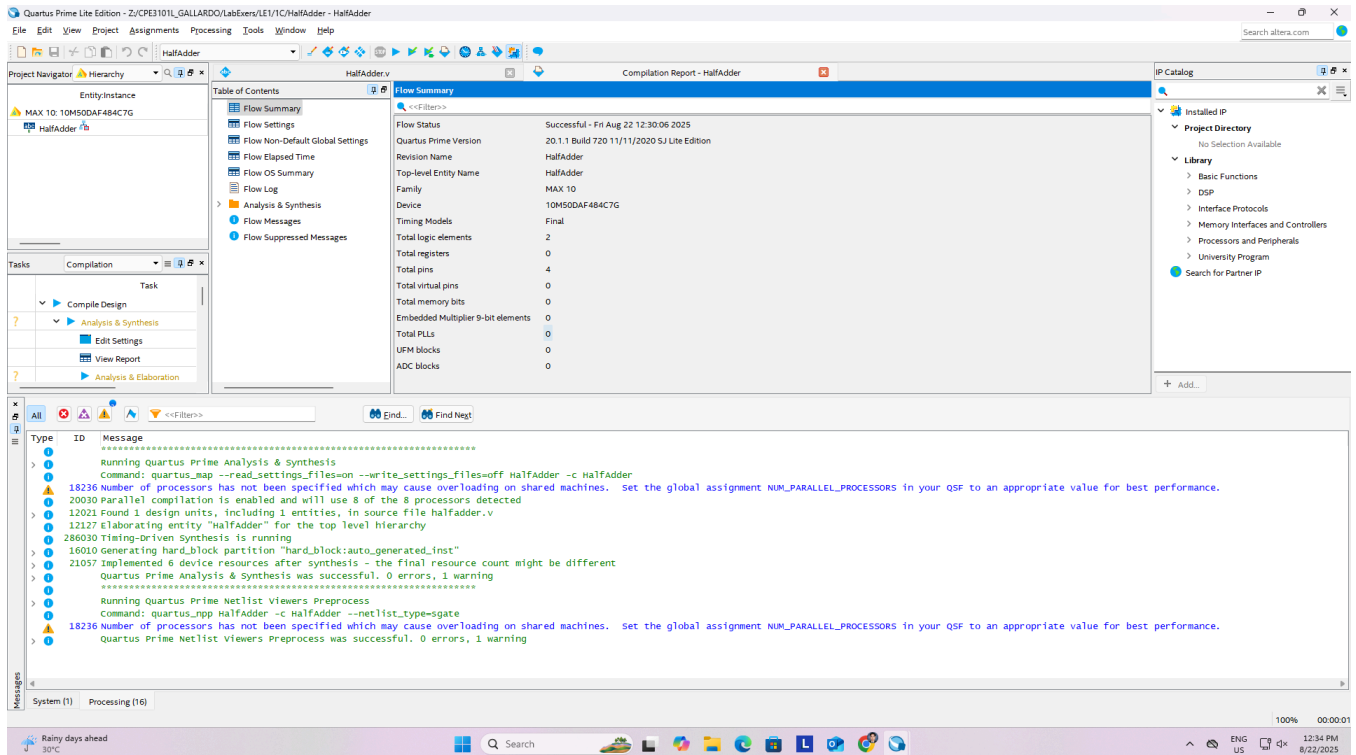
*Briefly summarize what was being performed or designed in this exercise. Include the following, whenever applicable:*

- *Entity diagram, I/O ports, truth table/s, methods (modeling type and other specifications given in the problem)*
- *Necessary solutions (data in tables, answers to questions, Boolean functions, logic/block/state diagrams, etc., if any)*
- *Clear screenshot showing the compilation report (Flow Summary)*
- *Clear screenshot of synthesis results (Message window of Quartus Prime, showing successful synthesis with errors/warnings)*
- *Clear screenshot of verified designs (RTL View schematic diagram)*
- *Clear screenshots of simulation waveform/s with annotations*
- *Other screenshots and information specified in Laboratory Exercise guide*

To design, analyze, and synthesize a Half Adder circuit using Verilog HDL, and verify its structure through RTL schematic and compilation reports.

**Table 1.** Half Adder Truth Table

Input		Output	
x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



**Figure 1. Compilation Report for the Flow Summary**

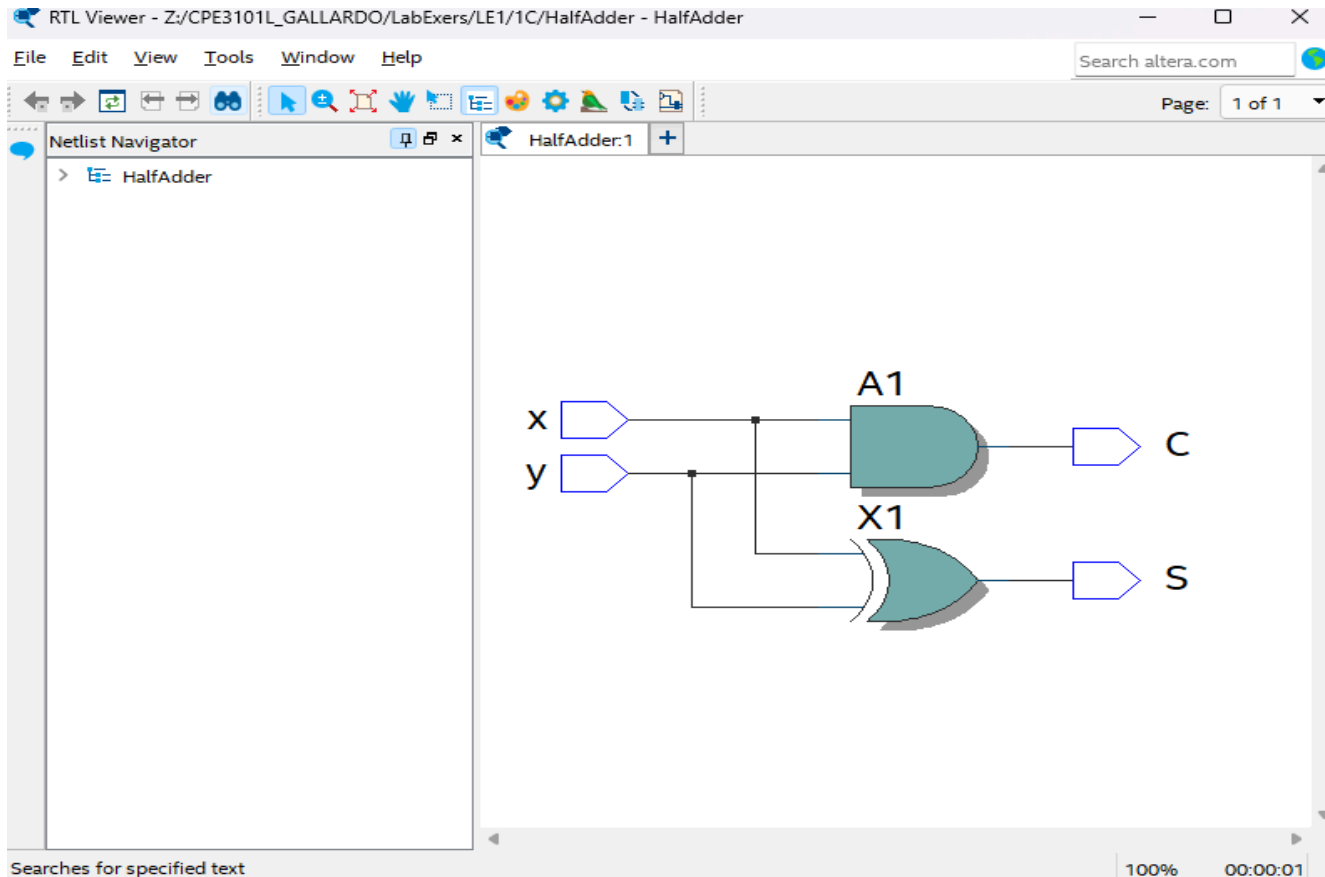


Figure 2. Schematic Diagram of Synthesized Circuit

```
HalfAdder.v
1 // Name: Christian Jay Y. GALLARDO
2 // Date: 8/22/2025
3 // Schedule: CPE 3101L 10:30AM - 1:30AM SAT
4 // Detail: verilog HDL code for a half adder circuit
5
6 module HalfAdder (x, y, C, S);
7
8     input    x, y;
9     output   C, S;
10
11     and     A1 (C, x, y);
12
```

Figure 3. Verilog HDL Design Entry



New Project Wizard

### Summary

When you click Finish, the project will be created with the following settings:

Project directory:	Z:\CPE3101L_GALLARDO\LabExers\LE1\1C
Project name:	HalfAdder
Top-level design entity:	HalfAdder
Number of files added:	0
Number of user libraries added:	0
Device assignments:	
Design template:	n/a
Family name:	MAX 10 (DA/DF/DC/SA/SC)
Device:	10M02DCU324A6G
Board:	n/a
EDA tools:	
Design entry/synthesis:	<None> (<None>)
Simulation:	<None> (<None>)
Timing analysis:	()
Operating conditions:	
Core voltage:	1.2V
Junction temperature range:	-40-125 °C

< Back   Next >   **Finish**   Cancel   Help

Figure 4. Project Settings Summary