Laboratory Report #7

Name: Christian Jay Y. Gallardo **Date Completed:** 20/12/2025

Laboratory Exercise Title: Finite State Machines (FSMs)

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

Exercise 7A:

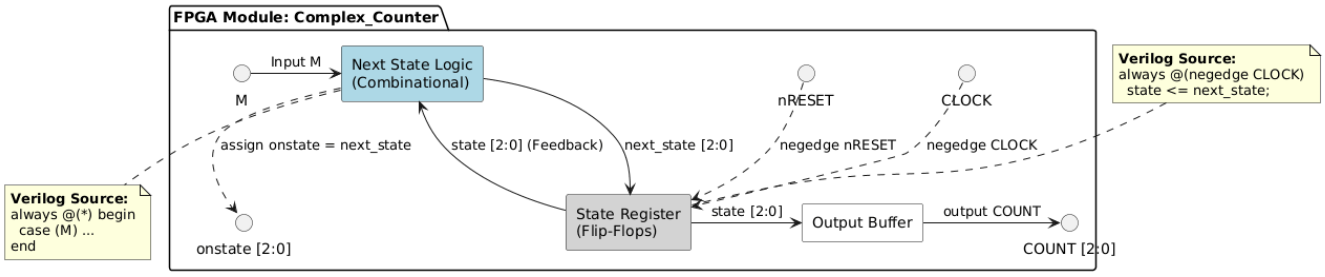

Figure 1: Moore State Machine

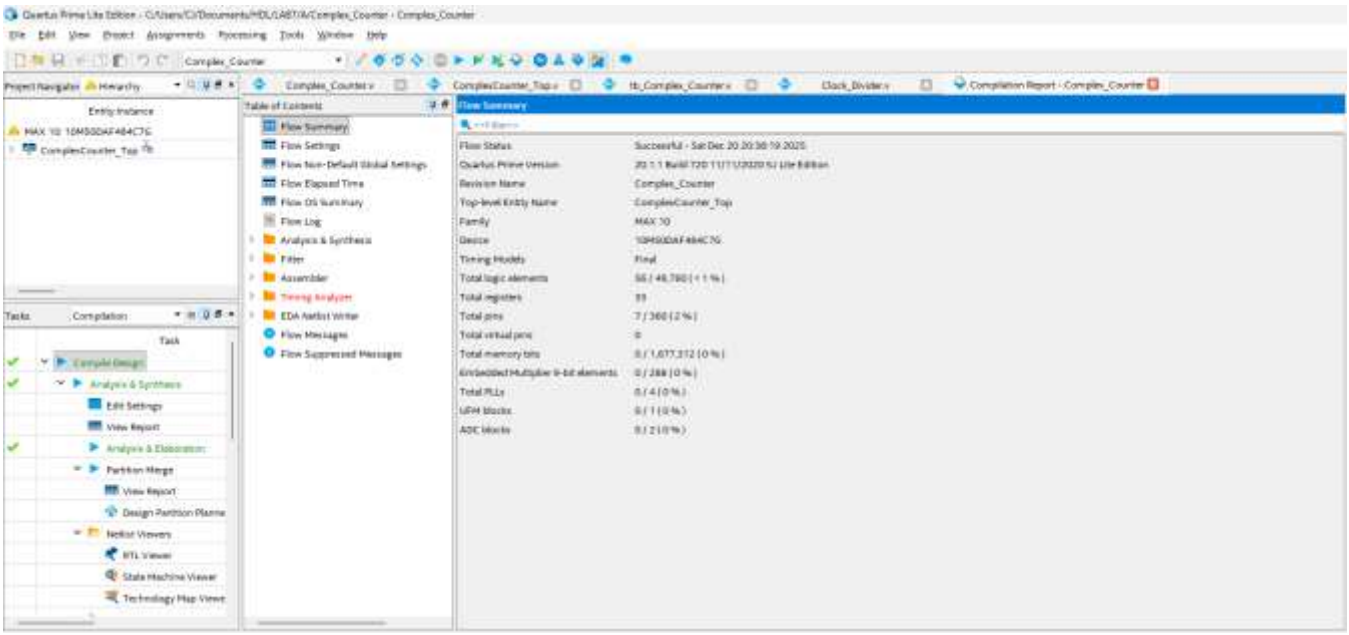

Figure 2: Compilation Report of Complex Counter

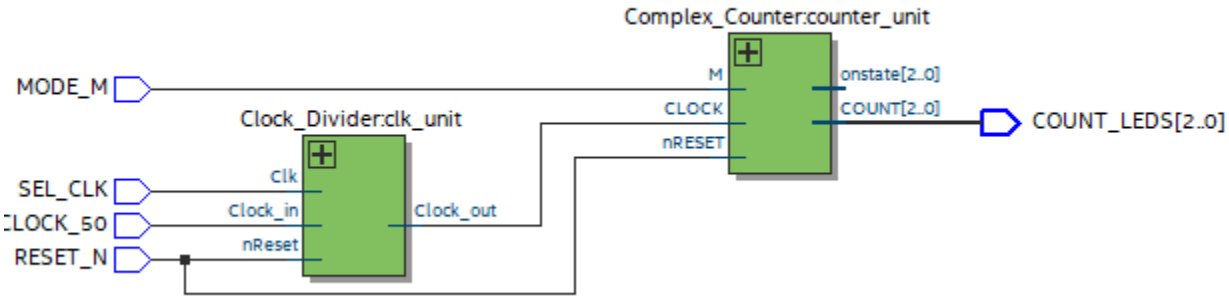

Figure 3: RTL Schematic of Complex Counter

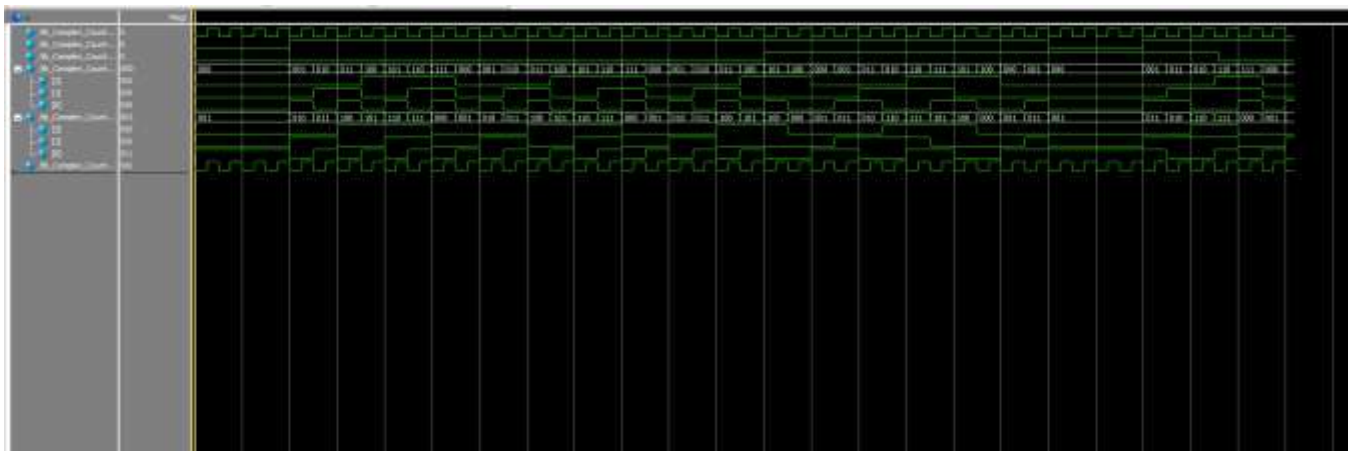

Figure 4: ModelSim Waveform of Complex Counter

- Initialization and Synchronous Reset: The simulation begins with inRESET held at logic 0. As per the requirements, the system remains in the 000 state and only releases to begin counting upon the first negative clock edge after inRESET transitions to logic 1.
- Binary Mode Execution (M=0): When the mode input iM is set to 0, the counter follows a standard 3-bit binary sequence: 000 → 001 → 010 → 011 → 100 → 101 → 110 → 111.
- Gray Code Mode Execution (M=1): Upon switching iM to 1, the counter shifts to the Gray code sequence: 000 → 001 → 011 → 010 → 110 → 111 → 101 → 100.
- Dynamic Mode Switching: The waveform specifically captures the transition behavior defined in the "Example of Valid I/O Behavior" table. For instance, if the current state is 010 in binary mode and M switches to 1, the next state correctly transitions to 110 (the next state in the Gray sequence) rather than continuing the binary count to 011.
- Moore FSM Output Stability: The oCOUNT output is clearly shown to be synchronized with the internal state registers, updating only at the falling edge of the clock (iCLOCK), which confirms the Moore architecture where the output depends solely on the current state.

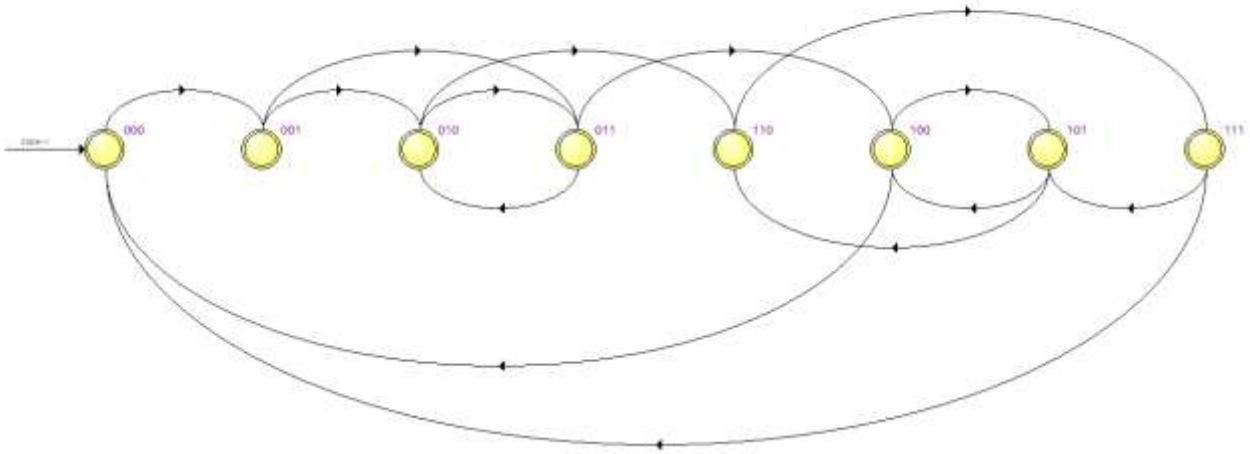

Figure 5: State Machine of Complex Counter

CurrentState (Binary)	M	NextState (Binary)	OutputCount (Decimal/Binary)
0	0	1	0 (000)
1	0	10	1 (001)
10	0	11	2 (010)
11	0	100	3 (011)
100	0	101	4 (100)
101	0	110	5 (101)
110	0	111	6 (110)
111	0	0	7 (111)
0	1	1	0 (000)
1	1	11	1 (001)
11	1	10	3 (011)
10	1	110	2 (010)
110	1	111	6 (110)
111	1	101	7 (111)
101	1	100	5 (101)
100	1	0	4 (100)

Figure 6: State Table of Complex Counter

Exercise 7B:

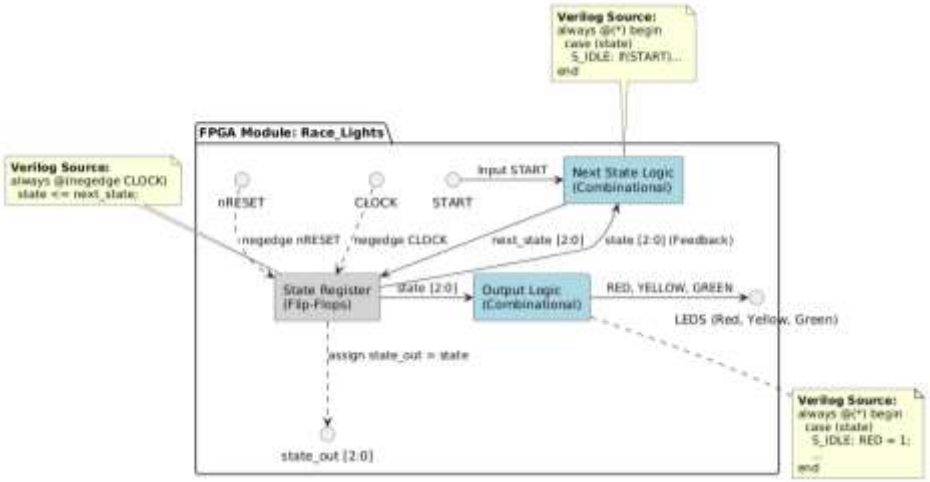

Figure 7: Mealy State Machine

Figure 8: Compilation Report of Race Lights

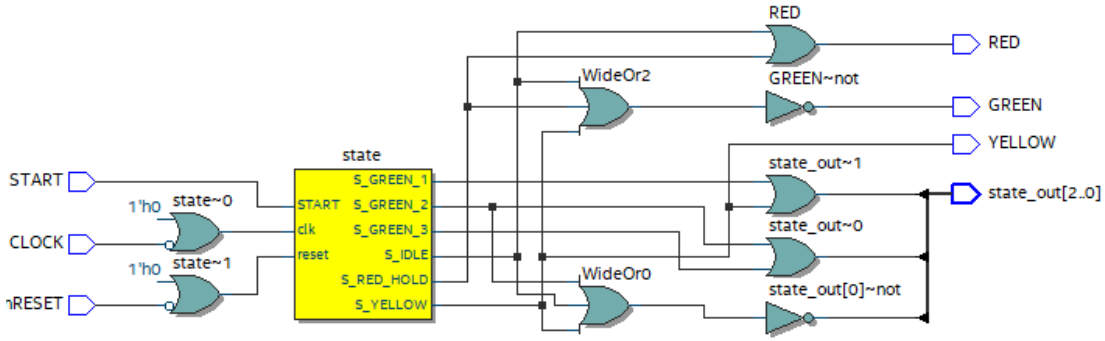

Figure 9: RTL Schematic of Race Lights

CurrentState (Symbol/Binary)	Input (START)	NextState (Symbol/Binary)	Output Lights (RED, YELLOW, GREEN)
S_IDLE (000)	0	S_IDLE (000)	1 0 0 (Red ON)
S_IDLE (000)	1	S_RED_HOLD (001)	1 0 0 (Red ON)
S_RED_HOLD (001)	X	S_YELLOW (010)	1 0 0 (Red ON)
S_YELLOW (010)	X	S_GREEN_1 (011)	0 1 0 (Yellow ON)
S_GREEN_1 (011)	X	S_GREEN_2 (100)	0 0 1 (Green ON)
S_GREEN_2 (100)	X	S_GREEN_3 (101)	0 0 1 (Green ON)
S_GREEN_3 (101)	X	S_IDLE (000)	0 0 1 (Green ON)

Figure 10: State Table of Race Lights

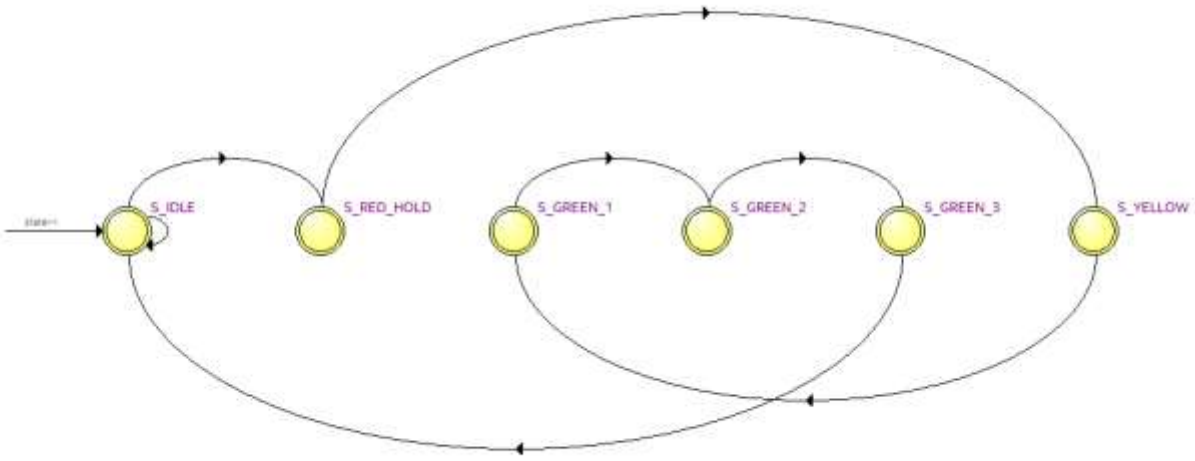

Figure 11: State Machine of Race Lights

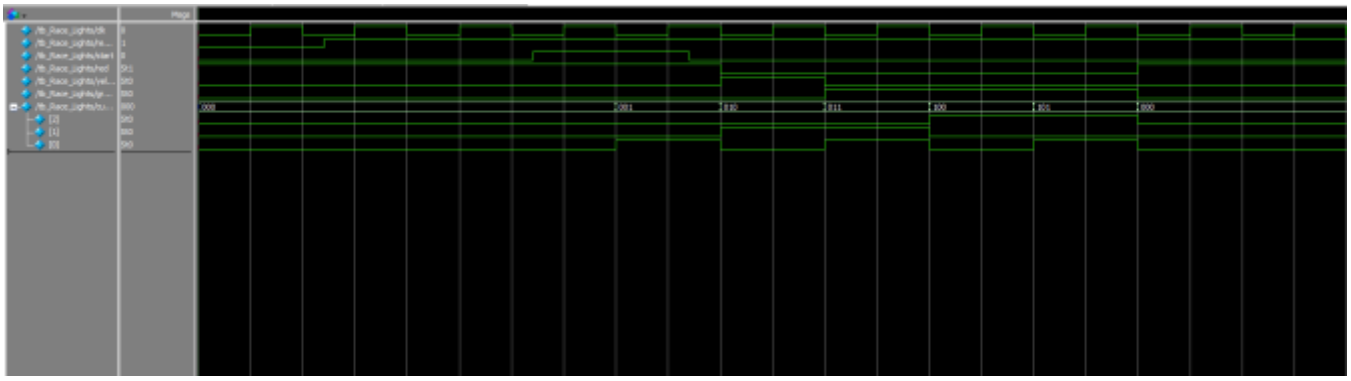

Figure 12: ModelSim Waveform of Race Lights

- Initialization and Idle State: The simulation begins with reset_n held at logic 0. As per the requirements, the system remains in the S_IDLE state (000) with the red output signal asserted high, establishing the default stop condition until the reset is released and the start input is detected.

- Start Sequence and Red Hold: Upon the activation of the start signal, the FSM transitions to the S_RED_HOLD state (001) at the next falling edge of the clock. In this state, the red output remains active for one full clock cycle, satisfying the requirement for the red light to remain illuminated for an additional second after the button press.

- S_YELLOW (010), causing the red signal to drop low and the yellow signal to drive high for exactly one clock cycle. The sequence immediately proceeds to the green light phase, starting at state S_GREEN_1 (011).

- Timing Verification: The waveform explicitly demonstrates the required timing durations. The green output signal remains high for three consecutive clock cycles as the state progresses through 011, 100, and 101, fulfilling the three-second duration requirement before the light turns off.

- Return to Reset: After the third second of the green sequence completes at state 101, the system automatically transitions back to the S_IDLE state (000). At this point, the green signal is de-asserted and the red signal is re-asserted, confirming the controller has returned to its initial reset state ready for the next start command.