Laboratory Report #6

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Laboratory Exercise Title: Behavioral Modeling of Sequential Circuits: Clock Dividers and Digital Systems

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

Exercise 6C:

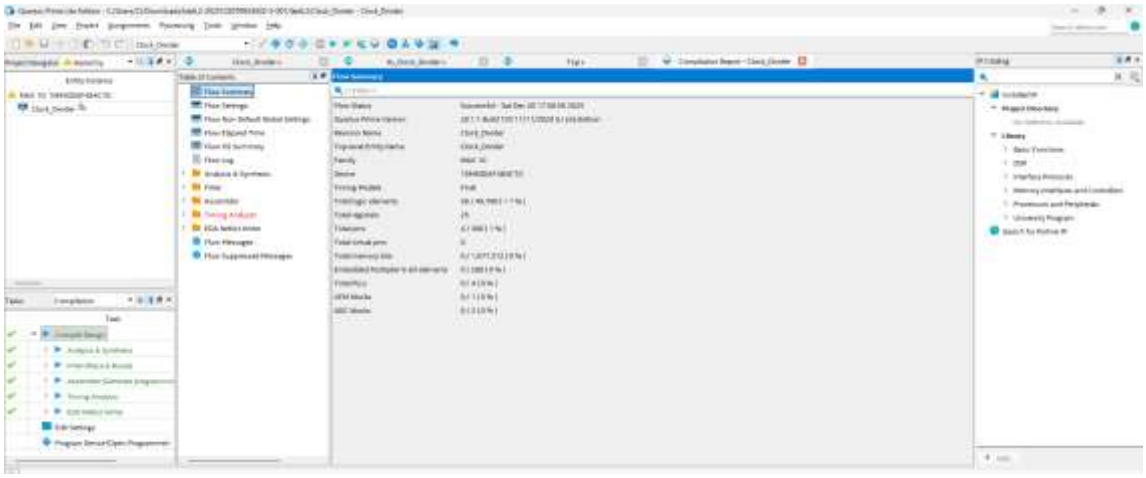

Figure 1: Compilation Report of Clock Divider

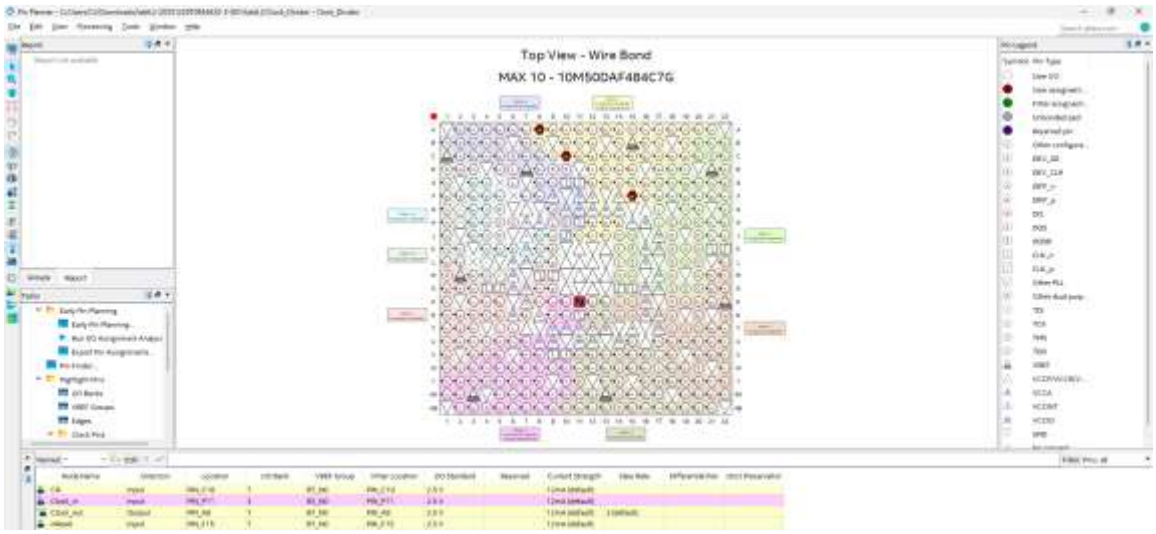

Figure 2: Pin Setup Of Clock Divider

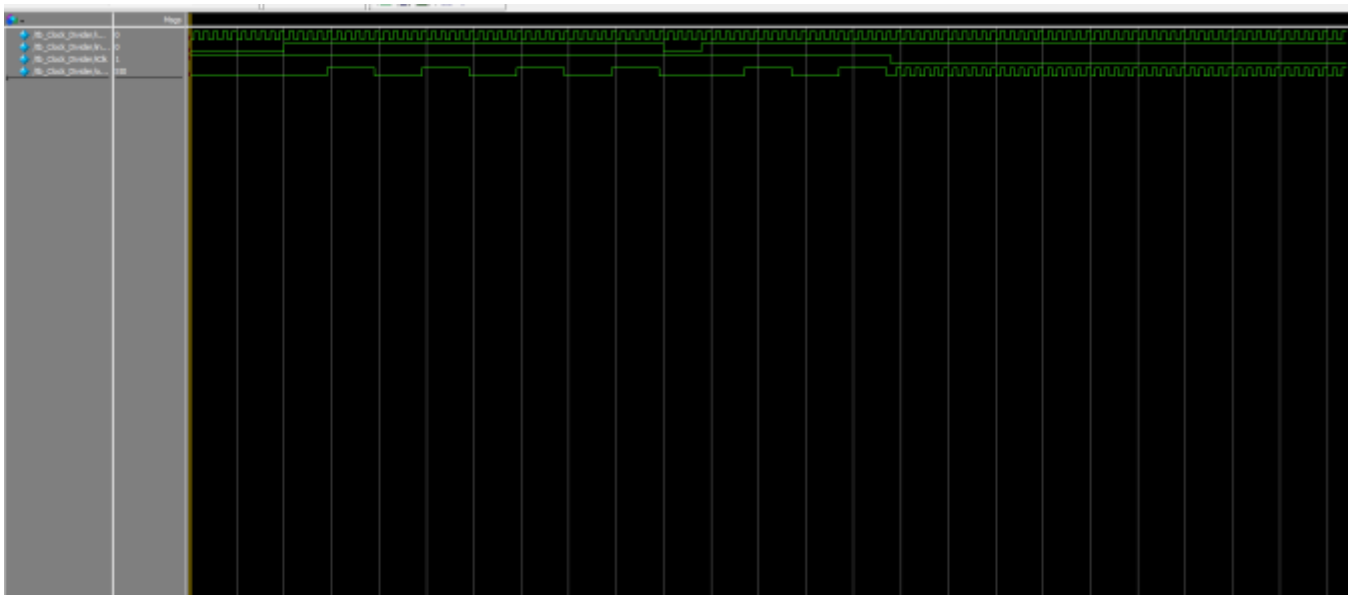

Figure 3: Waveform Simulation of Clock Divider

- Phase A: Asynchronous Reset: At the start of the simulation, the inReset signal is held low (active), which forces the oClock_out to remain at a constant logic level despite the rapid toggling of the input source clock iClock_in.

- Phase B & C: Functional Division: Once inReset is pulled high, the internal counter begins its cycle. The output oClock_out begins to toggle at a rate significantly slower than the input—specifically a 10x reduction based on the simOldHz and simNewHz parameters. The waveform shows clear square wave cycles where each period of the output encompasses ten periods of the input source. A brief pulse of inReset to 0 in Phase C demonstrates the circuit's ability to immediately halt and re-synchronize the division process.

- Phase D: Bypass Mode and Mode Switching: The simulation effectively tests the iClk mux control. When iClk is high, the circuit outputs the divided (slower) clock. When iClk is transitioned to 0, the waveform shows the oClock_out bypassing the divider logic to directly mirror the high-frequency iClock_in signal. This phase concludes by switching back to the divided mode, showing a seamless return to the 10x slower toggling rate before the simulation finishes.

Exercise 6D:

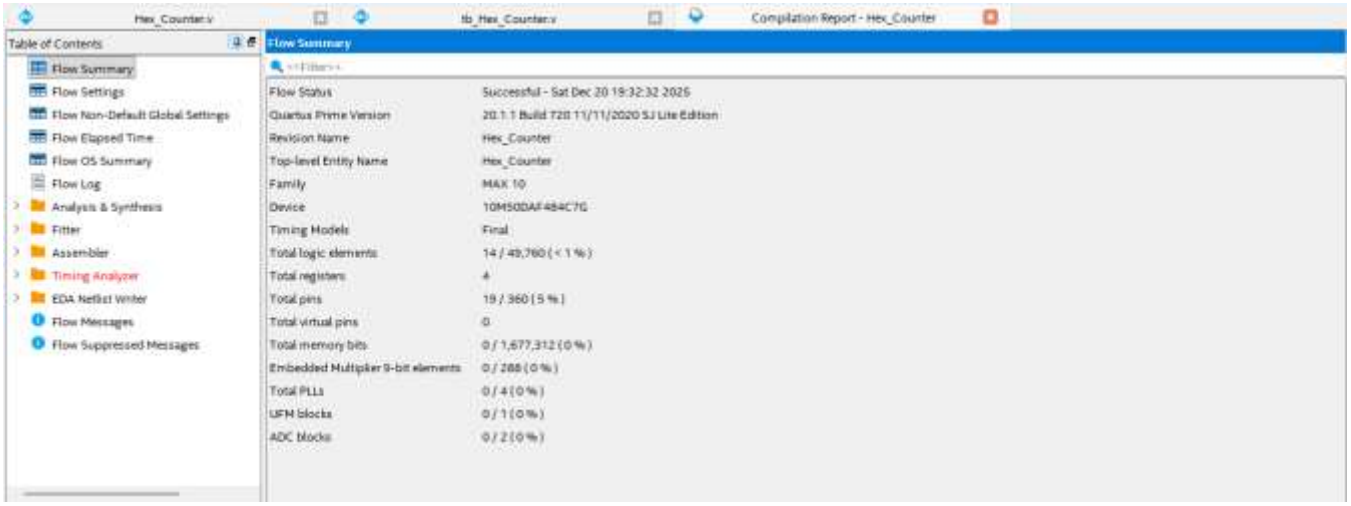

Figure 4: Compilation Report of Hex Counter

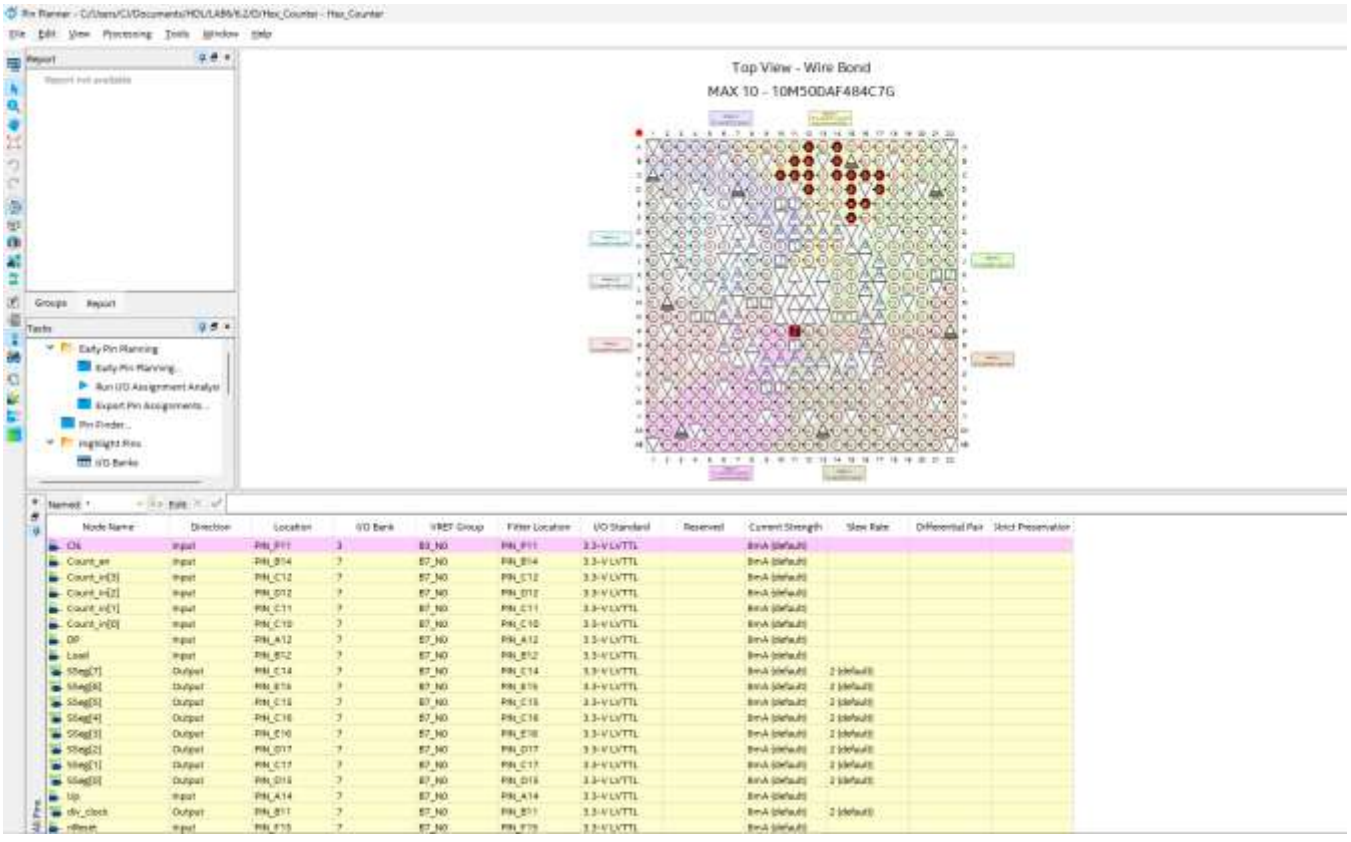

Figure 5: Pin Setup of Hex Counter

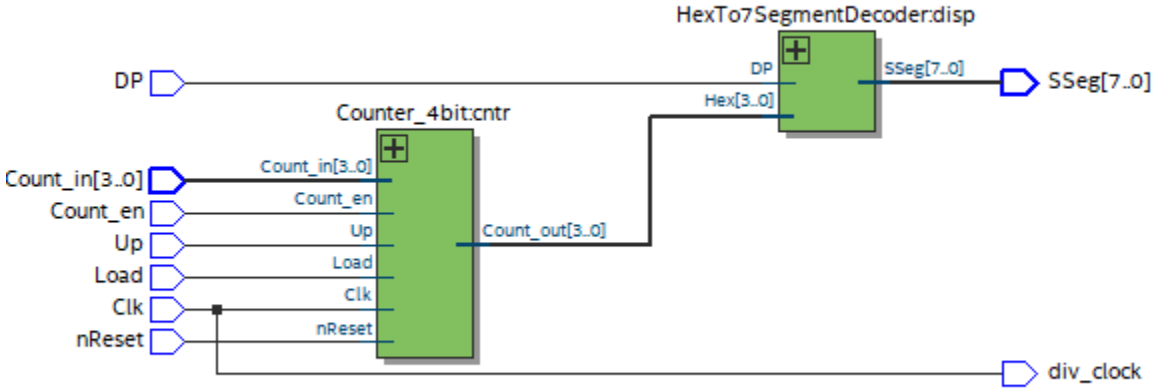

Figure 6: RTL Block Diagram of Hex Counter

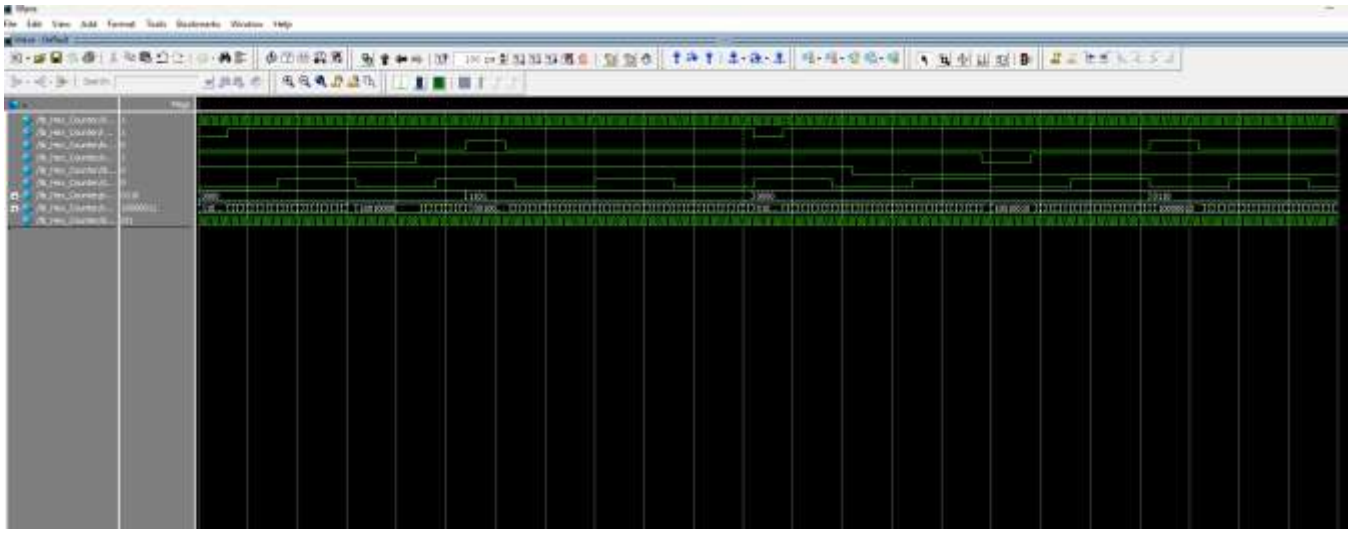

Figure 7: Waveform Simulation of Hex Counter

- Initialization and Reset Logic: The simulation starts with a clear state where rst_n is asserted, ensuring the internal counter and the seven_seg_out begin at a known zero value.
- Sequential Counting: As the system clock cycles, the counter increments from 0000 through 0101. The seven_seg_out bus simultaneously updates to reflect the active-low patterns required to display these digits on a hardware display.
- Parallel Data Loading: The functionality of the load_cmd signal is clearly demonstrated when it transitions high, causing the counter to immediately jump to the input value 1101 (Hex 'D'). The 7-segment output follows this change instantly, transitioning to the bit pattern for a 'D' character.
- Directional Control: When the dir_up signal is toggled to logic 0, the counter reverses its operation. The waveform shows the binary values and the 7-segment patterns successfully decrementing (e.g., from 0011 to 0010).

- Decimal Point and Enable: The independent toggling of the dot_pt (DP) signal is visible, showing it can be controlled without affecting the primary numerical count. Additionally, the enable signal successfully pauses the count, holding both the binary state and the 7-segment pattern steady until counting is resumed.