Final Exam (Take-Home-Task)

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

CO3: Design HDL-based digital systems following the design flow for FPGA implementation.

Vending Machine Controller (VMC)

Design a vending machine controller that is able to dispense 3 items with the following prices, respectively: Php 3.00, Php 5.00 and Php 12.00. After the **START** is initiated, the machine allows the user to select a particular item by using **SELECT** to traverse through the available items. Every time **SELECT** is asserted an item is selected/highlighted, one at a time, as indicated by a light emitting diode (**ITEM**) assigned to each item. An **OK** signal will allow the user to proceed to payment. The machine can accept the following denominations: Php 1.00, Php 5.00 and Php 10.00. It will continue accepting payment until the paid amount is at least the same amount as that of the selected item. Any payment made after which will be rejected by the machine. Another assertion of **OK**, after the payment has been made, will dispense the selected item if the payment is enough. The machine provides change when the user overpays or cancels the purchase after a payment has already been made.

Inputs	Outputs
CLOCK (negative-edged) **nRESET** (asynchronous active low) **START** (synchronous active high) **OK** (synchronous active high) **CANCEL** (asynchronous active high) **SELECT** (synchronous active high)	**ITEM** indicator **DISPENSE** actuator **C1** Php 1.00 change actuator **C5** Php 5.00 change actuator **C10** Php 10.00 change actuator

I. Create the Verilog Project and compile the required items below in a PDF file using the filename format VMC_{*FamilyName1*}_{*FamilyName2*}pdf. Format the contents of the document according to the following:

1. **Drawing of the State Diagram and Table of States including the assumptions needed per state.**
2. **Verilog HDL design entry:**
   - **Project Folder: VMC**
   - **Module Name: VMC**
   - Include your names on the Verilog file placed in comments.
   - Add comments to the Verilog file describing the function of the module.
   - Screenshot of the Verilog file labeled as **VMC_DesignEntry.**
3. **Synthesized results showing the Compilation Report (Flow Summary) window:**
   - Screenshot of the entire Quartus Prime window showing 0 errors, and labeled as **VMC_Synthesis.**
4. **RTL Viewer result:**
   - Provide screenshots of the entire window of RTL Viewer diagram showing the project path and file name. Label it as **VMC_RTL.**
5. **Synthesized State Machine with its transition table.**
   - Provide screenshots of the synthesized state diagram. Label it as **VMC_StateMachine**.
6. **Verilog HDL code of your testbench file**
   - **Module Name: tb_VMC**
   - For test inputs, consider sample test cases that show the different states and input port functions of the design.
   - Include your names on the file placed in comments.

- Add comments to the Verilog file describing the function of the module.
- Take a clear screenshot of your Verilog file. Label it as **VMC_TBFile.**

7. **ModelSim Generated Simulation Waveform**
   - Provide a clear screenshot of the Wave window only. Label it as **VMC_TBWaveform.**
   - The waveforms must show all input combinations provided in the testbench.
   - Annotate the waveforms accordingly for easy verification of the results.

II. Implement the design in an FPGA board and provide a video demonstration (demo) of the design following the guidelines below:

1. To be able to use the Intel DE10-Lite FPGA Boards, you may come to the Digital and Microprocessors Laboratory (DML) anytime, from Wednesday, Dec. 17, to Friday, Dec. 19, between 8:00am-4:00pm, and perform the task using the boards.
2. Record a video demo that exhibits the various test inputs and cases that show the different states of the design.
3. Each member of the group must have a part in the demo.
4. Limit the video length to five (5) minutes only.

III. Submit a compressed or zipped file, using the filename format VMC_{*FamilyName1*}_{*FamilyName2*}, that contains the items below:

1. **Project Folder: VMC**
2. **PDF File: VMC_{*FamilyName1*}_{*FamilyName2*}.pdf**
3. **Demo Video:** ***(****using a common video format****)***
   Note: If the video file size is too large to be uploaded in Canvas, you may upload the recorded video to a video sharing platform such as Youtube or a file storage platform such as Google Drive. Place the link to the video in a text file named "link" (link.txt) and include the file in the submission in place of the actual video file. Make sure that the video is publicly accessible.