Laboratory Report #6

Name: Christian Jay Y. Gallardo **Date Completed:** 20/12/2025

Laboratory Exercise Title: Behavioral Modeling of Sequential Circuits: An Introduction

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

Exercise 6A:

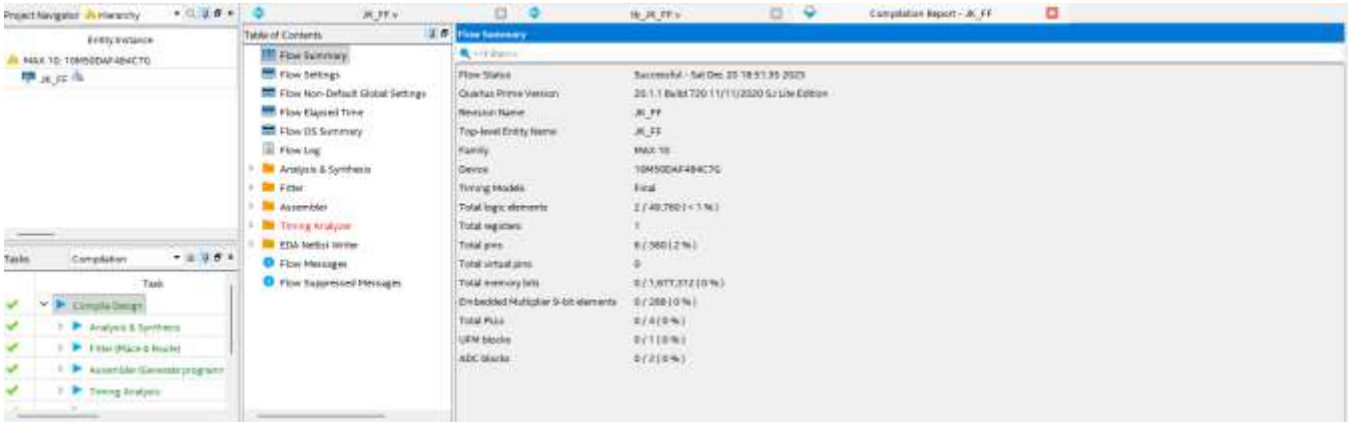

Fig 1: Compilation Report Of JK Flip-Flop

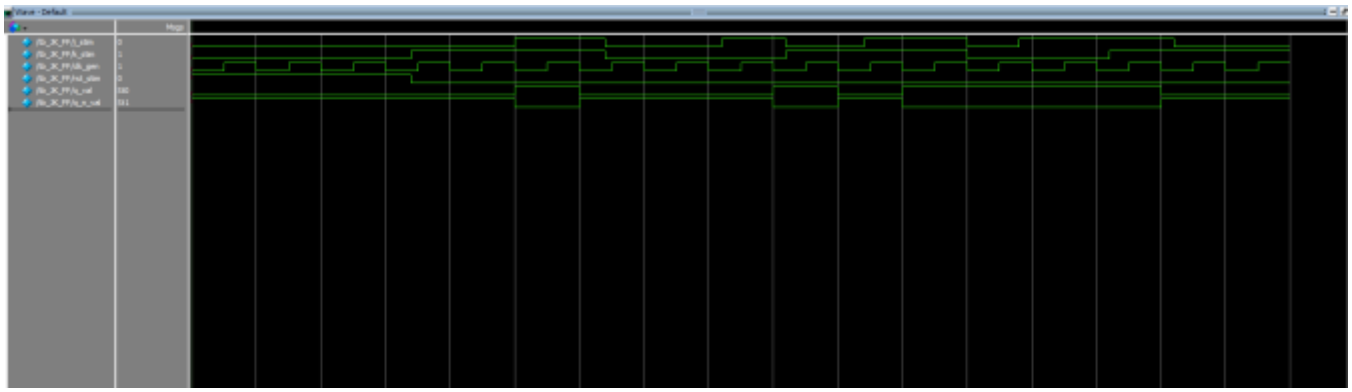

Fig 2: Waveforms of JK Flip-Flop

- Asynchronous Reset: At the start of the simulation, the rst_stim (reset) signal is asserted high, which immediately forces the output q_val to 0 and its complement q_n_val to 1.

- Set and Reset States: When the j_stim input is high and k_stim is low, the flip-flop enters the "Set" state, driving q_val to 1 on the next falling edge of the clock (clk_gen). Conversely, when j_stim is low and k_stim is high, the output is "Reset" back to 0.

- Toggle Mode: The waveform demonstrates the "Toggle" functionality when both j_stim and k_stim are held at logic 1. In this mode, the output q_val flips its state (from 0 to 1 or 1 to 0) on every active clock edge.

- Hold State: When both inputs are at logic 0, the waveform shows the outputs remaining stable, effectively storing the previous bit of information.

Exercise 6B:

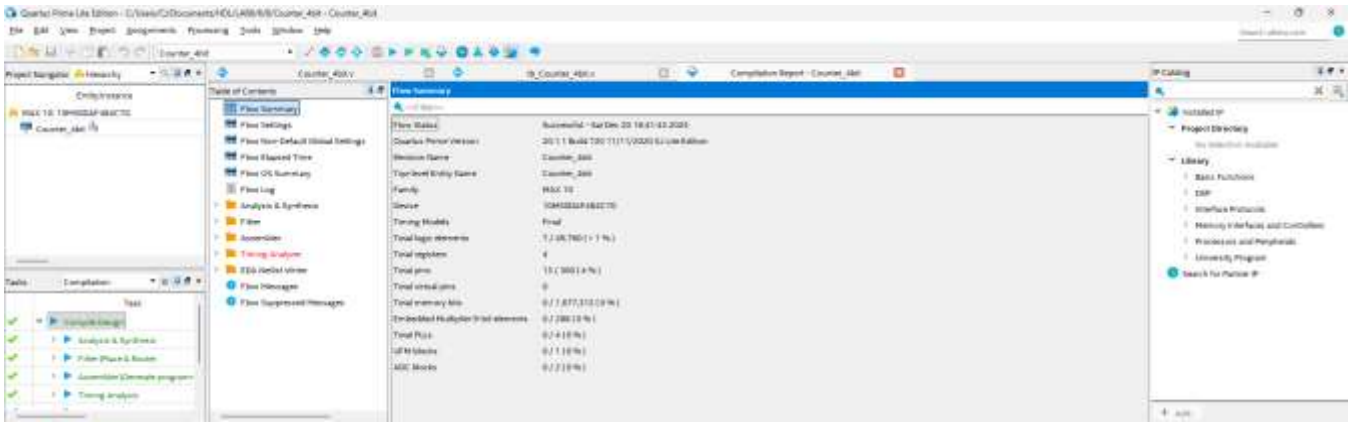

Fig 3: Compilation Report Of Counter 4Bit

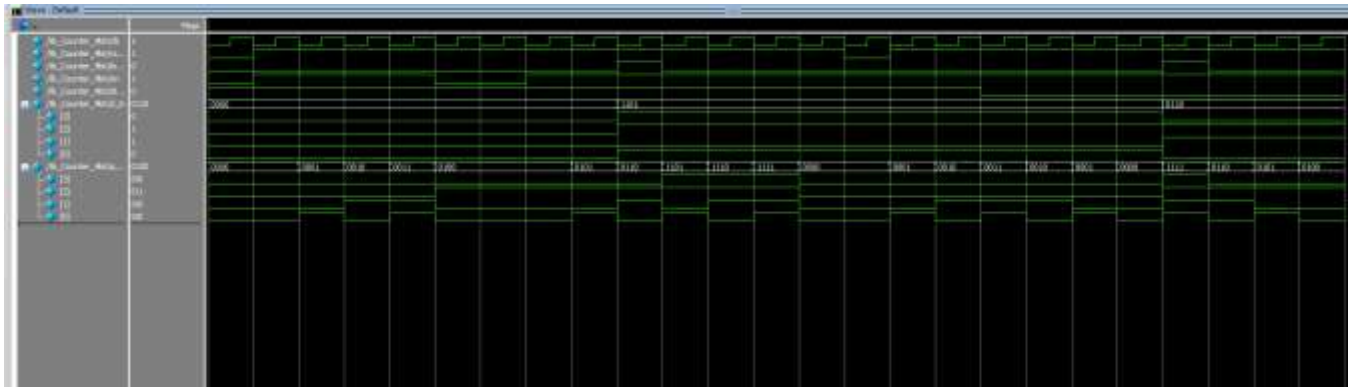

Fig 4: Waveforms of Counter 4Bit

- Initialization and Counting: The simulation begins with an asynchronous reset (where rst_n drops low), clearing the output to 0000. Once en and dir_up are set high, the counter increments on each falling edge of the clock (clk), as seen in the progression from 0000 to 0101.

- Parallel Load: Mid-simulation, the load_en signal is pulsed while d_in is set to 1101. The waveform shows the counter immediately jumping to 1101 (13 in decimal), bypassing the normal sequence.

- Direction Change: Later in the timeline, the direction bit (di...) switches to 0, causing the counter to begin decrementing (e.g., from 0000 down to 1111 and 1110).

- Enable Logic: The waveform also demonstrates the "Pause" functionality; when en is pulled low, the output q_out remains stable at its last value despite the clock continuing to cycle, proving the clock enable logic is robust.