Laboratory Report #_1__

Name: Christian Jay Y. Gallardo, **Date Completed: 8/22/2025**

Laboratory Exercise Title: Design Flow of Digital Systems

Target Course Outcomes:

CO1: Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

CO2: Verify the functionality of HDL-based components through design verification tools.

Exercise _C_:

Briefly summarize what was being performed or designed in this exercise. Include the following, whenever applicable:

- *Entity diagram, I/O ports, truth table/s, methods (modeling type and other specifications given in the problem)*
- *Necessary solutions (data in tables, answers to questions, Boolean functions, logic/block/state diagrams, etc., if any)*
- *Clear screenshot showing the compilation report (Flow Summary)*
- *Clear screenshot of synthesis results (Message window of Quartus Prime, showing successful synthesis with errors/warnings)*
- *Clear screenshot of verified designs (RTL View schematic diagram)*
- *Clear screenshots of simulation waveform/s with annotations*
- *Other screenshots and information specified in Laboratory Exercise guide*

To design, analyze, and synthesize a Half Adder circuit using Verilog HDL, and verify its structure through RTL schematic and compilation reports.

Table 1. Half Adder Truth Table

Input		Output	
x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

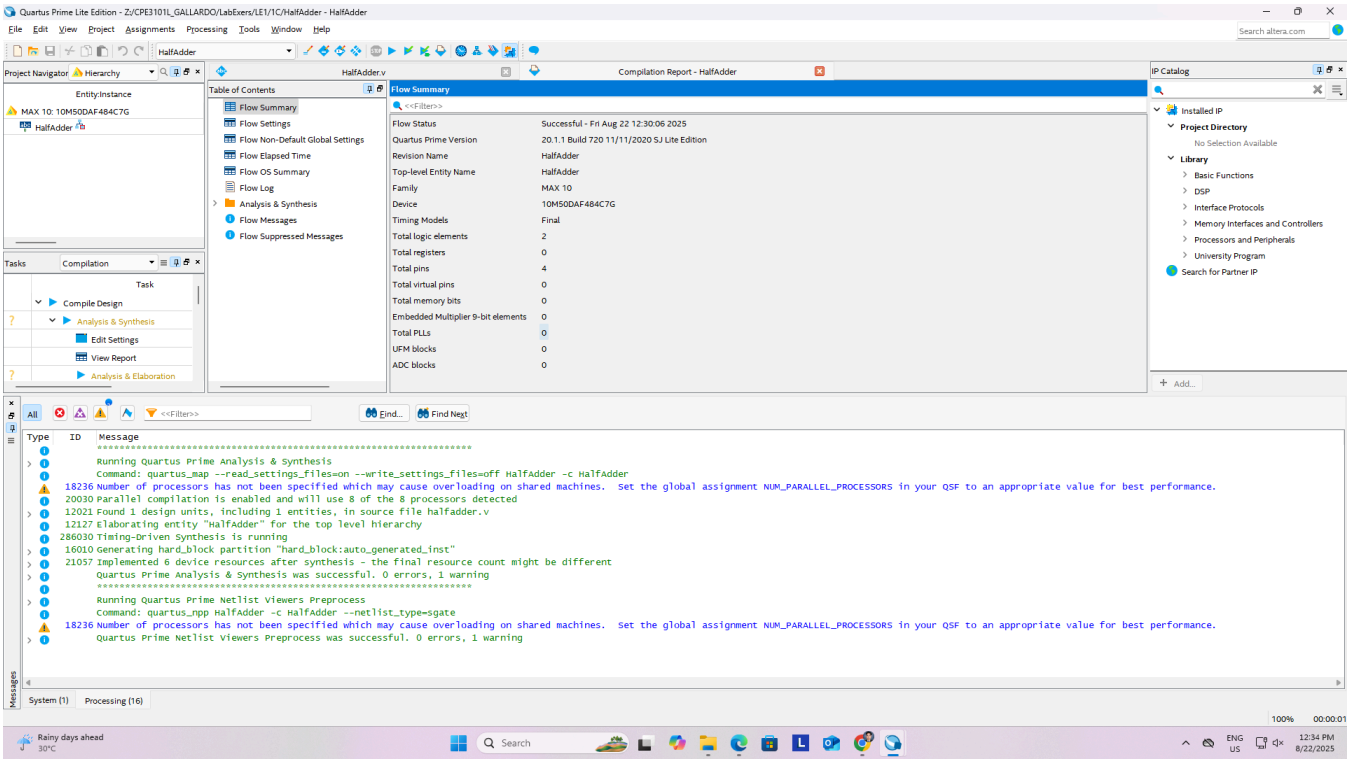

Figure 1. Compilation Report for the Flow Summary

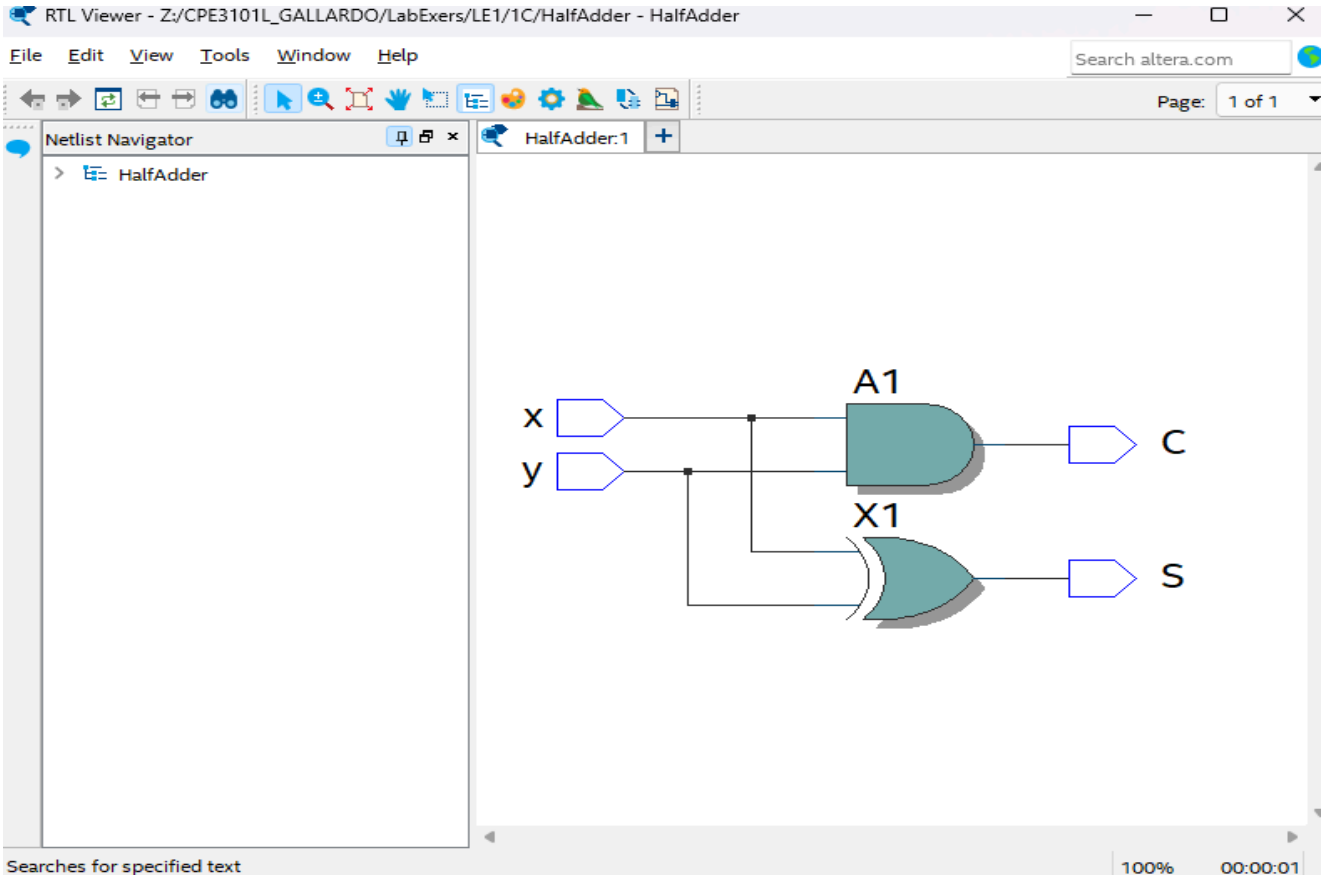

Figure 2. Schematic Diagram of Synthesized Circuit

HalfAdder.v

```
1   // Name: Christian Jay Y. GALLARDO
2   // Date: 8/22/2025
3   // Schedule: CPE 3101L 10:30AM - 1:30AM SAT
4   // Detail: Verilog HDL code for a half adder circuit
5
6   module HalfAdder (x, y, C, S);
7
8       input    x, y;
9       output   C,S;
10
11      and      A1 (C, x, y);
```

Figure 3. Verilog HDL Design Entry

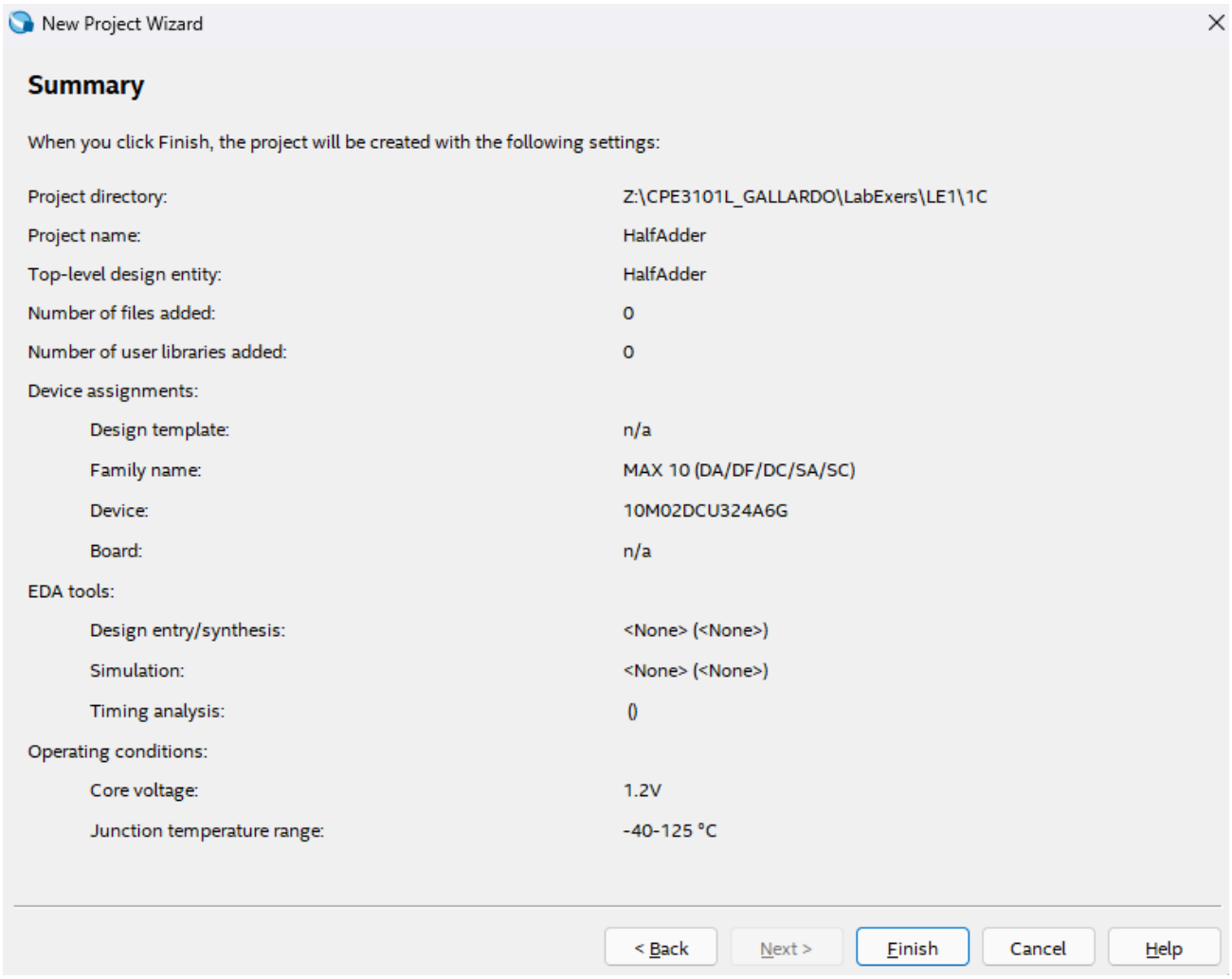

Figure 4. Project Settings Summary