Department of Computer Engineering
Digital Hardware Systems
CpE 3104 - Microprocessors

Laboratory Exercise #5
I/O Interfacing (Address Decoding and I/O Ports)

Laboratory Exercise No.:	5	**Date Performed:**	11/9/2025
Laboratory Exercise Title:	**I/O Interfacing (Address Decoding and I/O Ports)**		
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Activity #1:

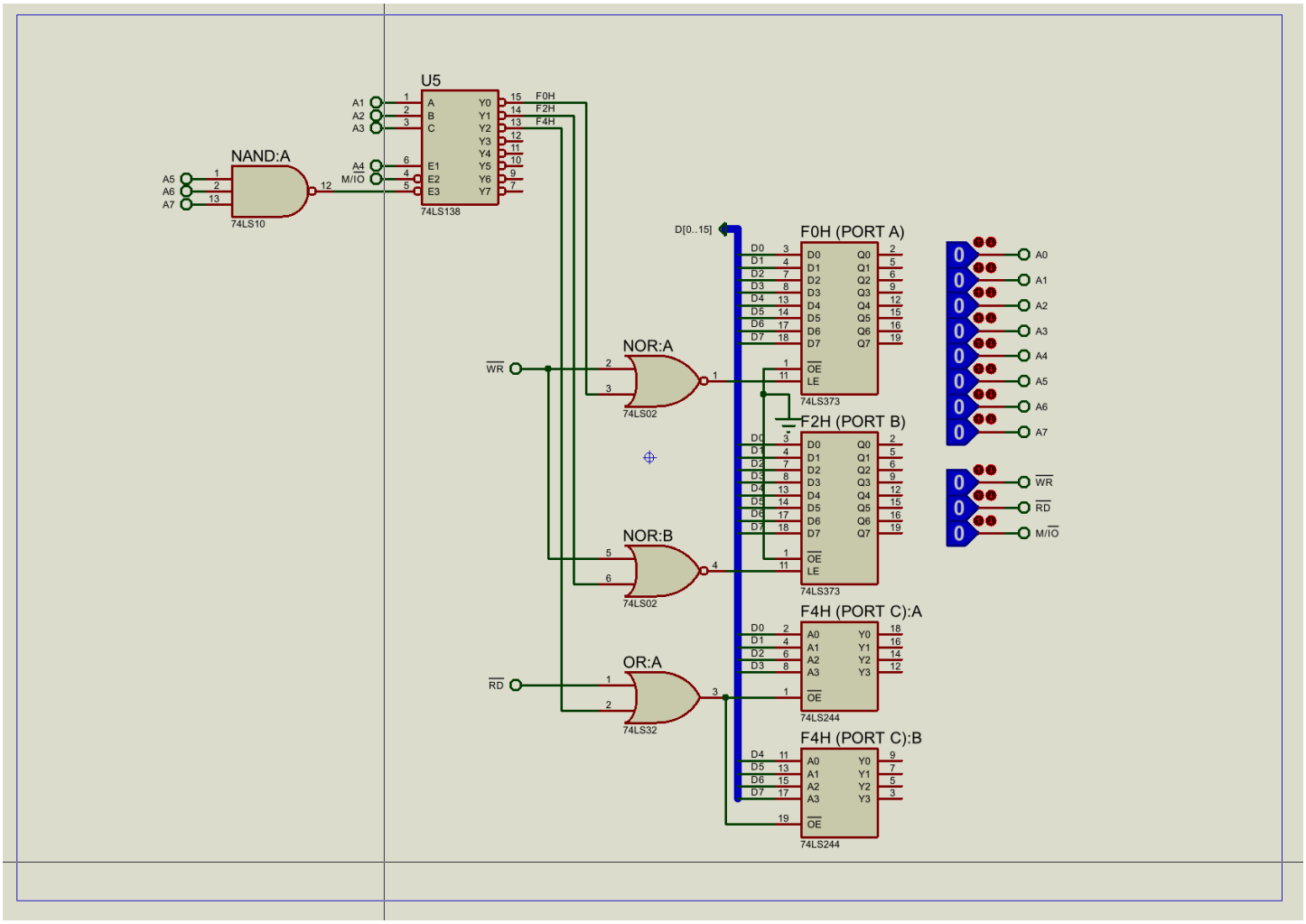


Table 1: Address Decoder Test

$Address\ (A_0 - A_7)$	$\overline{WR}$	$\overline{RD}$	$M/\overline{IO}$	$I/O\ Port\ Enabled$
F0H	0	1	0	PORTA (F0H)
F1H	1	0	0	None
F4H	0	1	0	None
F4H	0	1	1	None
F5H	1	0	0	PORTC (F4H)
F3H	0	1	0	PORTB (F2H)
F2H	0	1	1	None
02H	1	0	0	None
65H	0	1	1	None
F6H	1	0	0	None

- **Observe the data in Table 1. What is the role of the control lines M/IO, WR and RD in I/O address decoding?**
  The control lines M/IO, WR, and RD determine whether the 8086 is performing a memory operation or an I/O operation, and whether that operation is a read or a write.

  The M/IO line selects the type of access: when M/IO is at logic 1, the processor is accessing memory and no I/O ports can be enabled; when it is at logic 0, the processor is performing an I/O operation and an I/O port may be activated.

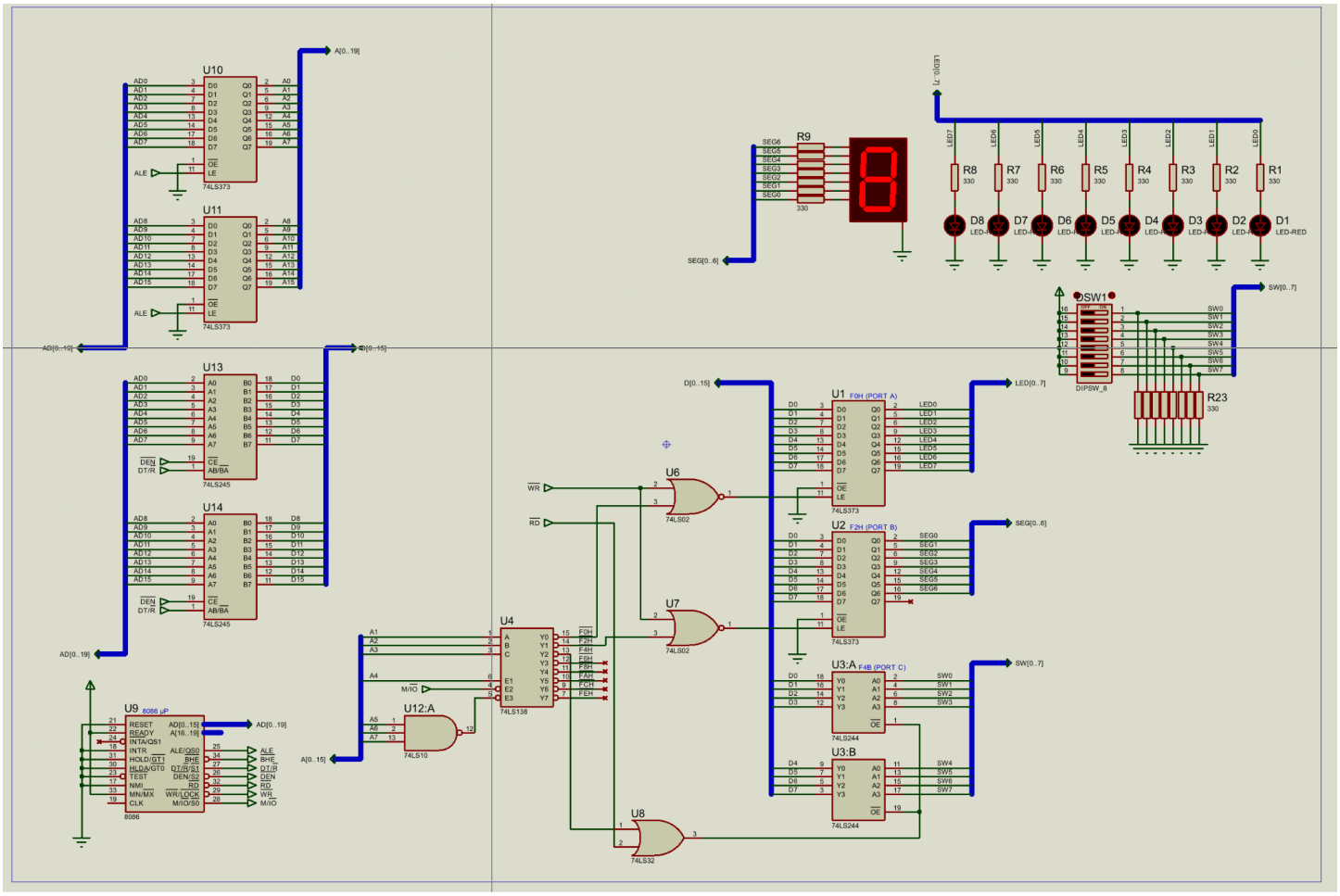
  The WR and RD signals specify the direction of the I/O transfer. A logic 0 on WR indicates a write operation, during which all input ports are disabled, while a logic 0 on RD indicates a read operation, during which all output ports are disabled.

  If a specific I/O port is to be enabled, the values of the decoded address must all align correctly in order for that I/O port to be enabled.

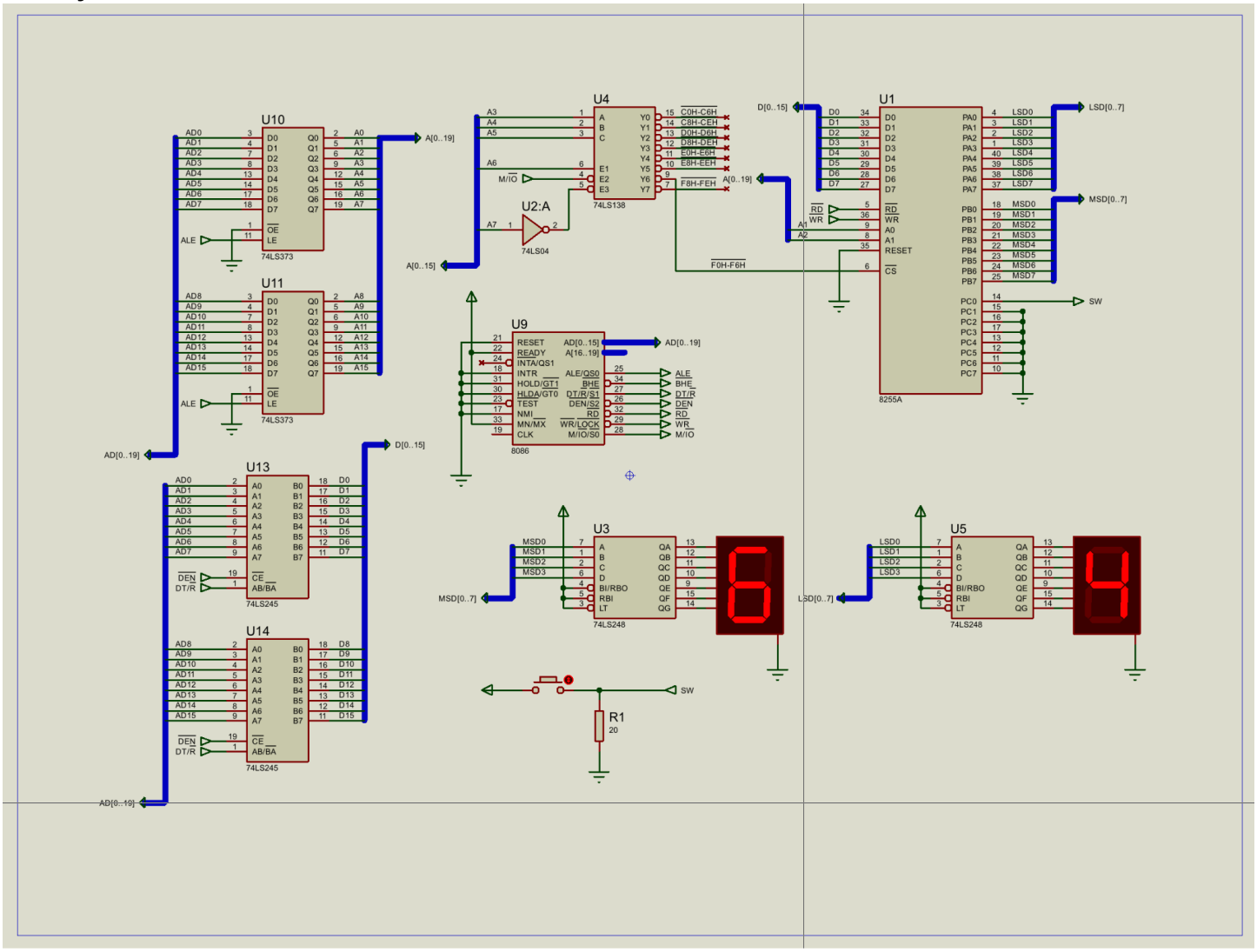
- **What do you think is the purpose of the latches and buffers?**
  The latches in the circuit hold the data coming from the data bus before sending it to the output device to ensure that the data remains stable long enough to be used, since the bus values change quickly while the buffers, on the other hand, regulate the flow of data from input devices to the processor and prevent multiple input sources from driving the bus simultaneously, which would potentially cause problems on the circuit.

- **Based on the decoder circuit and I/O address range, is the I/O system “memory mapped” or “isolated”? Why?**
  Because the circuit uses isolated I/O rather than memory-mapped I/O due to being only having an 8-bit I/O address (A0–A7) is decoded for the ports instead of the full 20-bit memory address range of the 8086.

Activity #2:


U10
U11
U13
U14
74LS373
74LS245
U9
8086 µP
8086
U4
74LS138
U12:A
74LS10
U1
F0H (PORT A)
U2
F2H (PORT B)
U3:A
F4B (PORT C)
U3:B
74LS244
U6
U7
U8
74LS02
74LS32
R9
R1
R2
R3
R4
R5
R6
R7
R8
330
LED-RED
DSW1
DIPSW_8
R23
A[0..19]
AD[0..19]
D[0..15]
LED[0..7]
SEG[0..6]
SW[0..7]

Activity #3:



- **With the I/O address range from C0H-FEH, determine the address of PORTA, PORTB, PORTC and Command Register**

  Addresses:

  PORTA: F0H
  PORTB: F2H
  PORTC: F4H
  Command Register (COM_REG): F6H

- **Determine the command byte if PORTA and PORTB are set as output and PORTC as input. All ports should operate in Mode 0.**

  Command byte (in binary): 1000_1001

- **Based on Activity #3, what can you say about the 8255 Programmable Peripheral Interface (PPI)?**

  The 8255 PPI simplifies I/O interfacing by reducing hardware complexity and requiring minimal firmware setup. It provides flexibility on each port, can be programmed as input or output and can operate in multiple modes, allowing one chip to handle many I/O operations efficiently.

  It also manages both data and control signals, making circuits easier to wire, scale, and debug. Although it is more complex and expensive than simple latches and buffers due to its need for software initialization, versatility and ability to support advanced I/O tasks.

- **What do you think are the advantages and disadvantages of using the 8255 from the simple latches and buffers as I/O ports?**

  Using the 8255 IC for I/O ports offers advantages over simple latches and buffers. It greatly reduces the required control logic, is easy to expand by adding more decoders and 8255 chips, and provides programmable ports that can be reconfigured without any hardware changes. This makes it far more flexible and suitable for handling a wide range of I/O operations. On the other hand, the 8255 is more complex because it requires software initialization using control words, and it is generally more expensive than basic latches and buffers.