Laboratory Report

Activity #1

<Write the calculations and solutions performed in Activity #1. Include sources codes and schematic diagrams if required in the e

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Activity #1

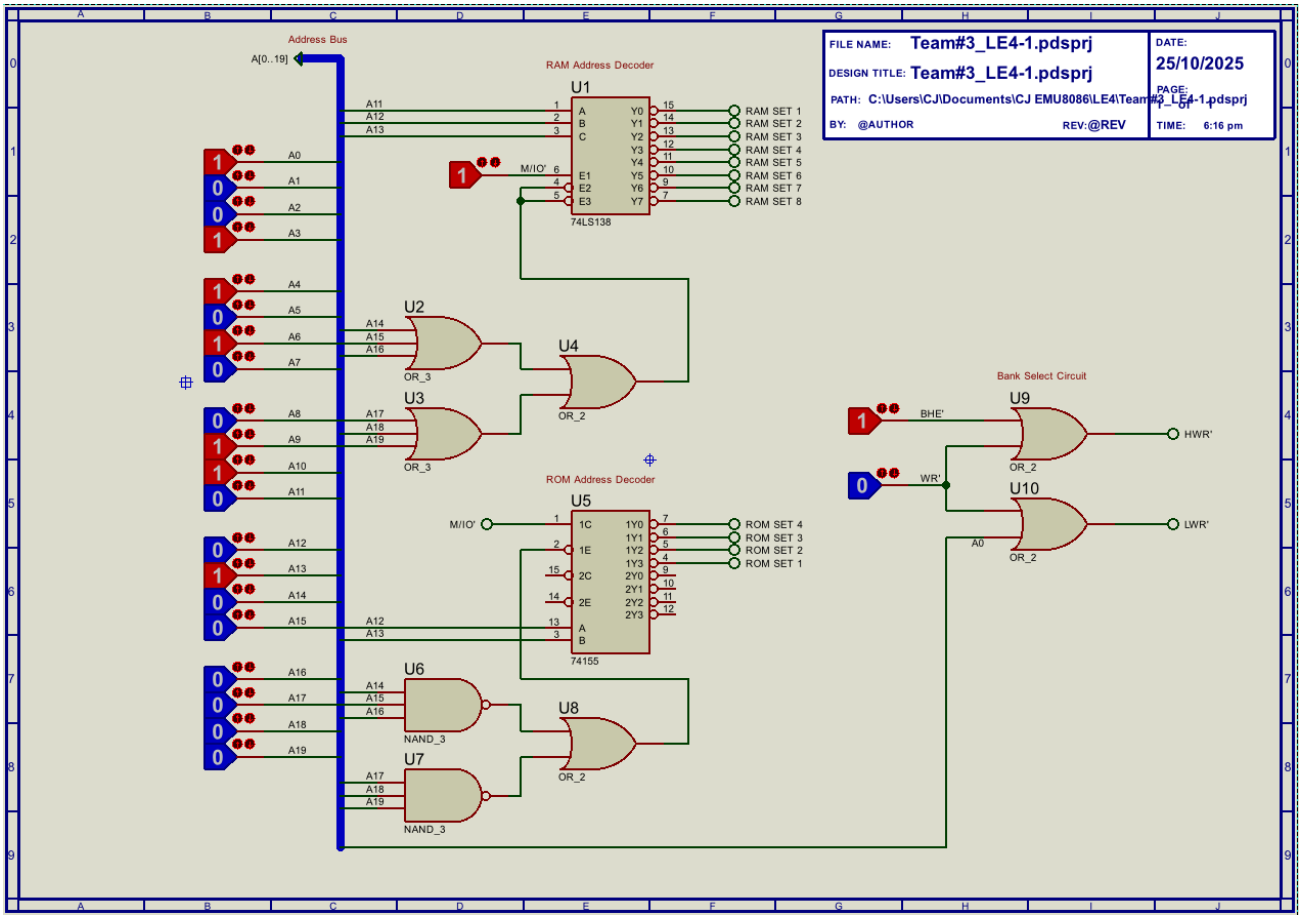

Figure 1.

Table 1. Simulated address decoding and RAM write/read data.

ADDRESS ($A_{19}..A_0$)		M/$\overline{IO}$	$\overline{WR}$	$\overline{BHE}$	Memory Set Enabled	$\overline{HWR}$	$\overline{LWR}$	**Observations**
0000 0000 1111 0000 0001	00F01H	1	0	0	RAM Set 2	0	1	high bank 8-bit transfer (write)
1111 1100 0110 1000 0010	FC680H	1	0	1	ROM Set 4	1	0	low bank 8-bit transfer (write)
0000 0101 1010 0111 1100	05A7CH	1	1	0	none	1	1	address out of range
1111 1111 0000 0000 0010	FF002H	0	0	0	none	0	0	none
0000 0001 1111 1111 1111	01FFFH	1	1	1	RAM Set 4	1	1	read from memory
0000 0000 0000 0000 0001	00001H	1	1	0	RAM Set 1	1	1	read from memory
1111 1011 1111 0000 0011	FBF03H	1	0	0	none	0	1	address out of range
0000 0000 1111 1100 1110	00FCEH	0	1	1	none	1	1	none
0000 0100 0000 0000 0000	04000H	1	0	0	none	0	0	none
0000 0010 0110 0101 1001	02659H	1	0	1	RAM Set 5	1	1	no bank enabled

a. How many RAM and ROM chips are used?

- The circuit uses eight RAM chips and four ROM chips, as indicated by the configuration of the address decoders, with a 3-to-8 decoder for RAM giving eight chip select outputs and a dual 2-to-4 decoder for ROM giving four chip select outputs for four chips.

b. What is the chip size of the RAM and ROM?

- Each RAM chip has a chip size of 2K x 8, meaning it stores 2048 bytes, while each ROM chip has a size of 4K x 8, storing 4096 bytes, based on the number of address lines feeding the chip enables and internal address decoding.

c. Determine the address range of the RAM and ROM.

- The total address range for the RAM is 0x0000 to 0x3FFF, or 16 KB spread over eight RAM chips, and the total address range for the ROM is 0x4000 to 0x7FFF, or 16 KB covered by four ROM chips, reflecting the mapping due to their sizes and how the chips are enabled in the circuit.

d. Based on the number of chips and chip size, calculate and determine the address range (start and end) of each chip sets for both RAM and ROM.

RAM

Set	Start Address	End Address	Address Range
1	00000H	00000H + 007FFH = 007FFH	00000H - 007FFH
2	00800H	00800H + 007FFH = 00FFFH	00800H - 00FFFH
3	01000H	01000H + 007FFH = 017FFH	01000H - 017FFH
4	01800H	01800H + 007FFH = 01FFFH	01800H - 01FFFH
5	02000H	02000H + 007FFH = 027FFH	02000H - 027FFH
6	02800H	02800H + 007FFH = 02FFFH	02800H - 02FFFH
7	03000H	03000H + 007FFH = 037FFH	03000H - 037FFH
8	03800H	03800H + 007FFH = 03FFFH	03800H - 03FFFH

ROM

Set	Start Address	End Address	Address Range
1	04000H	04000H + 00FFFH = 04FFFH	04000H - 04FFFH
2	05000H	05000H + 00FFFH = 05FFFH	05000H - 05FFFH
3	06000H	06000H + 00FFFH = 06FFFH	06000H - 06FFFH
4	07000H	07000H + 00FFFH = 07FFFH	07000H - 07FFFH

- Each RAM and ROM chip set gets a block of addresses, and you find each chip's end address by adding the chip size minus one to its start address. This makes it easy to see the address range covered by each chip, with no gaps or overlap.

e. Suggest an actual RAM (static RAM) and ROM (EPROM) integrated circuit (IC) with the same size as determined in (b).

- A suitable RAM IC matching the 2K x 8 chip size is the 6116 SRAM, which is a static RAM commonly used for this size. For ROM, a fitting EPROM IC for the 4K x 8 chip size is the 2732 or 27C32, which are standard EPROMs used for storing 4KB of data. These ICs align perfectly with the sizes calculated and are widely available for practical use in similar memory systems.

Activity #2

1. Calculate the start and end address of the ROM and RAM. Include also the number of sets and the start and end addresses of each chip.

RAM Address Mapping (16K x 16 Using 8K x 8 chips)

Each set uses two chips (one for low byte, one for high byte).

Set	Start Address	End Address (Calculation)	Address Range
1	00000H	00000H + 01FFFH = 01FFFH	00000H – 01FFFH
2	02000H	02000H + 01FFFH = 03FFFH	02000H – 03FFFH

Solution: 8K = 8 x 1024 = 8192 = 2000H bytes, thus each chip covers 2000H bytes, but for calculation with the last address included, use 01FFFH as chip size - 1 (8K = 2000H, so last byte: 0000H + 1FFFH = 1FFFH). Since the data bus is 16-bit, for each address range, one chip is for D0-D7 (low), one for D8-D15 (high).

ROM Address Mapping (16K x 16 Using 8K x 8 chips)

Each set uses two chips (one for low byte, one for high byte).

Set	Start Address	End Address (Calculation)	Address Range
1	FC000H	FC000H + 01FFFH = FDFFFH	FC000H – FDFFFH
2	FE000H	FE000H + 01FFFH = FFFFFH	FE000H – FFFFFH

Solution: FFFFFH − FC000H + 1 = 40000H addresses (so 16K), similar calculation for each set.