Cairo University, Faculty of Computers and Information

FACULTY OF COMPUTERS AND INFROMATION, CAIRO UNIVERSITY

CS322: Computer Architecture and Organization
Year 2020 – 2021

First Semester

Assignment 2 – Version 1.0

Course Instructors:

Dr. Mohammad El-Ramly

Revision History

Version 1.0	Dr Mohammed El-Ramly	25 Nov. 2020	Version 1.0

CS322: Computer Architecture and Organization
Assignment 2 (8 + 2 marks) – Version 1.0

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Objectives

1- Learn digital design with SystemVerilog and related tools.
2- Practice digital design with SystemVerilog.
3- Building and testing math circuits.
4- Train on digital design synthesis and simulation tools.

Instructions

1. **These instructions must be followed to get the full marks. يجب اتباع هذه التعليمات بكل دقة**
2. **Deadline is Friday 4 Dec. @ 10 am. Weight is 8 marks.**
3. **This is a group assignment to be solved in groups of 2.**
4. Solution is to be provided as one zip file containing a pdf file with all solutions (including designs, code, simulation results and screens), along with SystemVerilog files containing working designs, along with simulation files.
5. Please submit **only work that you did yourself**. If you copy work from your friend or book or the net **you will fail the course**. لا تغش تسليم حلول منقولة من أى مصدر يؤدى إلى الرسوب فى هذا المقرر الحل أو تنقله من أى مصدر و اسألنى فى أى شئ لا تفهمه لكن لا تنقل الحلول من النت أو من زملائك أو أى مكان

Task 0 (0 marks)

1. Watch SystemVerilog tutorial (see links on acadox)
2. Read chapters 4 and 5 from the course textbook.
3. Install and learn these tools (See links in acadox):
   - Quartus II Web Edition for model synthesis (converting Verilog to schematic and vie versa)
   - ModelSim PE Student Edition for model simulation (simulating the behavior of the model)
4. Learn how to run simulation and how to write a test bench for a circuit.

✓Task 1 - Bonus (2 marks) (Individual Task) – Due 28 Nov.

Individual students can earn bonus marks by producing a video showing the design of non-trivial circuit or a FSM in Quartus and its simulation in ModelSim or the development of a test bench file to validate that the circuit works right. **They should upload in a public place and send post link in acadox under the designated task.**

✓Task 2 – Problem Solving (4 marks) (Individual Task)

Each student will solve a set of problems (from Digital Design and Computer Architecture, 2nd ed. by Harris and Harris). He will design the circuit, write it in SystemVerilog, synthesize it, and simulate how it runs to test it. In the report, he will provide code for the design, the schematic diagram resulting from synthesizing the code and description and simulation results of the screen shots. **Student will submit solution in one pdf report, integrated, and problems put in order inside the solution (with name of student beside each problem he solved)**

- Student with less ID, will solve the problems: Implement SystemVerilog design for FSM of problem **3.31** and solve problems **4.42**, **4.46**, **4.50 a, b, c, d, e**
- Student with bigger ID, will solve problems: Implement SystemVerilog design for FSM of problem **3.32** and solve problems **4.44**, **4.48**, **4.50 f, g, h, i, j**

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Task 3 – FP Multiplier (2 marks) (Group Task)

Implement and test (synthesize, simulate and write a test-bench) for a **Floating Point Multiplication** that is capable of multiplying two single precision floating point numbers that follow IEEE 754. Simulate your circuit and write a test-bench to test it on different values.

Use modular design by building small building blocks (modules) and then integrating it to make eh multiplier. On the side you are given a block diagram of the components of the multiplier.

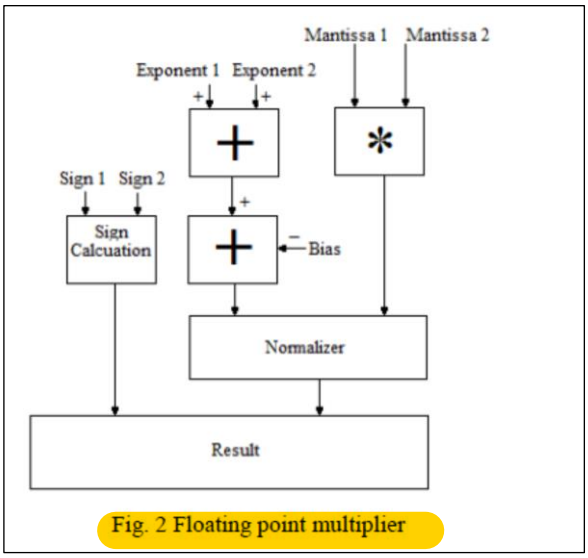
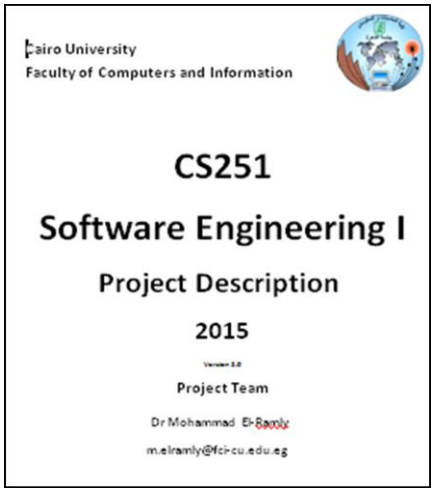


Fig. 2 Floating point multiplier

Task 4 – ALU (2 marks) (Group Task)

Solve problems **5.9, 5.10, 5.11** and **5.12** from the book which ask you to design an integer 32-bit ALU using SystemVerilog. Develop, synthesize, simulate ad test your design using a test-bench.



Submission Instructions

Task 1 (Bonus) – Deadline 28 Nov.

1- This video is needed early to help other students.
2- Upload your video in a public place like a shared Google drive or YouTube.
3- Submit the link to your video in a text file under acadox.

Task 2, 3, 4 – Deadline 4 Dec.

1. **Team will submit a zip file containing 2 components.**
2. **The first will be a printed pdf report, with the following:**
   - The document should have a cover page like this.
   - Document should be **organized and stabled**.
   - The document will include for every problem, SystemVerilog design, schematic design and screen shots of the simulation and result of the test-bench testing if needed.
3. **The second is a directory with project files, Verilog files, simulation files, test-bench files and any other SOURCE files. Do not include any intermediate or excitable files.**
4. TA can ask any team member about any of the programs developed and its code**.**

Marking Criterion

1. 2.0 for doing a useful video as in Task 1 that is clear, useful and with loud voice.
2. 4.0 for solving your problems of Task 3 successfully, 1 mark per problem.
3. 2.0 for building an testing the FP Multiplier and that it works successfully.
4. 2.0 for building an testing the integer 32-bits ALU and that it works successfully.
5. Up to -8 for any form of cheating.