KON309E

Microcontroller Architecture Overview

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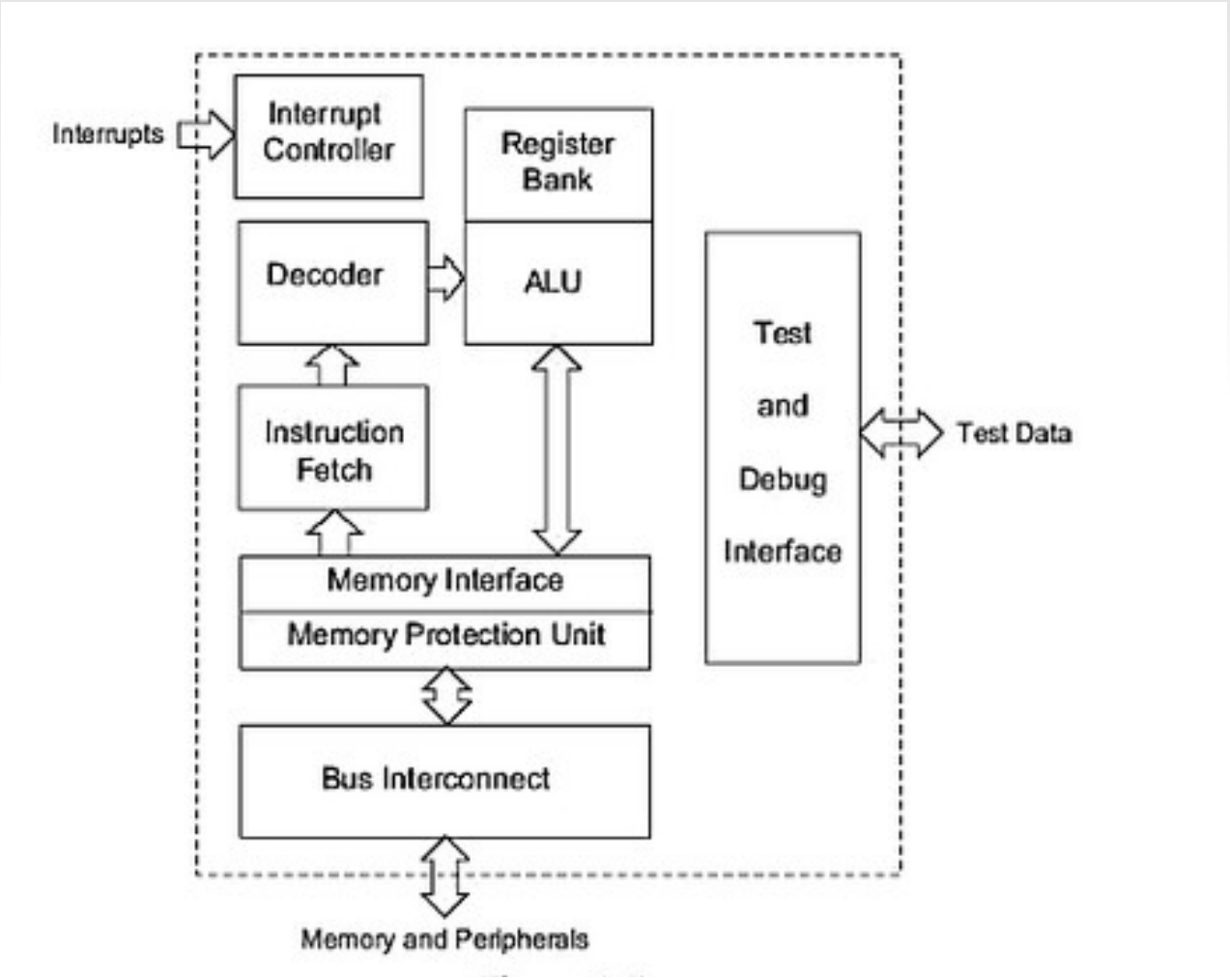
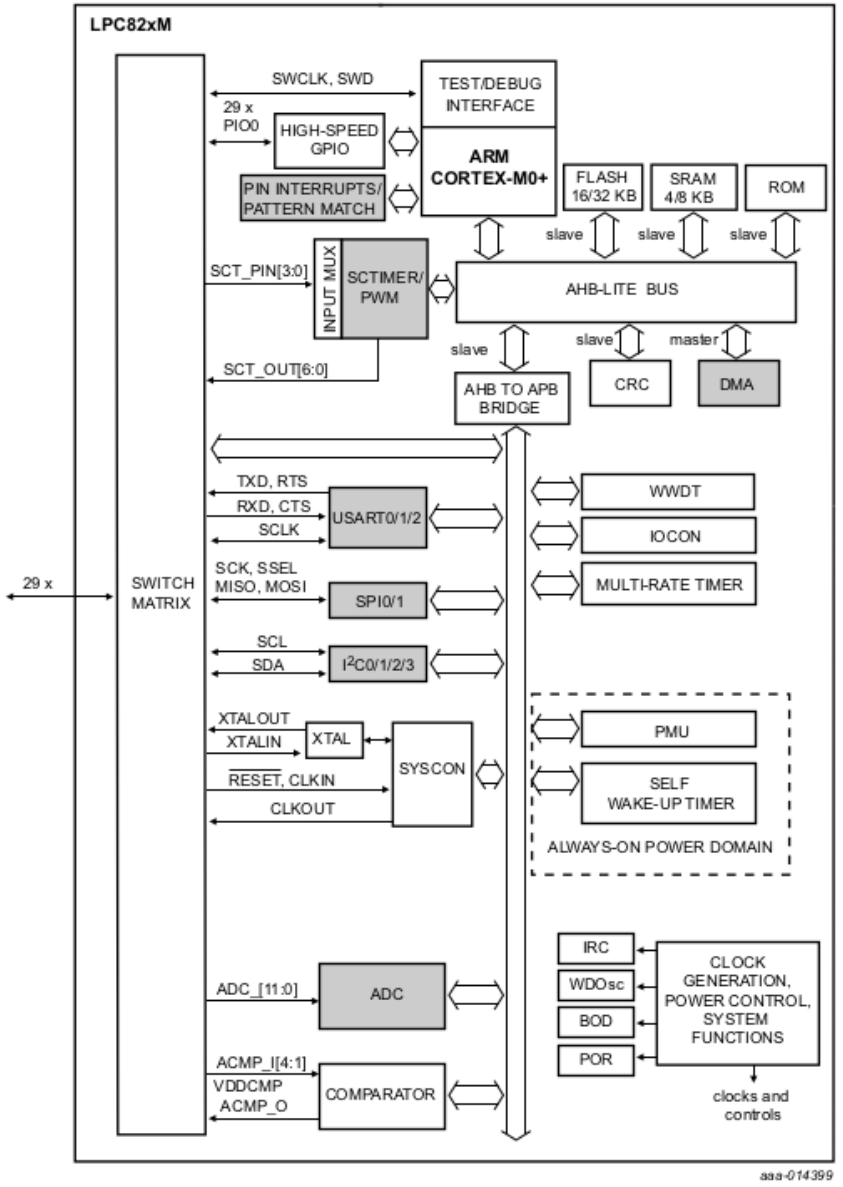
2023

ARM Cortex M0
Simplified Block Diagram



LPC824 Processor Structure

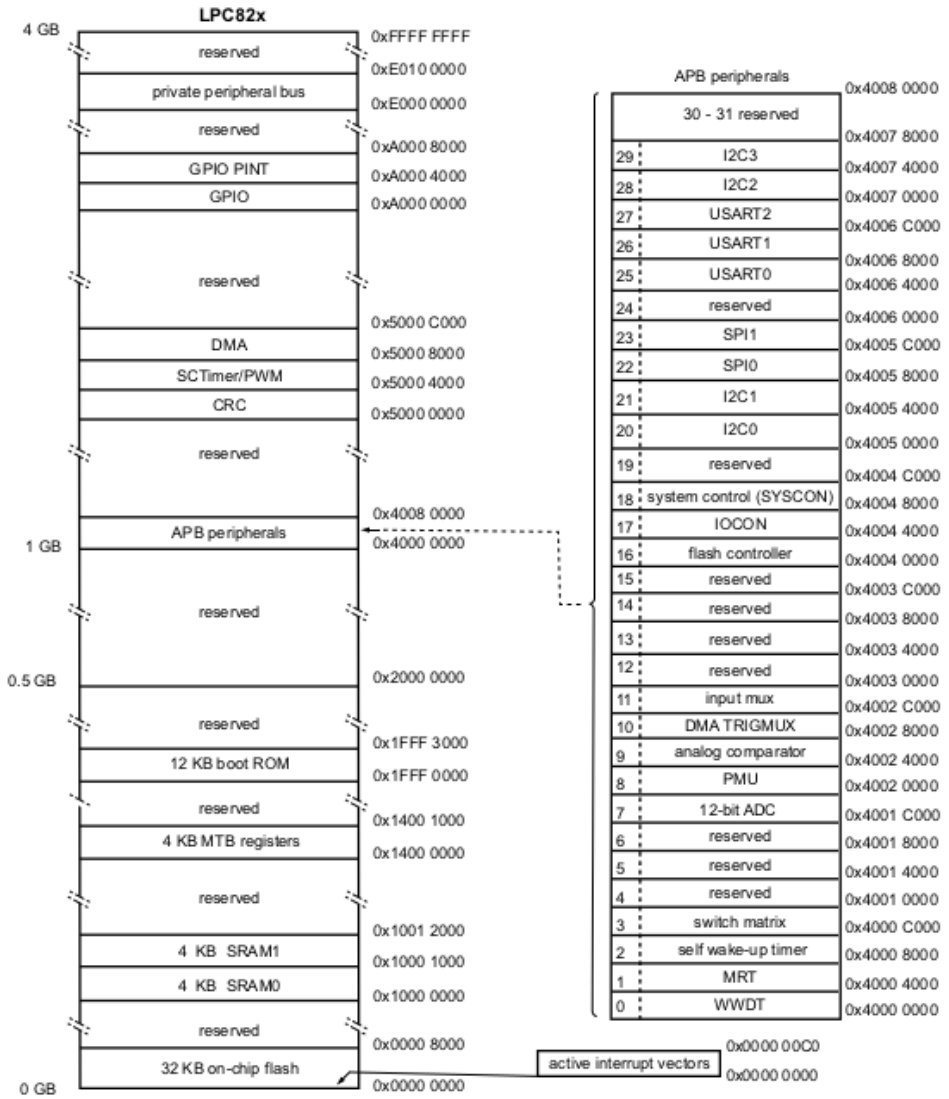


Gray-shaded blocks show peripherals that can provide hardware triggers or fixed DMA requests for DMA transfers.

Fig 3. LPC82x block diagram

LPC824 Memory Map

2.2.1 Memory mapping



The private peripheral bus includes the ARM Cortex-M0+ peripherals such as the NVIC, SysTick, and the core control registers.

Fig 2. LPC82x Memory mapping

LPC824 Clock Generation

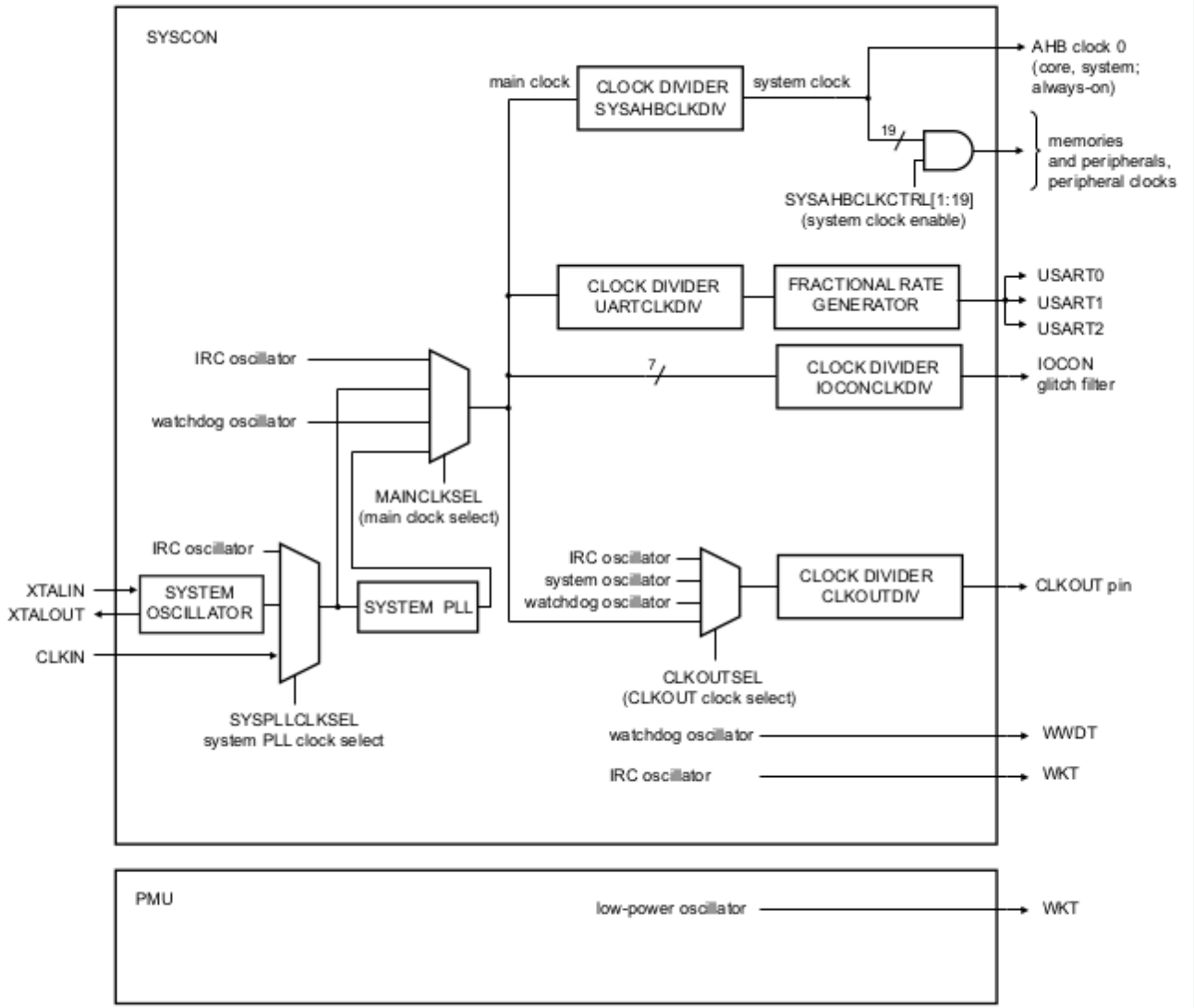


Fig 5. Clock generation

NXP LPC824

- ARMv7-M architecture, 32 bit processor.
- 3-stage pipeline with branch speculation.
- 32-bit hardware multiply with 32-bit or 64-bit result,
- signed or unsigned, add or subtract after the multiply.
- 32-bit hardware divide (2-12 cycles).
- Saturated math support.
- 240 interrupts, plus NMI.
- 32k FLASH, 8k RAM
- 30MHz clock frequency.
- LPC824M201JHI33 price: US$ 0.75

Contact Information

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