Bahar Asgari

Georgia Institute of Technology
School of Electrical and Computer Engineering
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Research Interests

- Computer Architecture
- Machine Learning
- Reliable Memory Systems
- Sparse Problem Acceleration
- Deep Neural Networks
- Scientific Computing (PDE solvers)

Education

Georgia Institute of Technology Aug. 2015 – Dec. 2020
Ph.D. in Electrical and Computer Engineering
Advisor: Sudhakar Yalamanchili
Co-Advisor: Hyesoon Kim
Dissertation Title: Efficiently Accelerating Sparse Problems by Enabling Stream Accesses to Memory Using Hardware/Software Techniques

Iran University of Science and Technology Sep. 2011 – Nov. 2013
M.E. in Computer Engineering - Computer Systems Architecture
Advisor: Mahdi Fazeli

Iran University of Science and Technology Sep. 2007 – Sep. 2011
B.E. in Computer Engineering - Hardware
Advisor: Nasser Mozayani

Awards

DAC Young Student Fellowship 2020
And the winner of best elevator-pitch presentation

iREDEFINE 2020
An intensive academic career workshop for women in ECE
Orlando, Florida

Rising Stars 2019
An intensive academic career workshop for women in EECS
University of Illinois at Urbana-Champaign

Ranked 1^{st} in the master's program class of 2013
Iran University of Science and Technology

Admitted to graduate studies as an exceptional talent 2011
Iran University of Science and Technology

Ranked 3^{rd} in the bachelor's program class of 2011
Iran University of Science and Technology

Ranked among top 0.5% 2007
Nationwide entrance exam of Iranian universities

Professional Experiences

Industry

- **Apple**, Cupertino, CA — May 2019 – Aug. 2019
  Intern at Special Project Group
  Involved in designing autonomous systems
- **Apple**, Cupertino, CA — May 2018 – Aug. 2018
  Intern at Special Project Group
  Modeled and designed hardware accelerators for sparse problems
- **Rahyaft**, Tehran, Iran — Oct. 2012 – July 2015
  Engineer at R&D Group
  Involved in a smart-home project as follows:
  - Designed and implemented digital IP-based microphones
  - Designed and implemented a remote door lock controlled by phone
- **Azm Electronics**, Tehran, Iran — June 2011 – Aug. 2011
  Intern at R&D Group
  - Designed and implemented a time-clock system using mifare cards
- **Saipa Co.**, Tehran, Iran — June 2010 – Aug. 2010
  Intern at Computer Networks Group

Academia

- **Georgia Institute of Technology**, Atlanta, GA — Aug. 2016 – Present
  Research assistant in the CASL and HPArch labs
  - Research topics: accelerating sparse problems, designing hardware for efficiently solving PDEs, accelerating training and inference of neural networks, systolic-based computation, near-data processing, and scalable memory systems
- **Sharif University of Technology**, Tehran, Iran — Dec. 2013 – July 2015
  Research assistant in the Digital Electronics lab
  - Research topics: designing fault-tolerant SRAM cells
- **Iran University of Science and Technology** — Sep. 2011 – Nov. 2013
  Research assistant in the Dependable Systems and Architectures lab
  - Research topics: Enhancing the reliability of on-chip memories in modern processors by employing STTRAM

Publications

2021

19. **Bahar Asgari**, Ramyad Hadidi, Jiashen Cao, Da Eun Shim, Sung-Kyu Lim, Hyesoon Kim. "Fafnir: Accelerating Sparse Gathering by Using Efficient Near-Memory Intelligent Reduction." 27^{th} IEEE International Symposium on High-Performance Computer Architecture (HPCA), 2021.

18. Ramyad Hadidi, **Bahar Asgari**, Sam Jijina, Adriana Amyette, Nima Shoghi, Hyesoon Kim. "Quantifying the Design-Space Tradeoffs for Autonomous Drones." 26^{th} Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2021.

2020

17. **Bahar Asgari**, Ramyad Hadidi, Tushar Krishna, Hyesoon Kim, Sudhakar Yalamanchili. "Alrescha: A Light-Weight Reconfigurable Sparse-Computation Accelerator." 26^{th} IEEE International Symposium on High-Performance Computer Architecture (HPCA), 2020.

16. **Bahar Asgari**, Ramyad Hadidi, Nima Shoghi Ghaleshahi, Hyesoon Kim. "Pisces: Power-Aware Implementation of SLAM by Customizing Efficient Sparse Algebra." 57^{th} Design Automation Conference (DAC), 2020.

15. **Bahar Asgari**, Ramyad Hadidi, Hyesoon Kim. "Meissa: Multiplying Matrices Efficiently in a Scalable Systolic Architecture." 38^{th} IEEE International Conference on Computer Design (ICCD), 2020.

14. **Bahar Asgari**, Ramyad Hadidi, Hyesoon Kim. "Ascella: Accelerating Sparse Problems by Enabling Stream Accesses to Memory." 23^{rd} Design, Automation, and Test in Europe (DATE), 2020.

13. **Bahar Asgari**, Ramyad Hadidi, Hyesoon Kim. "Proposing a Fast and Scalable Systolic Array to Implement Matrix Multiplications." 28^{th} Symposium on Field-Programmable Custom Computing Machines (FCCM), 2020.

12. **Bahar Asgari**, Saibal Mukhopadhyay, and Sudhakar Yalamanchili. "Mahasim: Machine Learning Hardware Acceleration Using a Software-Defined Intelligent Memory System." Springer Journal of Signal Processing Systems, Special Issue on Embedded Machine Learning, 2020.

2019

11. Ramyad Hadidi, Jiashen Cao, Yilun Xie, **Bahar Asgari**, Tushar Krishna, Hyesoon Kim. "Characterizing the Deployment of Deep Neural Networks on Commercial Edge Devices." IEEE International Symposium on Workload Characterization (IISWC) 2019. [**Best Paper Nominee**]

10. **Bahar Asgari**, Ramyad Hadidi, Hyesoon Kim, Sudhakar Yalamanchili. "Eridanus: Efficiently Running Inference of DNNs Using Systolic Arrays." IEEE Micro, Special Issue on Machine Learning Acceleration, 2019.

9. **Bahar Asgari**, Ramyad Hadidi, Hyesoon Kim, Sudhakar Yalamanchili. "Lodestar: Creating Locally-Dense CNNs for Efficient Inference on Systolic Arrays." 56^{st} Design Automation Conference (DAC), 2019.

8. Prashant Nair, **Bahar Asgari**, Moinuddin Qureshi. "SuDoku: Tolerating High-Rate of Transient Failures for Enabling Scalable STTRAM." 49^{th} IEEE/IFIP International Conference on Dependable Systems and Networks (DSN), 2019.

7. Fares Elsabbagh, **Bahar Asgari**, Hyesoon Kim and Sudhakar Yalamanchili. "Vortex RISC-V GPGPU system: Extending the ISA, Synthesizing the Microarchitecture, and Modeling the Software Stack." The Workshop on Computer Architecture Research with RISC-V (CARRV), 2019.

6. Younmin Bae, Ramyad Hadidi, **Bahar Asgari**, Jiashen Cao, Hyesoon Kim. "Capella: Customizing Perception for Edge Devices by Efficiently Allocating FPGAs to DNNs." 29^{th} FieldProgrammable Logic and Application (FPL), 2019.

Before 2019

5. Ramyad Hadidi, **Bahar Asgari**, Jeffrey Young, Burhan Ahmad Mudassar, Kartikay Garg, Tushar Krishna, Hyesoon Kim. "Performance Implications of NoCs on 3D-Stacked Memories: Insights from the Hybrid Memory Cube." IEEE international symposium on performance analysis of systems and software (ISPASS), 2018.

4. Ramyad Hadidi, **Bahar Asgari**, Burhan Ahmad Mudassar, Saibal Mukhopadhyay, Sudhakar Yalamanchili, and Hyesoon Kim. "Demystifying the Characteristics of 3D-Stacked Memories: A Case Study for Hybrid Memory Cube." IEEE International Symposium on Workload Characterization (IISWC), 2017.

3. **Bahar Asgari**, Mahdi Fazeli, Ahmad Patooghy, and Seyed Vahid Azhari. "A Microarchitectural Approach to Efficient Employment of STTRAM Cells in Microprocessors Register File." IET Computers & Digital Tech., 2016.

2. Ramin Rajaei, **Bahar Asgari**, Mahmoud Tabandeh, Mahdi Fazeli, "Single Event Multiple Upset Tolerant SRAM Cell Designs for Nano-scale CMOS Technology." Turkish Journal of Electrical Eng. & Computer Scn., 2016.

1. Ramin Rajaei, **Bahar Asgari**, Mahmoud Tabandeh, and Mahdi Fazeli. "Design of Robust SRAM Cells Against Single-Event Multiple Effects for Nanometer Technologies." IEEE Transactions on Device and Materials Reliability, 2015.

Preprints & Work in Progress

4. **Bahar Asgari**, Ramyad Hadidi, Joshua Dierberger, Charlotte Steinichen, Hyesoon Kim. "Copernicus: Characterizing the Performance Implications of Compression Formats Used in Sparse Workloads." arXiv preprint, arXiv:2011.10932, 2020.

3. Ramyad Hadidi, **Bahar Asgari**, Jiashen Cao, Younmin Bae, Da Eun Shim, Hyojong Kim, Sung-Kyu Lim, Michael S. Ryoo, Hyesoon Kim. "LCP: A Low-Communication Parallelization Method for Fast Neural Network Inference in Image Recognition." arXiv preprint, arXiv:2003.06464, 2020.

2. **Bahar Asgari**, Amaan Marfatia, Dheeraj Ramchandani, Hyesoon Kim. "Maia: Matrix Inversion Acceleration Near Memory." work in progress.

1. Ramyad Hadidi, Nima Shoghi, **Bahar Asgari**, Hyesoon Kim. "Context-Aware Task Handling in Resource-Constrained Robots with Virtualized Execution." work in progress.

Service

Submission co-chair

51^{th} International Symposium on Microarchitecture (MICRO-2018)

Reviewer

IEEE Computer Architecture Letters (CAL)
ACM Transactions on Architecture and Code Optimization (TACO)
IEEE Transactions on Reliability
IEEE Transactions on Aerospace and Electronic Systems (TAES)
IET Electronics Letters
IET Computers and Digital Techniques
Springer Journal of Signal Processing Systems

Judge

President's Undergraduate Research Awards (PURA)
Undergraduate Research Opportunities Program (UROP)
Honeywell STEM challenge

Discussion chair

PeRSonAl tutorial at ISCA 2020

Teaching Experiences

Instructor

- **Shahid Rajaee University**, Tehran, Iran

Microprocessors lab — Fall 2014
Computer architecture lab — Fall 2014
Microprocessor design — Spring 2014
Computer Organization and programming — Spring 2014

- **Iran University of Science and Technology**, Tehran, Iran
  Computer Organization and programming — Fall 2013
- **Azad Islamic University**, Tehran, Iran
  Computer Organization and programming — Spring 2013
- **University of Applied Science and Technology**, Tehran, Iran
  Computer Organization and programming — Fall 2012

Mentor

- **Georgia Institute of Technology**, Atlanta, GA
  Amaan Marfatia (*Recepient of PURA Award*) — Fall 2020
  Dheeraj Ramchandani (*Master's student*) — Fall 2020
  Joshua Dierberger — Spring 2020
  Charlotte Steinichen — Spring 2020
  Malik Burton — Spring 2020
  Luis Pastrana — Spring 2020
  Saiharshith Kilaru — Spring 2020
  Fares Elsabbagh (*Now at Apple*) — Spring 2019

Teaching Assistant

- **Georgia Institute of Technology**, Atlanta, GA
  Computer communications — Summer 2016
  Fundamentals of digital design — Spring 2016
  Fundamentals of digital design — Fall 2015
- **Iran University of Science and Technology**, Tehran, Iran
  Advanced computer architecture (graduate course) — Fall 2013
  Fault-tolerant design (graduate course) — Spring 2013
  Advanced digital design (graduate course) — Fall 2012
  Electronics circuits — Spring 2012

Grants

Georgia Institute of Technology, Atlanta, GA — Fall 2019
Participated in writing a grant proposal for
Laboratory of Physical Sciences (LPS)
