

实训详情

第1关 全加器设计

评测次数	评测信息
第1次	共有1组测试集,其中有1组测试结果不匹配。
最后一次	compile successfully

最近通过的代码

```
1 module fa_behavioral(a,b,ci,s,co);//考虑进位的加法器模块
2
      input a,b;
      input ci;
4 5
      output s;
      output co;
6 // 请在下面添加代码,完成一位全加器功能
 7 /* Begin */
8 assign s=a^b^ci;
9
    assign co=a&b|a&ci|b&ci;
10
11 /* End */
13 endmodule
14
```

第2关 无符号二进制数加法器的实现

评测次数	评测信息
第1次	./adder.v:9: syntax error ./adder.v:9: error: Invalid module instantiation
第2次	./adder.v:9: syntax error ./adder.v:9: error: Invalid module instantiation
最后一次	compile successfully

最近通过的代码

```
module adder(a,b,cin,cout,sum);
parameter bit_width=8;
output[bit_width-1:0] sum;
output cout;
input [bit_width-1:0] a,b;
input cin;

// 请在下面添加代码,完成n=8位的无符号二进制数加法器功能
/* Begin */
assign {cout,sum}=a+b+cin;
/* End */
endmodule
```

评测次数	评测信息
第1次	./substractor.v:9: error: Unable to bind parameter `a' in `substractor_tb.m' ./substractor.v:9: error: Unable to bind parameter `b' in
	`substractor_tb.m' ./substractor.v:9: error: Unable to bind parameter `cin' in `substractor_tb.m' ./substractor.v:9: error: Cannot evaluate
	genvar conditional expression: (a)<((b)+(cin)) 4 error(s) during elaboration.
第2次	./substractor.v:9: error: Unable to bind parameter `a' in `substractor_tb.m' ./substractor.v:9: error: Unable to bind parameter `b' in
	`substractor_tb.m' ./substractor.v:9: error: Cannot evaluate genvar conditional expression: (a)<(b) ./substractor.v:9: error: Unable to
	bind parameter `a' in `substractor_tb.m' ./substractor.v:9: error: Unable to bind parameter `b' in `substractor_tb.m' ./substractor.v:9:
	error: Cannot evaluate genvar conditional expression: (a)<(b) 6 error(s) during elaboration.
第3次	共有1组测试集,其中有1组测试结果不匹配。
最后一次	compile successfully

最近通过的代码

```
module substractor(a,b,cin,cout,sum);
parameter bit_width=8;
output[bit_width-1:0] sum;
output cout;
input [bit_width-1:0] a,b;
input cin;//carry
// 请在下面添加代码,完成n位的无符号二进制数减法器功能
/* Begin */
assign cout=(a<b)?1'b1:1'b0;
assign sum={cout,a}-b-cin;
/* End */
endmodule
```

第4关 定点二进制数的补码加减法运算器

评测次数	评测信息
第1次	./add_sub.v:11: syntax error ./add_sub.v:12: error: invalid module item/add_sub.v:13: syntax error ./add_sub.v:13: error: Invalid module instantiation ./add_sub.v:16: error: Invalid module instantiation ./add_sub.v:17: error: Invalid module instantiation ./add_sub.v:20: syntax error ./add_sub.v:20: error: invalid module item/add_sub.v:21: syntax error ./add_sub.v:21: error: Invalid module instantiation ./add_sub.v:22: syntax error ./add_sub.v:22: error: Invalid module instantiation ./add_sub.v:22: error: invalid module instantiation add_sub.v:23: error: invalid module item. add_sub_tb.v:4: error: duplicate definition for parameter 'bit_width' in 'add_sub'. add_sub_tb.v:5: sum wire definition conflicts with reg definition at ./add_sub.v:5/add_sub.v:5: error: Net ``cout'' has already been declared. add_sub_tb.v:6:
	overflow wire definition conflicts with reg definition at ./add_sub.v:5/add_sub.v:5: error: Net ``overflow" has already been declared.
第2次	./add_sub.v:11: syntax error ./add_sub.v:12: error: invalid module item/add_sub.v:19: syntax error ./add_sub.v:19: error: invalid module item/add_sub.v:21: syntax error ./add_sub.v:21: error: Invalid module instantiation ./add_sub.v:22: syntax error ./add_sub.v:22: error: Invalid module instantiation ./add_sub.v:23: error: Invalid module instantiation ./add_sub.v:23: error: Invalid module instantiation add_sub_tb.v:3: error: invalid module item. add_sub_tb.v:4: error: duplicate definition for parameter 'bit_width' in 'add_sub'. add_sub_tb.v:5: sum wire definition conflicts with reg definition at ./add_sub.v:5/add_sub.v:5: error: Net ``sum" has already been declared. add_sub_tb.v:6: overflow wire definition conflicts with reg definition at ./add_sub.v:5/add_sub.v:5/add_sub.v:5: error: Net ``overflow'' has already been declared.
第3次	./add_sub.v:12: tgt-vvp sorry: procedural continuous assignments are not yet fully supported. The RHS of this assignment will only be evaluated once, at the time the assignment statement is executed/add_sub.v:13: tgt-vvp sorry: cannot %cassign signal to a part select (a2[3:0])/add_sub.v:16: tgt-vvp sorry: procedural continuous assignments are not yet fully supported. The RHS of this assignment will only be evaluated once, at the time the assignment statement is executed/add_sub.v:17: tgt-vvp sorry: cannot %cassign signal to a part select (b2[3:0]). error: Code generation had 2 error(s).
最后一次	compile successfully

最近通过的代码

```
1 module add_sub(a,b,control,cout,overflow,sum);
    parameter bit_width=4;
    output[bit_width-1:0] sum;
                                  output cout, overflow;
    always@(a,b,control)
/********** End ********/
10
11
12
13
      begin
        a2[bit_width]=a[bit_width-1]; //将a符号位扩展成2位并赋值给a2
       14
15
16
17
18
     if (control==0) {cout,sum2}=a2+b2;
else {cout,sum2}=a2+(~b2)+control;
if((sum2[bit_width]^sum2[bit_width-1])==1) overflow=1;
else overflow=0; //用双符号位判溢出
sum[bit_width-1:0]=sum2[bit_width-1:0];
19
20
21
22
23
24 end
25 endmodule
```