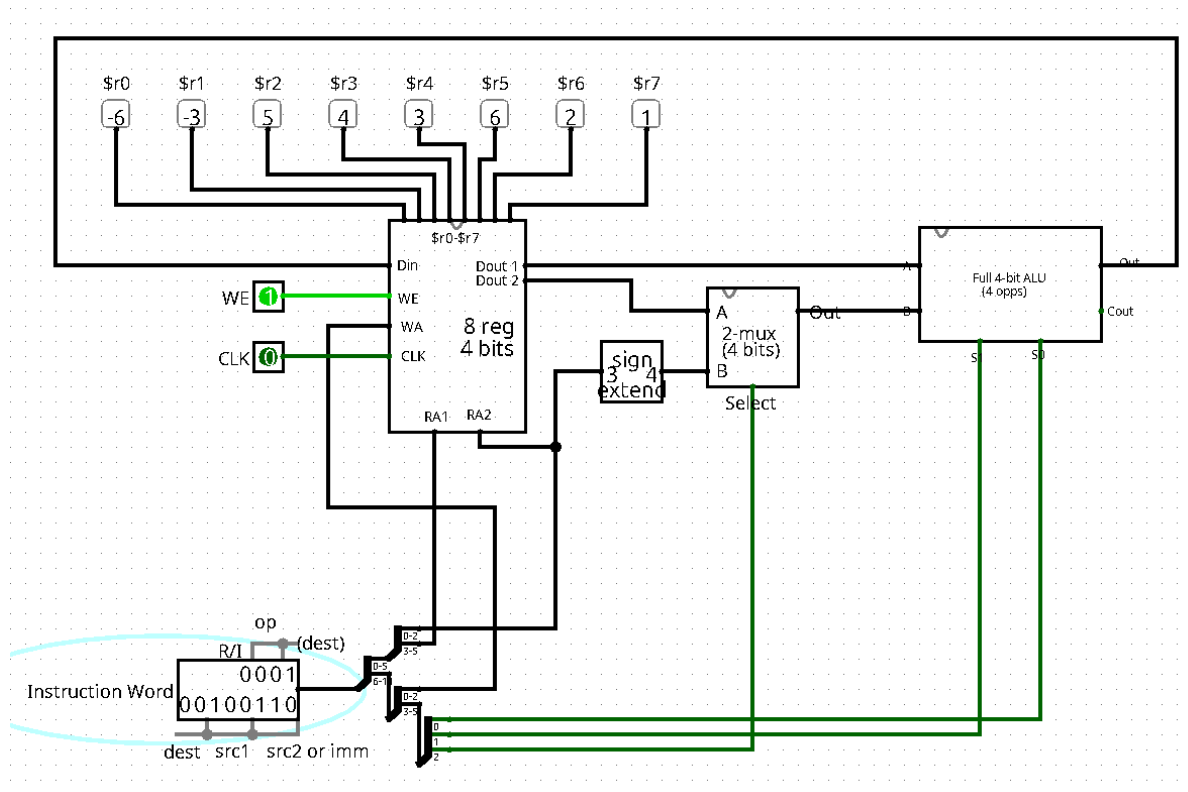
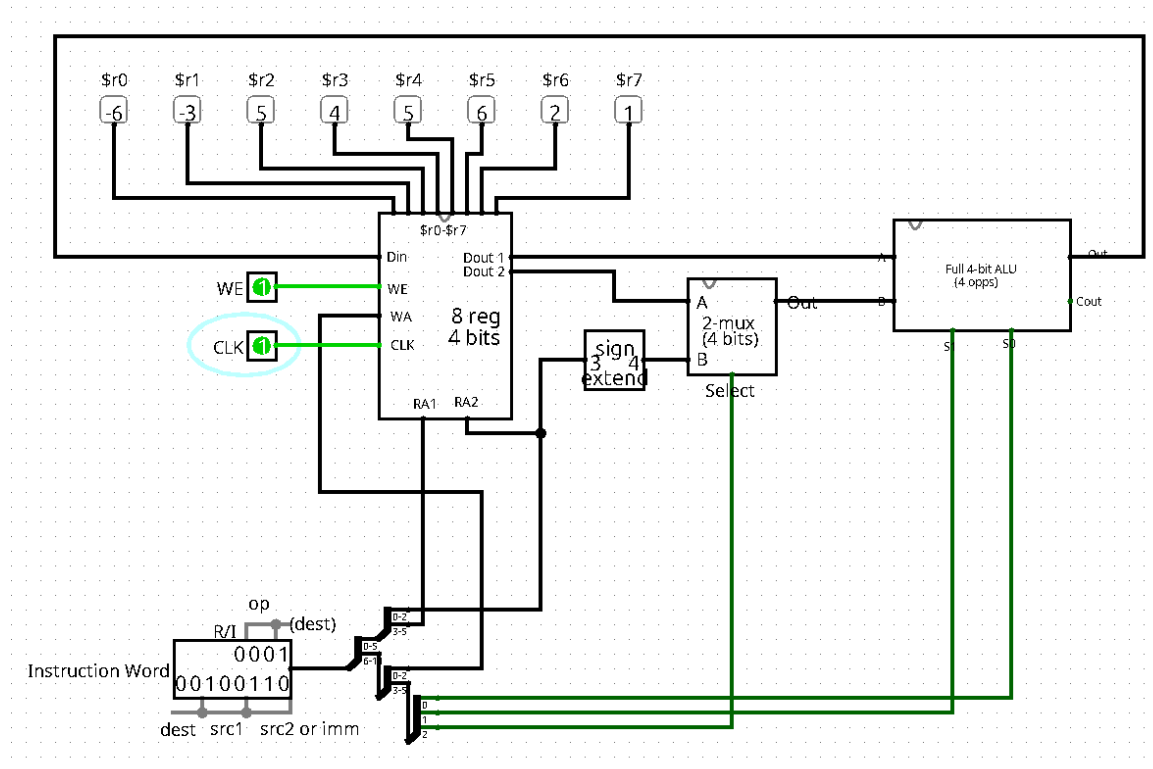


Lab 3

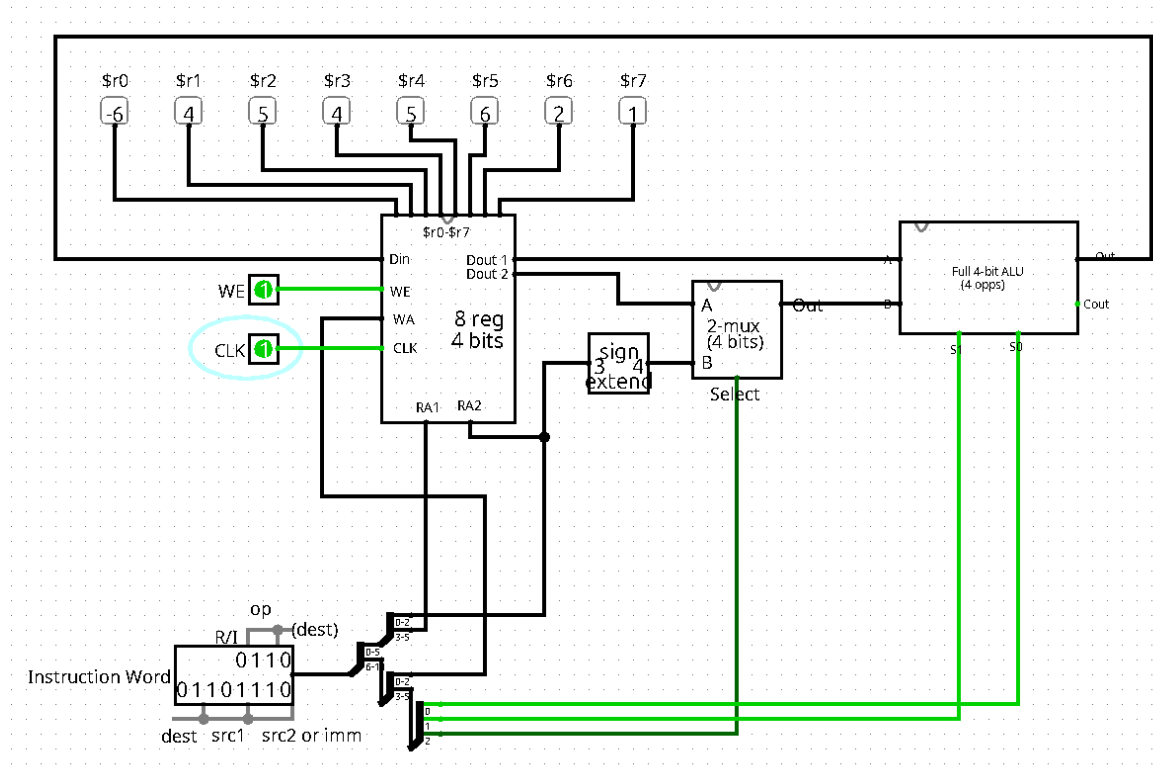
This processor implements a 12-bit instruction set architecture with support for both register-register and register-immediate operations, where the instruction word is divided into four fields: The 12 bit signifies if a register or immediate is being used. The bits 11 and 10 are the 2-bit operation codes for the ALU. The bits 9-7 are a 3-bit destination register address. The bits 6-4 are a 3-bit first source register address. Finally, the bits 3-1 are a 3-bit second source register address or the immediate number. The operation code specifying the ALU operation (00=ADD, 01=SUB, 10=AND, 11=OR). The destination and first source fields each specify one of eight registers (\$r0-\$r7), while the final field serves as either the second source register or a 3-bit signed immediate value (range -4 to +3) that is sign-extended to 4 bits before entering the ALU.

Initial State: ADD \$r4 \$r4 \$r6

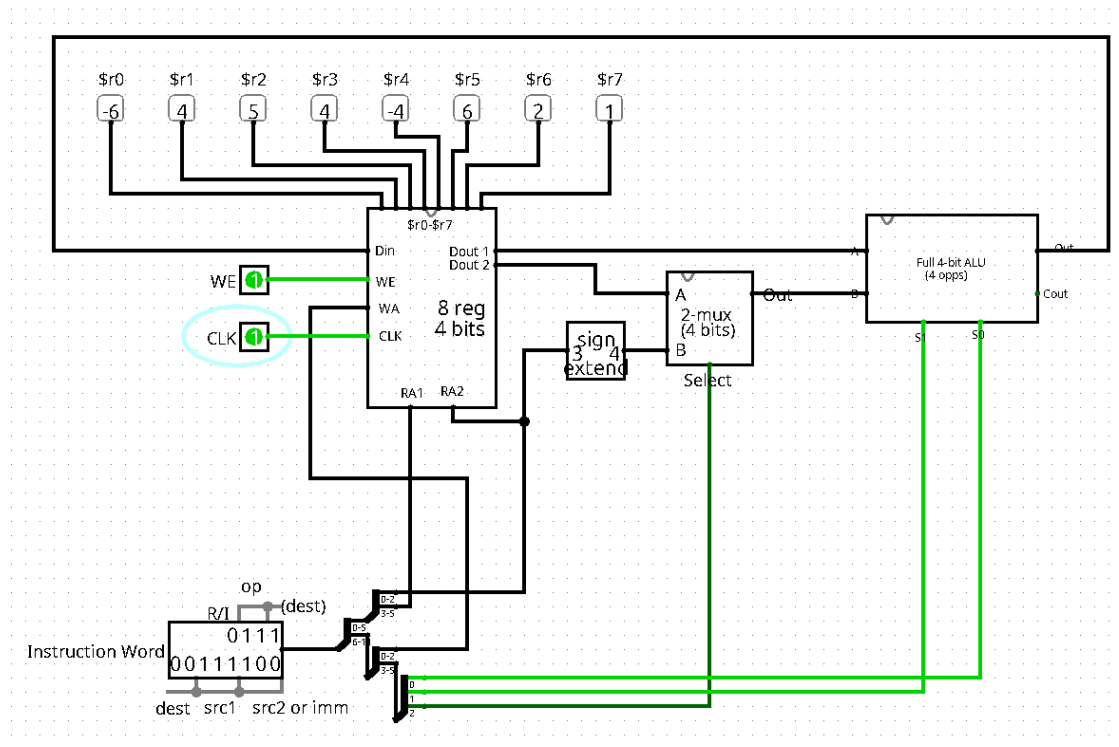




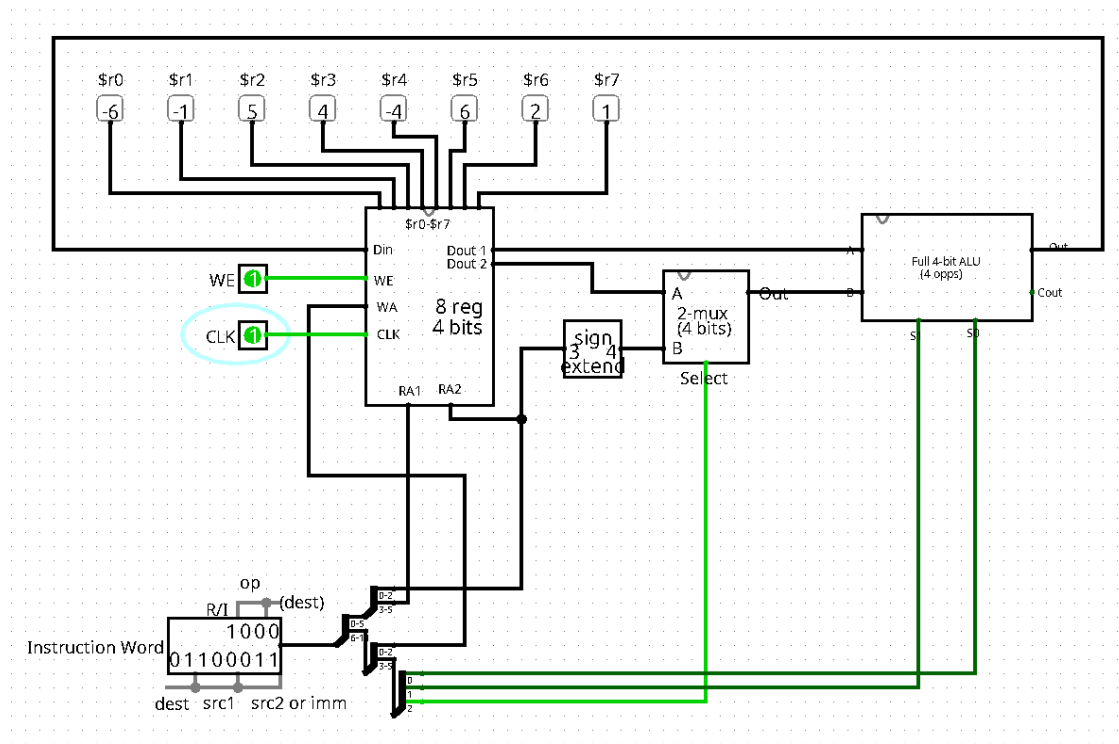
SUB \$r1 \$r5 \$r6



SUB \$r4 \$r7 \$r4



ADDi \$r1 \$r4 3



1. The missing bit is from the RA2 section of the instruction word because there are 8 registers. 8 registers require only 3 input bits so the instruction word uses 3 bits for RA2 but since it is also used for the immediate, we use a bit extender.
2. The largest immediate value you can put is 111 since there are only 3 bits to be used so the largest decimal number for the immediate is 7.
3. The lowest is 0 for the same logic as stated above.
4. It is only 8 out of the the 16 numbers that the immediate could possibly be since it is a 4-bit ALU, so a bit extender that could add a zero or a 1 could give us the full 16 decimal number that we could use for the immediate