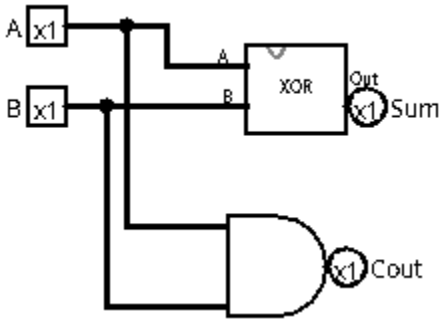
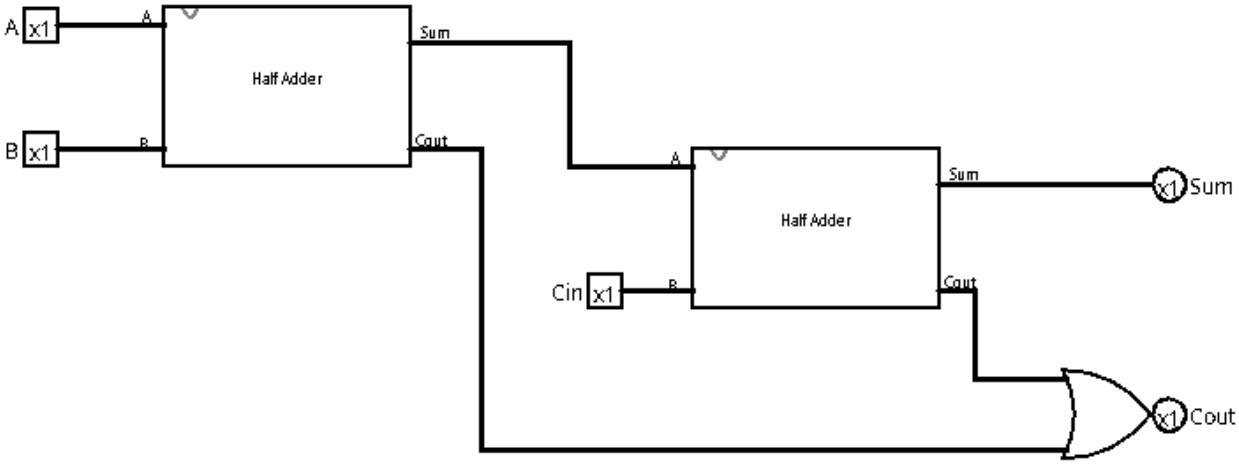
Lab 2

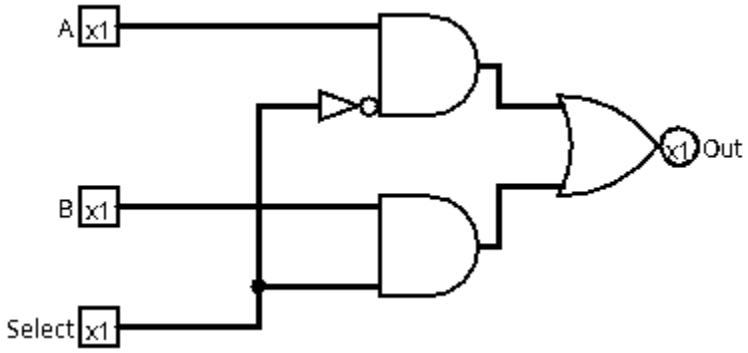
Half Adder



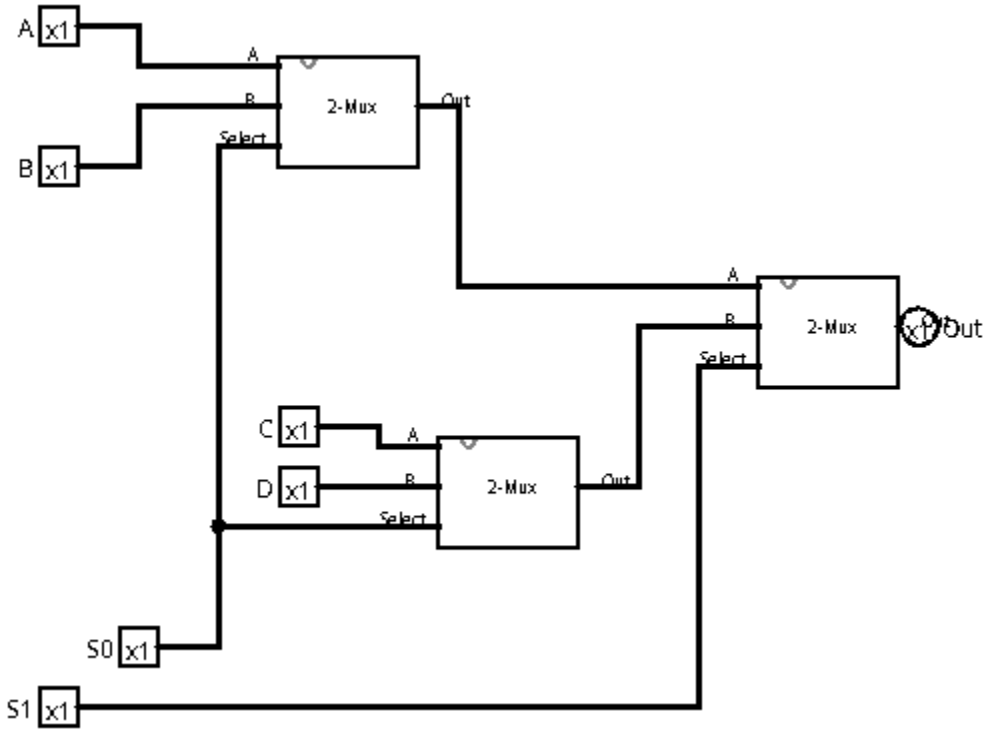
Full Adder



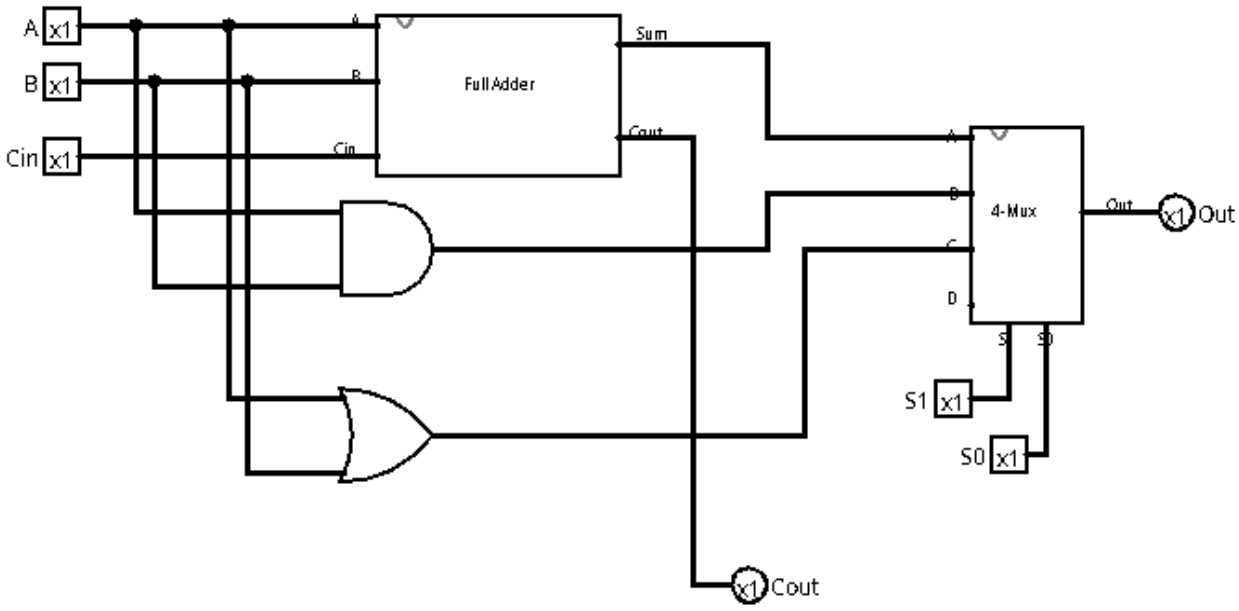
2-MUX



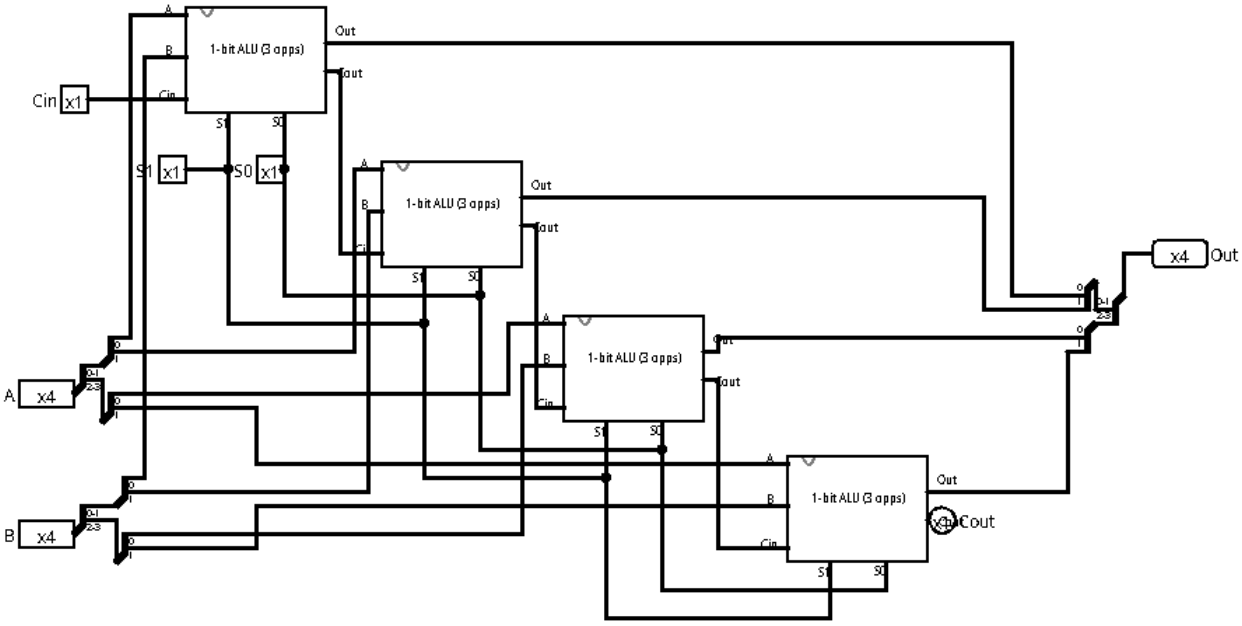
4-MUX



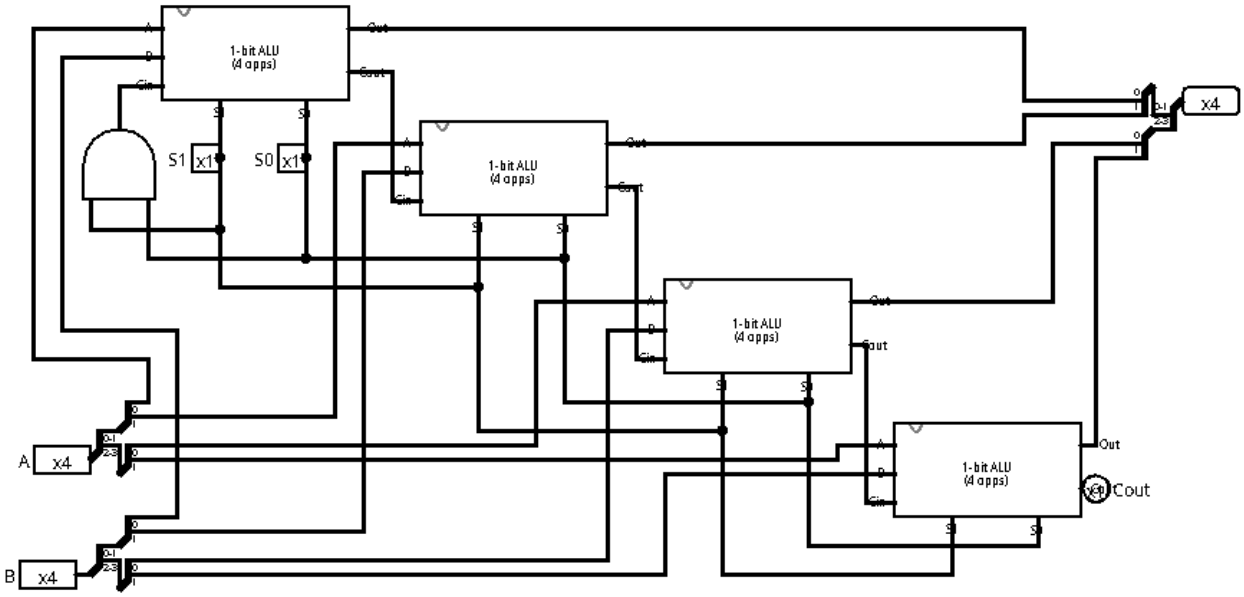
1-Bit ALU



4-Bit ALU



Full 4-Bit, 4-operation ALU



Writeup:

I created an input and output table that I used to test my outputs of my 4-bit, 4-op ALU. I selected all 4 mux operations, and for each operator I tested a couple of different numbers for both inputs and tested those outputs with each operation. For adding, ANDing and ORing, I just confirmed that each digit in their respective columns are correct based on what operation. For the subtract, double checking that when B is greater than A that the result is a 2's complement number with accurate magnitude.

A (bin)	B (bin)	S1 S0	Operation	Sum (bin)	Cout
0000	0000	00	ADD	0000	0
1010	1100	00	ADD	0110	1
0101	0011	01	AND	0001	0
1101	1110	01	AND	1100	0
0011	0001	10	OR	0011	0
1001	0011	10	OR	1011	0
0100	0010	11	SUB	0010	1
1011	0111	11	SUB	0100	1
0001	0110	11	SUB	1011	0