# Baili LIU

FPGA Engineer in the Financial Sector at NOVASPARKS Graduated from Polytech Nantes in 2022

# **PROFESSIONAL EXPERIENCE**

#### NovaSparks, Paris

FPGA Engineer | July 2024 - Present

- Development of Feed-handlers for financial market data processing
- Collaboration with the software team and tech lead to define specifications
- Decoding Ethernet market data such as CBOE Canada, Strike, CSE
- Developing new functionalities on multiple FPGA modules
- Developing reference models in C++ for RTL module verification
- Synthesis, P&R, and on-board verification on an automated platform

## Forvia (Faurecia Clarion Electronics), Paris

ASIC RTL Engineer, Outsourced via Elsys Design | February 2023 - July 2024

- Migrating algorithms from C++ to synthesizable RTL modules in SystemVerilog
- Functional verification and unit test development using Verilator
- Formal verification using JasperGold
- Adjusting constraints according to synthesis results

## CentraleSupélec, Cesson-Sévigné

Final Year Internship | March 2022 - September 2022

- RTL design and development in VHDL for the NGD circuit
- · Using Matlab for the optimization of digital filter
- Implementing the digital NGD prototype on Zyng-7000 SoC

# Rcospi, Le Loroux-Bottereau

Internship | June 2021 - September 2021

- Programming in C language on Microchip microcontroller and ESP32
- PCB design on Eagle PCB

## **EDUCATION**

# Polytech Nantes, Nantes

Engineering Degree | Graduated in 2022 Specialization: Electronics and Digital Technologies

#### South China University of Technology, Guangzhou

Bachelor's Degree, Automation | Graduated in 2020

# University of Technology Sydney, Sydney

Summer Campus, Data Science topic | July 2017 - August 2017

47 rue Marcel Bonnet 94230 Cachan, France +xx xxxxxxxxxx scutliubaili@gmail.com



# **HDL** and **Programming** Languages

**VHDL** \*\*\*\* SystemVerilog \*\*\*\* C++/C \*\*\*\* Verilog \*\*\*\* Pvthon \*\*\*\* TCL \*\*\*\*

# Verification & Simulation

Xcelium, Verdi, Modelsim, JasperGold

#### **Tools & Platforms**

Xilinx Vivado, Cadence Genus, Libero

#### **Microcontrollers**

Microchip Studio, ESP32

# **Protocols & Communication Buses**

Ethernet, I2C, SPI, UART, AMBA, **AVALON** 

## **Version Control Tools**

Git, SVN

#### **Others**

Matlab, Makefile, Script shell, Confluence, Jira

## **LANGUAGES**

• English: Complete professional proficiency

• French: Complete professional proficiency

• Chinese: Native language

## **INTERESTS**

- Badminton
- Go (Weigi)