



SL. No. 24(F)

40200

## ANSWER SCRIPT

08 JUN 2024

Dept. of Electronic &amp; Telecommunications Engineering

09 JUN 2024

Dept. of Electronic &amp; Telecommunications Engineering

Question No.	Marks Allocated	Marks Obtained	Remarks
1		—	
2		—	
3		5 + 3	
4		2.5 + 5	
5		0 + 1.5	
6			
7			
8			
9			
10			
Total		17	

Signature of Examiner

Matric/ID No. : T221008 ID No. (In Words) : T-Two-Two-One-Zero-Zero-Eight

Semester :  Spring.  Autumn. Section: A

Academic Year : 2024 .....  Mid-Term Exam.  Final Exam.

Program : BSc in ETE Semester Enrolled : 5th

Course Title : Microprocessor & Peripherals

Course Code : ETE-3543 Date of Exam : 09-06-2024

Signature of Invigilator with date

No.	Serial Number of Additional Answer script	Signature of Invigilator
1		
2		
3		
4		
5		
6		

## PART-B

Ans. to the que. No. 03(a)

Software - ~~that's the stored instruction~~

- ⇒ They are caused using the writing,
- ⇒ Software interrupts are 8 types
- ⇒ Software interrupts all are the same priority ~~not~~ ⇒ It's can be masked

⇒ RST0 → ~~RST7 output bus~~

- ⇒ They are specific address in vector form

Hardware -

- ⇒ They occurs ~~are~~ the external signal pins

- ⇒ Hardware interrupts are the 5 types

- ⇒ Hardware Interrupts are not a same priority

- ⇒ They are ~~not~~ specific address is not vector (INTR)

- ⇒ It's can be masked disable only TRAP

## Part-B

(D)  $\Rightarrow$  In the 8085 microprocessor 2T states are performed by the machine cycle performing to the checks for an interrupt.

$\Rightarrow$  List of the hardware and software interrupts.

Hardware

Software

- |         |        |   |      |
|---------|--------|---|------|
| 1) RST0 | -0000H | — | RST1 |
| 2) RST1 | -0008H | — | RST2 |
| 3) RST2 | -0010H | — | RST3 |
| 4) RST4 | -0018H | — |      |
| 5) RST5 | -0020H | — |      |
| 6) RST6 | -0028H | — |      |
| 7) RST7 | -0030H | — |      |
| 8)      | -0038H | — |      |

9) AT plus old zip

## LIST of the software & Hardware

### interrupts -

#### software

- 1) RST 0 — 0000H
- 2) RST 1 — 0008H
- 3) RST 2 — 0010H
- 4) RST 3 — 0018H
- 5) RST 4 — 0020H
- 6) RST 5 — 0028H
- 7) RST 6 — 0030H
- 8) RST 7 — 0038H

#### hardware

- |                        | Hardware |
|------------------------|----------|
| 1) TRAP                |          |
| 2) RST 7-High priority | 024H     |
| 3) RST 6-H             | 003CH    |
| 4) RST 5-H             | 034H     |
| 5) RST 4-H             | 042CH    |
| 6) INTR - low priority | 002CH    |

Ans to. the que. No. 3 (b)

### TRAP -

- 1) TRAP are the part of a Hardware Interrupts
- 2) TRAP are the High priority
- 3) TRAP can not be masked
- 4) It's a vector address
- 5) TRAP vector address 024H

### RST 7.5 -

- 1) RST 7.5 part of the Hardware interrupts
- 2) RST 7.5 lower than TRAP
- 3) It's can be also DI instruction
- 4) It's can be masked
- 5) It's vector address 00BCH

6) Vector address 003CH

Ans. to the Que. No. 4 (a)

Given that,  $\boxed{0\ 0\ 1\ 0\ 0\ 0\ 0\ 0}$

MVI A, XXH,

SIM, L of (b7H28M) & D

We know,

$D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1\ D_0$   
 $SOD\ SDE\ X\ [Reset]\ Masked\ M_{7-5}\ M_{6-5}\ M_{5-5}$

SOD - serial output data

SDE - serial data enable

X - Unused | 0 | 1

Reset - Reset R7-5

Masked - Masked of RSTIVM

M<sub>7-5</sub> - Masked RESET R7-5

M<sub>6-5</sub> - n n 6-5

M<sub>5-5</sub> - n n 5-5

# MVI instruction RST 6-5 & (a)

(a) RST 6-5. Shift left

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>L</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	0	0	1	0	1	1

D<sub>3</sub> (Masked) to ↑ MIG 4 2 1

D<sub>2</sub> (RST 6-5) to ↑ Masked

D<sub>0</sub> (RST 6-5) to ↑

In the binary method

calculate

$$\begin{array}{r}
 \text{old value} \\
 8 \quad 9 \quad 2 \\
 \text{new value} \\
 1 \quad 0 \quad 1 \\
 \hline
 \end{array}
 \quad 8 + 2 = 10$$

[MVI A, R1] - R1 = R2  
 [SIM, RE2] - RE2 = WORKER

R1 - N - N - R1 = R1

R1 - N - N - R1 = R1

## ~~(d) Process Control~~

⇒ Masking prevent to the instruction of disturbing of the process of the execution. It's important the job execution for masking.

when masking are disable but process masking execution are to the continue.

### Interrupts ~~to~~ software interrupts

are not a maskable. But hardware interrupts are the maskable without (TRAP)

TOF is a TRAP

Ans to the Que. No: 4(b)

~~SNT OF FAN 200M (S)~~

~~LOOP~~

MVI 40H ;

SIM

CALL DELAY

MVI C0H ;

SIM

CALL DELAY

JMP LOOP

HLT

DELAY

MVI C, COUNT ; FT

DEC C ; YT

JNZ LOOP ; IOT

RET

) IOT

$$\frac{1}{500} = 0.002 \\ = 2 \text{ msec}$$

Given that  $0.001 \text{ MHz}$   
 $= 1 \text{ msec}$

Assuming the 8085 microprocessor

in  $3 \text{ MHz}$   $T_d = 0.5 \times 10^{-3}$   
 $= 0.333 \times 10^{-6}$

calculation  $(\text{count} = \text{value})$

~~$0.5 \times 10^{-3} = 17T + (\text{value} \times 14T) - 3T$~~

~~$0.5 \times 10^{-3} = 17 \times 0.333 \times 10^{-6} + (\text{value} \times 14 \times 0.333 \times 10^{-6}) - 3 \times 0.333 \times 10^{-6}$~~

~~count = 706~~

~~$\approx 6 \text{ A H}$~~

using the STM instruction 20D

PIN

~~- count = 6 A H~~

Add it to the Ques No - 9 (b)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	0

I/O = I/O mode

(sub) M, PA = Mode of Port A

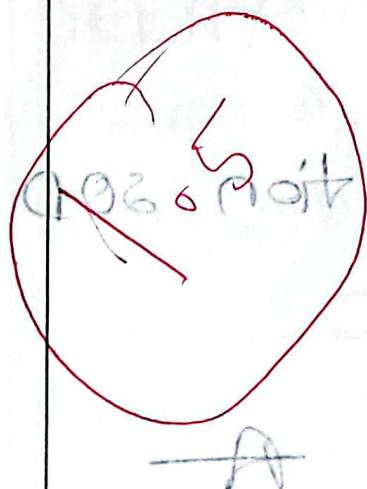
PAU = Port A input Upper

TE = (T1L + sub) + T2E INPUT MODE

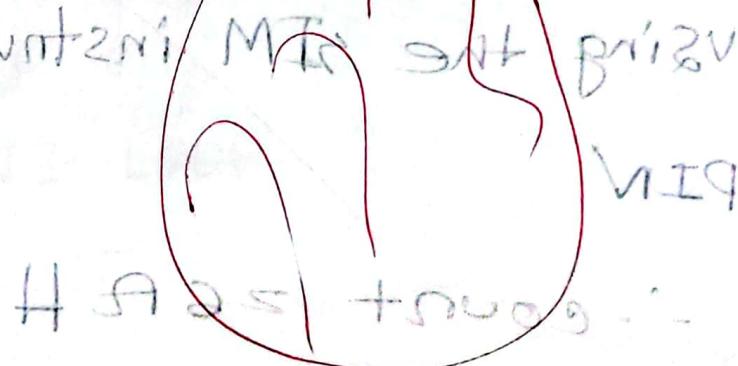
PBM = Port B output mode

PB = Port B output mode

PC = Port C lower input



HA2 =



⇒ BSR control word to set & reset PC<sub>3</sub> & PC<sub>5</sub> (3 & 5 no pin of port C) of 8255A

bits	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	PORT C
0 0 0.	00								
0 0 1	01								
0 1 0	02								
0 1 1	D <sub>3</sub>								
1 0 0	D <sub>4</sub>								
1 0 1	D <sub>5</sub>								
1 1 0	D <sub>6</sub>								
1 1 1	D <sub>7</sub>								

PC<sub>3</sub> 0110 *M*

PC<sub>5</sub> 100 *M*

	Mode 0	Mod 1	Mode 2
PORT A	✓	✓	X
PORT B	✓	✓	X



আন্তর্জাতিক ইসলামী বিশ্ববিদ্যালয় চট্টগ্রাম  
الجامعة الإسلامية 国际伊斯兰大学  
International Islamic University Chittagong

SL. No. 24 (B)

071628

## ANSWER SCRIPT

08 JUN 2024

Dept. of Electronic &  
Telecommunications Engineering

09 JUN 2024

Dept. of Electronic &  
Telecommunications Engineering

Question No.	Marks Allocated	Marks Obtained	Remarks
1		—	
2		—	
3		3 + 4	
4		52 + 5	
5		0 + 0	
6			
7			
8			
9			
10			
Total		14	

Signature of Examiner

Matric/ID No. : T221001 ID No. (In Words) : T-two-two-one-zero-zero-one

Semester :  Spring.  Summer  Autumn. Section : AAcademic Year : 2024 .....  Mid-Term Exam.  Final Exam.

Program : BSc. in ETE Semester Enrolled : 5th

Course Title : Microprocessor and Peripherals

Course Code : ETE - 3593 Date of Exam : 09/06/2024

Signature of Invigilator with date

No.	Serial Number of Additional Answer Script	Signature of Invigilator
1	89917	.....
2		
3		
4		
5		
6		

Ans To The Q:- No - 3 (a)

Interrupt architecture:

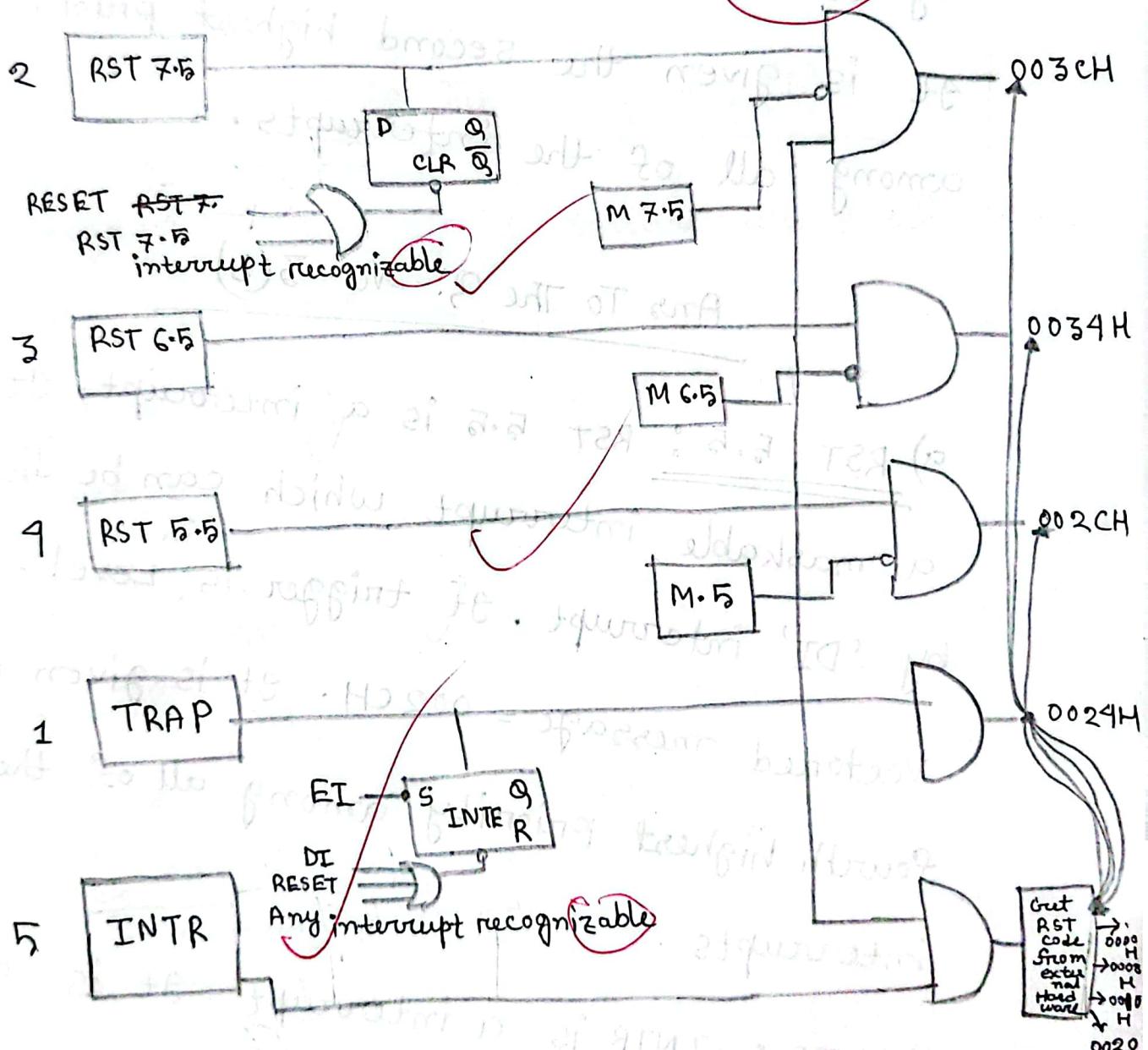


Fig :- Interrupt Structure

RST 7.5: RST 7.5 is a interrupt. It is a maskable interrupt which can be disable by 'DI' interrupt. Vectored message = 003CH. It is given the second highest priority among all of the interrupts.

Ans To The Q:- No - 3(b)

a) RST 5.5: RST 5.5 is a interrupt. It is a maskable interrupt which can be disable by 'DI' interrupt. If trigger is Level - vectored message = 002CH. It is given the fourth highest priority among all of the interrupts.

b) INTR: INTR is a interrupt. It is a non-maskable interrupt but it can be disable by 'DI' interrupt. It trigger is

in Level . It is a non-vector interrupt among all of the interrupts. It is given as the last priority among all the interrupts .



Ans To The Q:- No - 4 (b)

\* Program to generate a square wave of 0.001 MHz using SOD pin .

TFD = PM

TPE = PH

Program

Loop:  
MVI B, 40H ;

SIM

CALL DELAY

MVI B, COH ;

SIM

CALL DELAY

JMP Loop ;

DELAY :

```
MVI C, COUNT ; 7T
BACK: DCR C ; 4T ]  
JNZ BACK ; 10T ] NT
RET ; 10T ] MT
```

$$MT = 17T$$

$$NT = 19T$$

Assuming clock frequency,  $T = 3\text{MHz}$

$$= 0.333 \times 10^{-6} \text{ ms}$$

square wave generate of =  $0.001\text{MHz}$

$$= 0.001 \times 10^6 \text{ Hz}$$

$$= 1\text{kH}\zeta$$

So,

Time delay will be,  $T_D = 0.5 \text{ sec}$ .

We know,

$$T_D = MT + [(COUNT)_{10} \times NT] - 3T$$

$$\Rightarrow 0.5 \text{ sec} = 17 \times 0.333 \times 10^{-6} + [(count)_{10} \times 19 \times 0.333 \times 10^{-6}] - 3 \times 0.333 \times 10^{-6}$$

$$\Rightarrow 0.5 \text{ sec} = 5.661 \times 10^{-6} + [(count)_{10} \times 4.662 \times 10^{-6}] - 9.99 \times 10^{-7}$$

$$\Rightarrow [(count)_{10} \times 4.662 \times 10^{-6}] = -5.661 \times 10^{-6} + 9.99 \times 10^{-7} + 0.5$$

$$\Rightarrow [(count)_{10} \times 4.662 \times 10^{-6}] = 0.499$$

$$\Rightarrow count_{10} = \frac{0.499}{4.662 \times 10^{-6}}$$

$$\Rightarrow count_{10} = 10^6$$

$$\therefore count = 6AH$$

(Ans.)

Ans To The Q:- No - 4(a)

Masking: Masking is the process where we enable use 'EI' instruction to enable a interrupt.

Masking is required because we have to enable or disable all of the 5 basic pins for interrupt (TRAP RST 7.5, RST 6.5, RST 5.5); TRAP and INTR is non maskable interrupt.

Given instruction:-

MVI A, XXH ;

SIM ;

We can write this <sup>example</sup> as following program:-

MVI A, XXH ;

SIM ;

CALL DELAY

EI SIM ;

MVI A, XXH ;

EI ;

HLT ;

MVI A, 00H ; Hand address of RST 5.5  
SIM ;  
CALL DELAY ;  
SIM ;  
MVI A, 01H ;  
SIM ;  
EI ;  
HLT ;

Here we can say that RST 5.5 and RST 6.5 are masked.

SIM operation : By doing this we loaded the value of 'MVI A, 00H' at the accumulator. It enables the RST 5.5 ; which is now masked.

RST 5.5 Enable : By ~~do~~ By loading the value of 'MVI A, 01H' at the accumulator we use SIM (Set Interrupt Mask) operation which enables the RST 5.5 ; which is now masked.

EI : It means Enable Interrupt, which makes the interrupt 5.5 & 6.5 maskable.

HLT: It means halt the program.

It is done by this process:

Bit 1 : Masked  $\rightarrow$  RST 6.5.

Bit 1 : Masked  $\rightarrow$  RST 5.5.

$\therefore$  The value of XXH in MVI instruction

is OFH.

— x —

Ans To The Q:- No - 5 (b)

Given configuration of 8255A :-

i) 8255 A would be in I/O mode

ii) Port A would be output under mode 1

iii) Port B would be input under mode 1.

composing control word for the given configuration:

i) Port A

• Output (Mode - 1)

• sequence (PA<sub>6</sub>, PC<sub>5</sub>, PC<sub>6</sub>, PC<sub>7</sub>)

2) Port B

- gInput (Mode - 1)
- Sequence ( $D_0, D_1, D_2$ )

3) Port C (upper)

- gInput
- sequence ( $PC_4, PC_5$ )

4) Port C (lower)

- gInput
- sequence ( $PC_0, PC_1, PC_2$ )

∴ The control word for the given code  
word will be  $CW = 94$ .



9 JUN 2024

pt. of Electronic &  
Communications Engineering  
Semester

# আন্তর্জাতিক ইসলামী বিশ্ববিদ্যালয় চট্টগ্রাম

## جامعة دولية إسلامية - سنتا خوفخ

### International Islamic University Chittagong

89917

#### Additional Answer Script SL No. 19 (A)

Trimester:  Spring  Summer  Autumn Academic Year: 20.24

ID No.: T221001 Course Code : ETE - 3593

SL. No. of original Script : 071628

Signature of Invigilator with date

Writing should be started right from here

Writing a BSR control code word to set and reset PC3 & PC5 (3&5 no pin of Port C) of

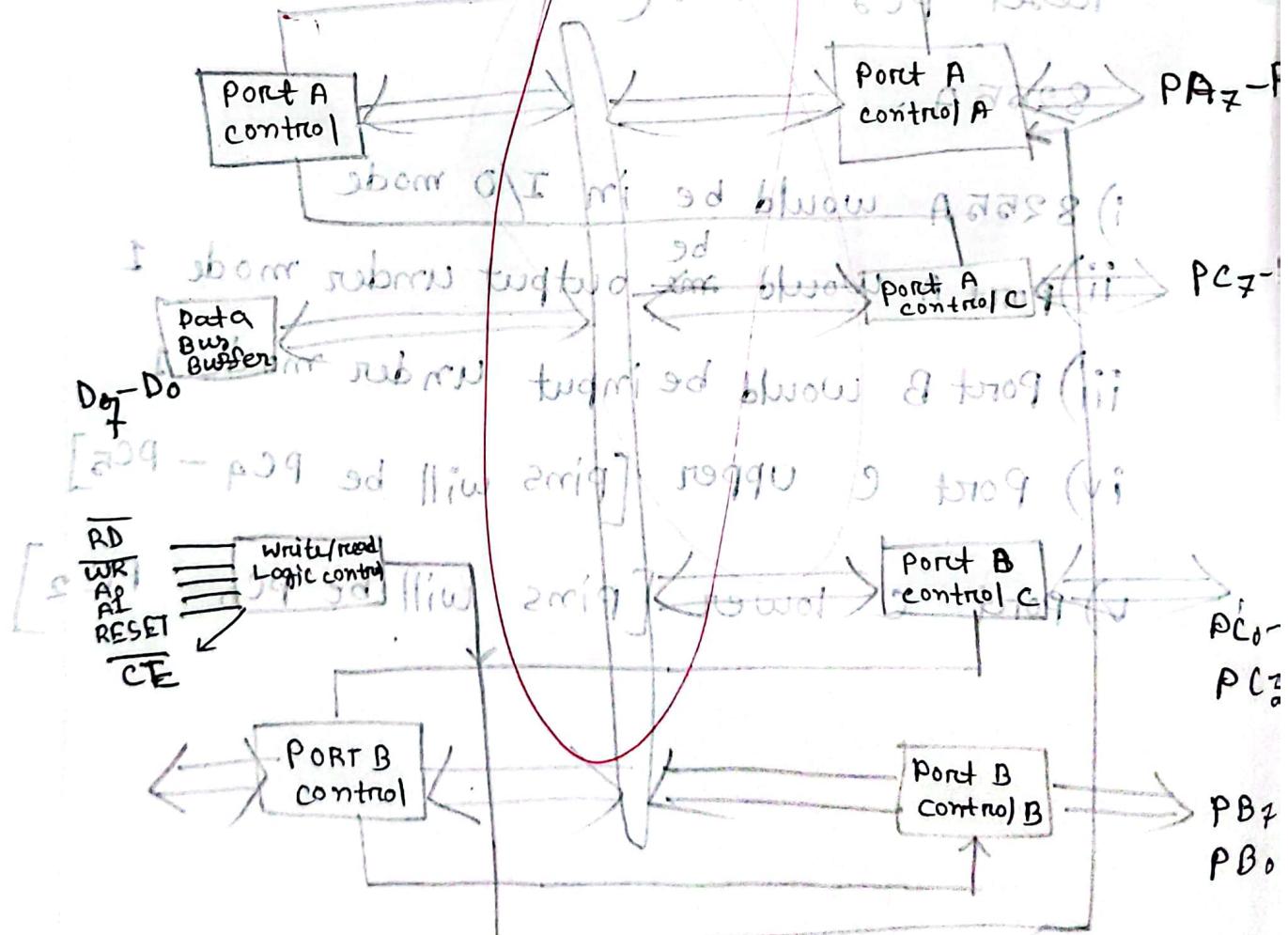
- i) 8255A would be in I/O mode
- ii) Port A would be output under mode 1
- iii) Port B would be input under mode 1
- iv) Port C upper pins will be PC9 - PC5
- v) Port C lower pins will be PC8 - PC2

Ans To The Q:- No - 5(a)

Functions of Handshake signals for  
8255 - based devices.

For, 8255-based devices we get two ports A and B which controls another port C.

20 (3) There is also a Data bus buffer.



# PART-B



## আন্তর্জাতিক ইসলামী বিশ্ববিদ্যালয় চট্টগ্রাম جامعة إسلامية دولية - بنغلاديش

International Islamic University Chittagong

SL. No. 24 (B)

071747

### ANSWER SCRIPT

09 JUN 2024

Dept. of Electronic &  
Telecommunications Engineering



Question No.	Marks Allocated	Marks Obtained	Remarks
1		—	
2		—	
3		1 + 1	
4		0 + 0	
5		0 + 0	
6			
7			
8			
9			
10			
Total		2	

Signature of Examiner

Matric/ID No. : T221020 ID No. (In Words) : T - two - two - one zero zero two

Semester :  Spring.  Summer  Autumn. Section : ..... A .....

Academic Year : 2024 .....  Mid-Term Exam.  Final Exam.

Program : BSC in ETE ..... Semester Enrolled : ..... 5th .....

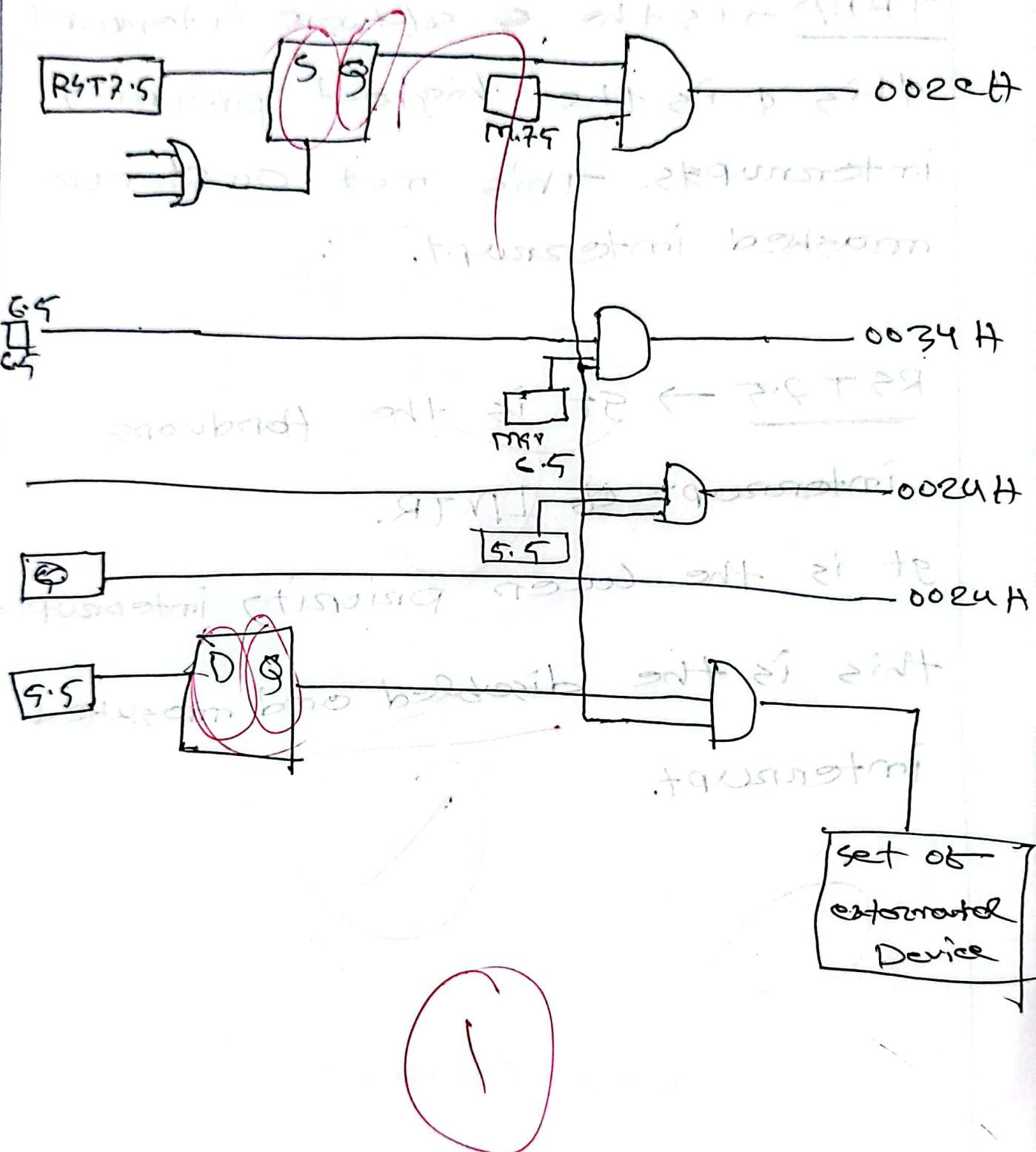
Course Title : microprocessor And peripherals .....

Course Code : ETE - 3543 ..... Date of Exam : 09 - 06 - 2024 .....

Signature of Invigilator with date  
09/06/2024

No.	Serial Number of Additional Answer Script	Signature of Invigilator
1		
2		
3		
4		
5		
6		

Ans to the que no: 3(a)



Ans to the sum 3(b)

TRAP → is the ~~software~~ interrupt  
this ~~is~~ is the highest priority  
interrupts. This ~~not~~ and ~~nor~~  
masked interrupt.

RST 2.5 → ~~It~~ is the hardware  
interrupt. of INTR.

~~gt~~ is the lower priority interrupt.  
this is the disabled and masked  
interrupt.

Ams to the sum no. q(6) b

Ams,

~~MVI A, 01H~~

MVI A, 03H;

out 85 H;

MVI B, 05H;

MVI 80H;

MVI C, 06H;

0

out 86H;

MVI A, 03H;

out 80H;

HL T ;

$$Ld = 7T + (14T \times 255) + 9T$$

=