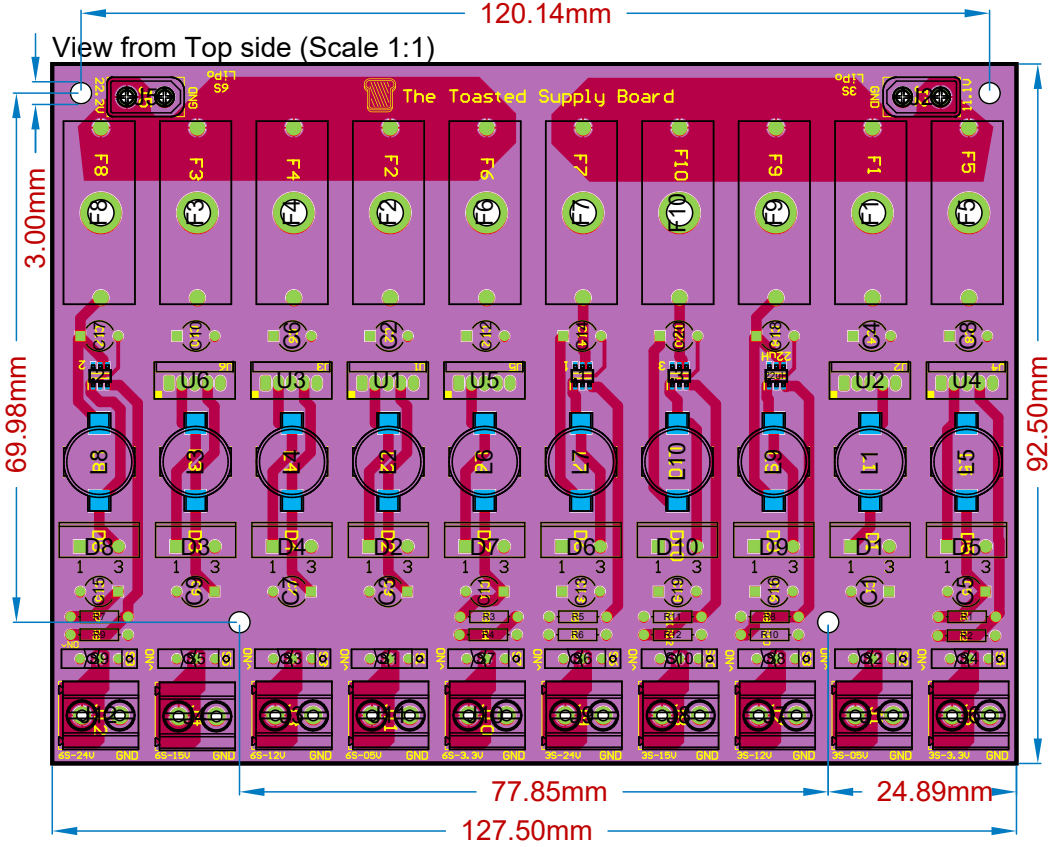
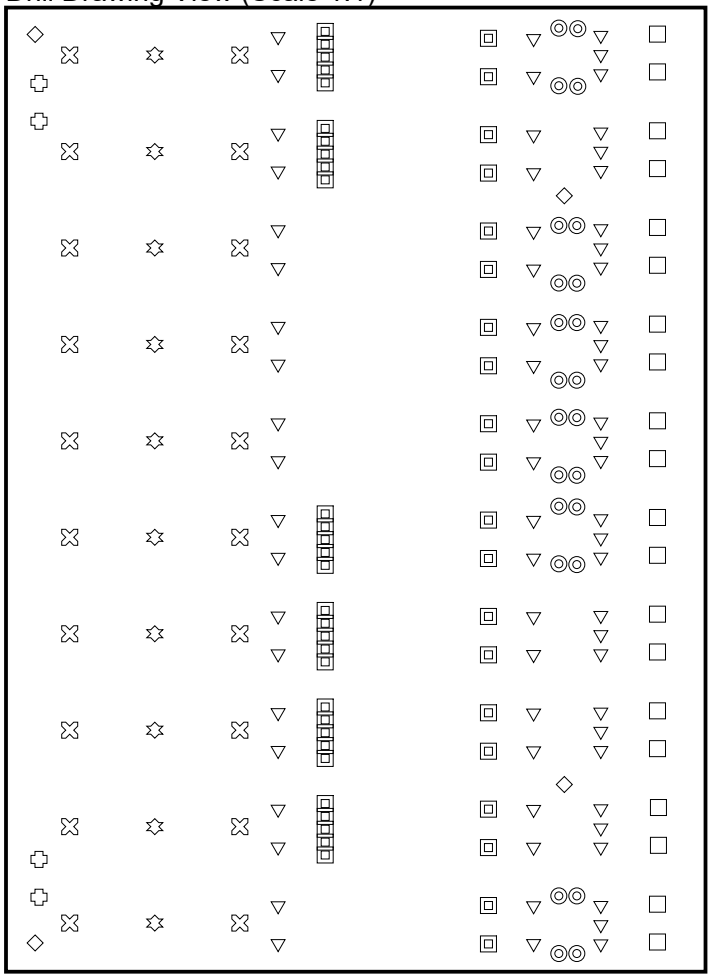
View from Top side (Scale 1:1)



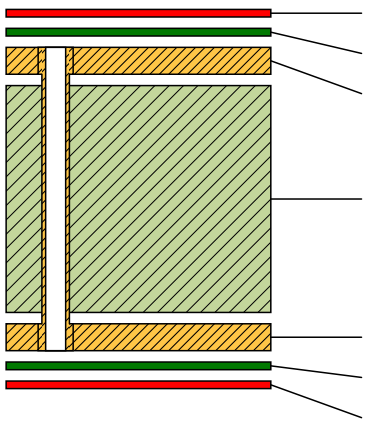
Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
▽	70	0.80mm	Plated	
◎	24	0.85mm	Plated	
⧈	50	1.10mm	Plated	
⊠	20	1.32mm	Plated	
□	20	1.60mm	Plated	
⯐	4	1.80mm	Plated	
◇	4	3.00mm	Non-Plated	
✡	10	3.65mm	Plated	
	202 Total			

Drill Drawing View (Scale 1:1)

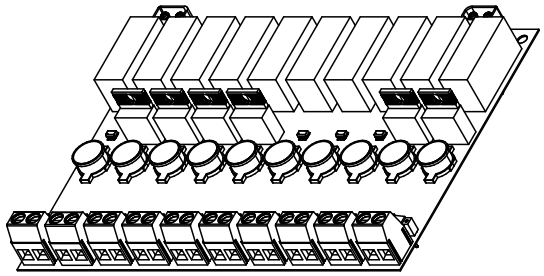


Layer Stack Legend



Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.01mm	Solder Resist	Solder Mask	GTS
Copper	**Top Layer**	**0.04mm**		**Signal**	**GTL**
		0.32mm	*FR-4*	*Dielectric*	
Copper	**Bottom Layer**	**0.04mm**		**Signal**	**GBL**
Surface Material	Bottom Solder	0.01mm	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

Total thickness: 0.41mm

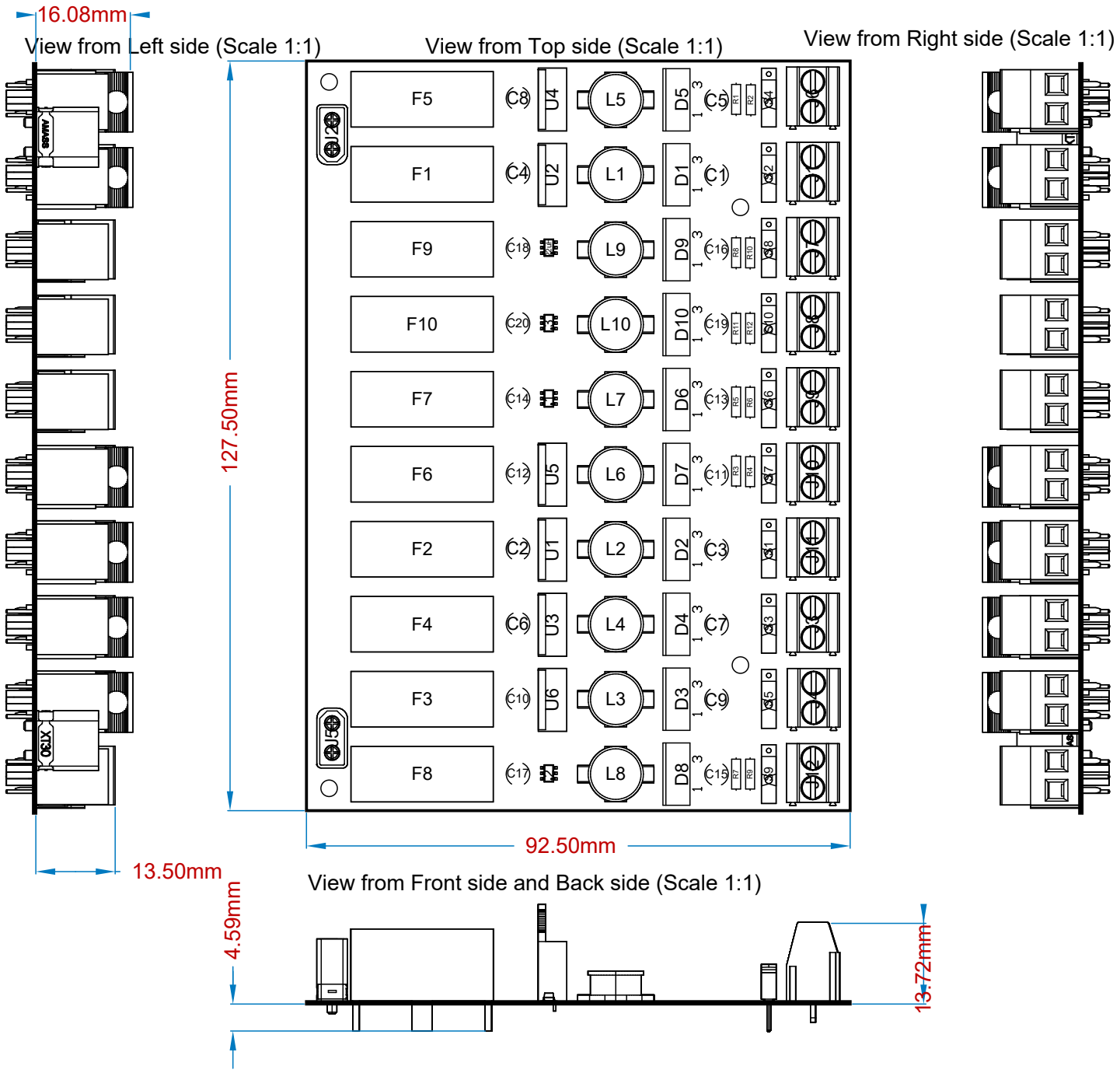


The Toasted Power Board

Fabrication Notes: UNLESS OTHERWISE SPECIFIED.

1. FABRICATE PER IPC-6012A CLASS 2.
2. FOR BOARD THICKNESS AND IMPEDANCE DETAILS REFER STACKUP DOCUMENT.
3. PRINTED WIRING BOARD SHALL COMPLY WITH REQUIREMENTS OF ANSI/J-STD-003.
4. SURFACE FINISH: IMMERSION SILVER
5. SILK SCREEN LEGEND TO BE APPLIED PER LAYER STACKUP USING WHITE NON-CONDUCTIVE EPOXY INK.
6. THIS PRINTED WIRING BOARD IS DESIGNED WITH A MINIMUM CONDUCTOR WIDTH AND SPACING OF 4 MIL & 4 MILS.
7. ALL VIAS ARE TENTED ON BOTH SIDES UNLESS SOLDERMASK OPENED IN GERBER.
8. ALL VIAS ON PAD SHOULD BE FILLED WITH NON CONDUCTIVE EPOXY AND SURFACE SHOULD BE FLAT. FLATNESS TOLERANCE FOR VIA ON PADS: +0.000 /- 0.001 INCHES ON BOTH SIDES. THE MANUFACTURER IS REQUESTED TO SIZE PER THEIR SOLDERMASK TOLERANCE.
9. SOLDER MASK OPENING IS KEPT SAME SIZE AS PAD (1:1) FOR ALL COMPONENTS
10. VENDOR SHOULD FOLLOW ROHS COMPLIANT PROCESS AND Pb FREE FOR MANUFACTURING
11. MANUFACTURER'S IDENTIFICATION, DATECODE LETTER SHALL BE SILKSCREENED ON SOLDER SIDE OF THE BOARD.
12. TRACE WIDTH SHOULD BE ACCURATELY ETCHED. MAX TOLERANCE +/- 1 MIL
13. ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED.
14. FLATNESS REQUIREMENTS:
A. BOW AND TWIST OF ASSEMBLY SUB-PANEL OR SINGULATED PWB SHALL NOT EXCEED 0.7% OF LONGEST SIDE
B. TEST IN ACCORDANCE WITH THE CURRENT REVISION OF IPC-TM-650 2.4.22
15. LAYER TO LAYER REGISTRATION SHALL BE WITHIN +/-2 MIL

ASSEMBLY NOTES
Board Name: The Toasted Power Board
Rev: A
1. Assemble in accordance with IPC-A-610, current revision, Class 2.
2. Solder electrical connections per latest revision of IPC J-STD-001.
3. This assembly contains ESD sensitive components. Handle per ANSI/ESD S20.20.
4. RoHS compliance required: Yes.
5. Mark with current assembly revision.
6. Mount components with polarity and orientation as shown on component designators/silkscreen.


16.08mm
View from Left side (Scale 1:1)
View from Top side (Scale 1:1)
View from Right side (Scale 1:1)
127.50mm
92.50mm
13.50mm
View from Front side and Back side (Scale 1:1)
4.59mm
13.72mm
F5
F1
F9
F10
F7
F6
F2
F4
F3
F8
L5
L1
L9
L10
L7
L6
L2
L4
L3
L8
D5
D1
D9
D10
D6
D7
D2
D4
D3
D8
U4
U2
U6
U5
U1
U3
C8
C4
C18
C20
C14
C12
C2
C6
C10
C17
C5
C1
C16
C19
C13
C11
C3
C7
C9
C15
J1
J2

Bill Of Materials

Line #	Designator	Comment	Quantity
1	1, 2, 3, 4	MT3608	4
2	C1, C3, C5, C7, C9, C11	1000uF	6
3	C2, C4, C6, C8, C10, C12	100uF	6
4	C13, C14, C15, C16, C17, C18, C19, C20	22uF	8
5	D1, D2, D3, D4, D5, D6, D7, D8, D9, D10	Diode	10
6	F1, F2, F3, F4, F5, F6, F7, F8, F9, F10	Fuse Holder	10
7	J1, J3, J4, J6, J7, J8, J9, J10, J11, J12	Screw Terminal	10
8	J2, J5	XT30PB	2
9	J6, J10	20020316-G021B01LF	2
10	L1, L2, L3, L4, L5, L6	100uH	6
11	L7, L8, L9, L10	22uH	4
12	R1, R3	5.05K	2
13	R2, R4	3K	2
14	R5, R7	39K	2
15	R6, R9, R10, R12	1K	4
16	R8	19K	1
17	R11	24K	1
18	S1, S2, S3, S4, S5, S6, S7, S8, S9, S10	SPST Switch	10
19	U1, U2	LM2576HVT-5.0/NOPB	2
20	U3	LM2576HVT-12/NOPB	1
21	U4, U5	LM2576T-ADJ/NOPB	2
22	U6	LM2576HVT-15/NOPB	1

PS - The Material in line 9 is not needed

Realistic View