



EEE234

Digital Integrated Circuit Design

Project: 02

Professor: Dr. Praveen Meduri

Submitted by:-

Shrividhya Srinivasan

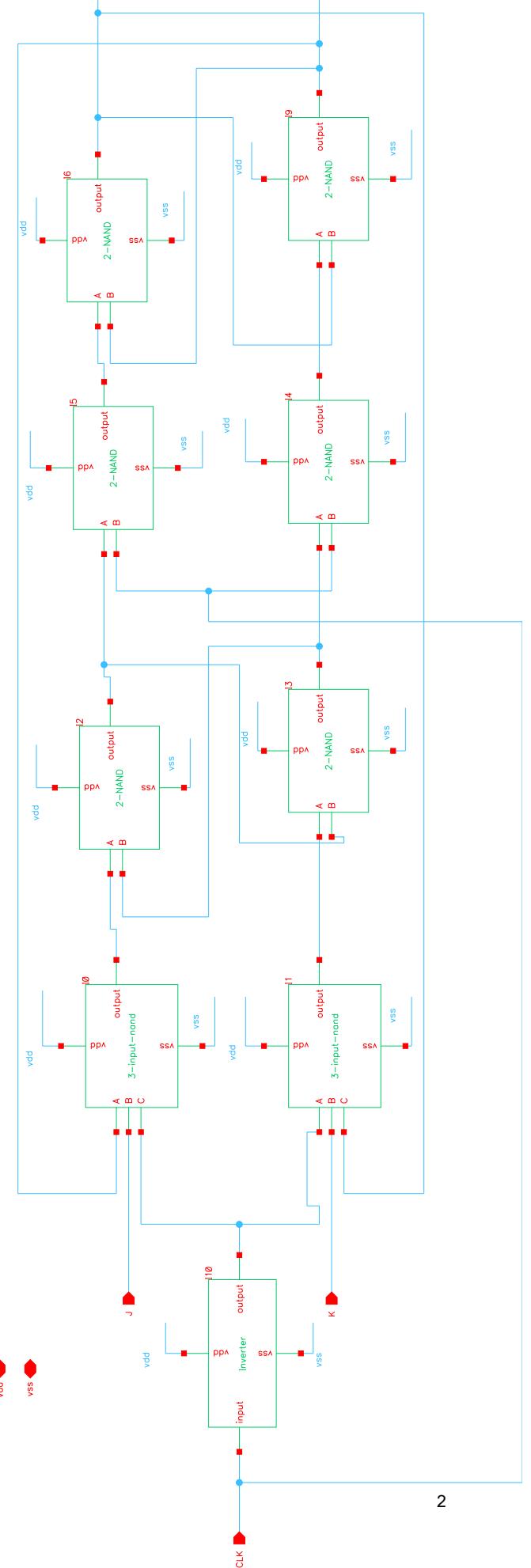
Omkar Kachare

Date of Submission: - 20th April 2019

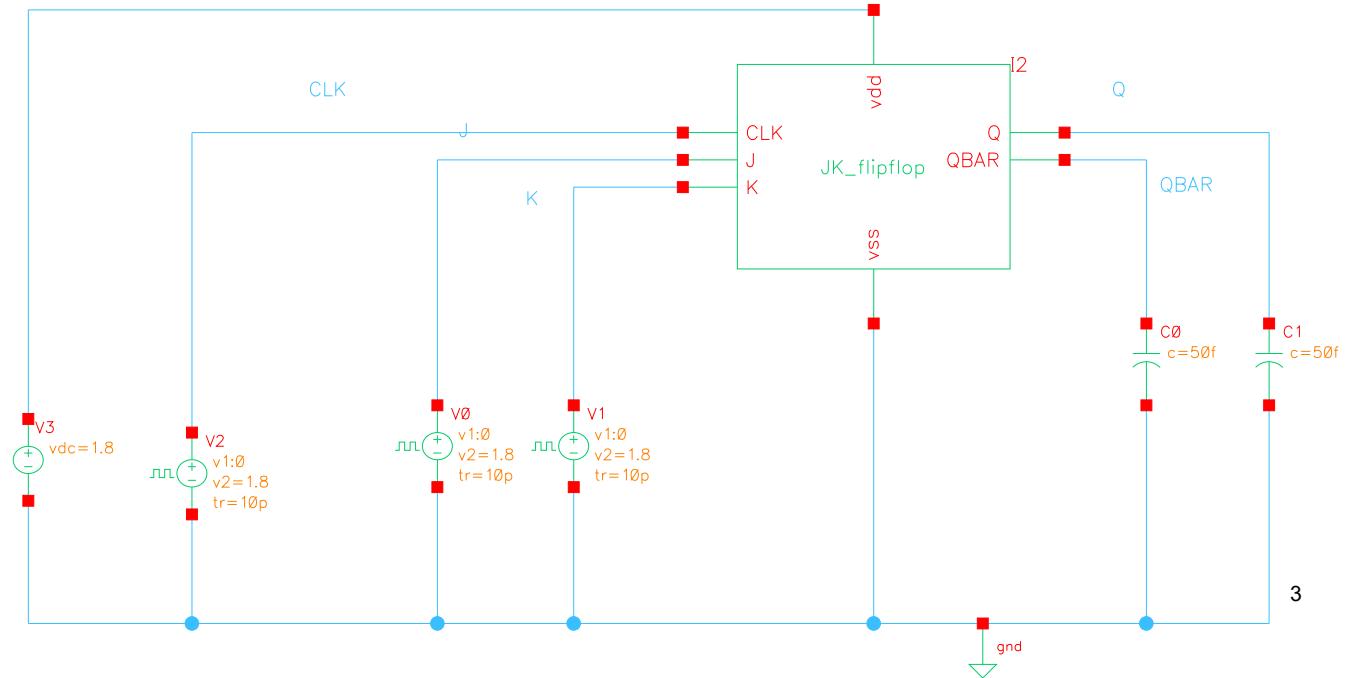
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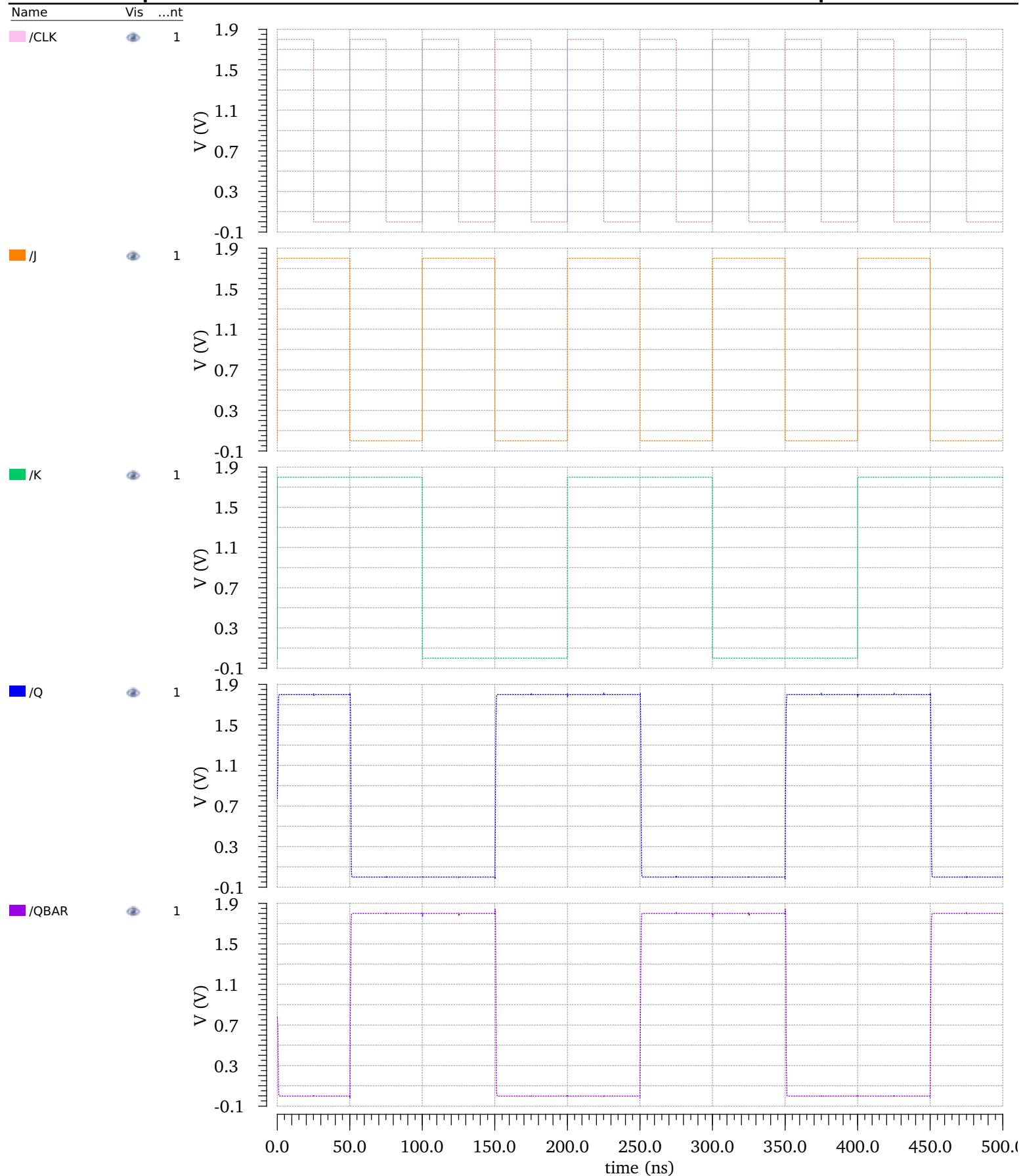
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JK Flip Flop Schematics

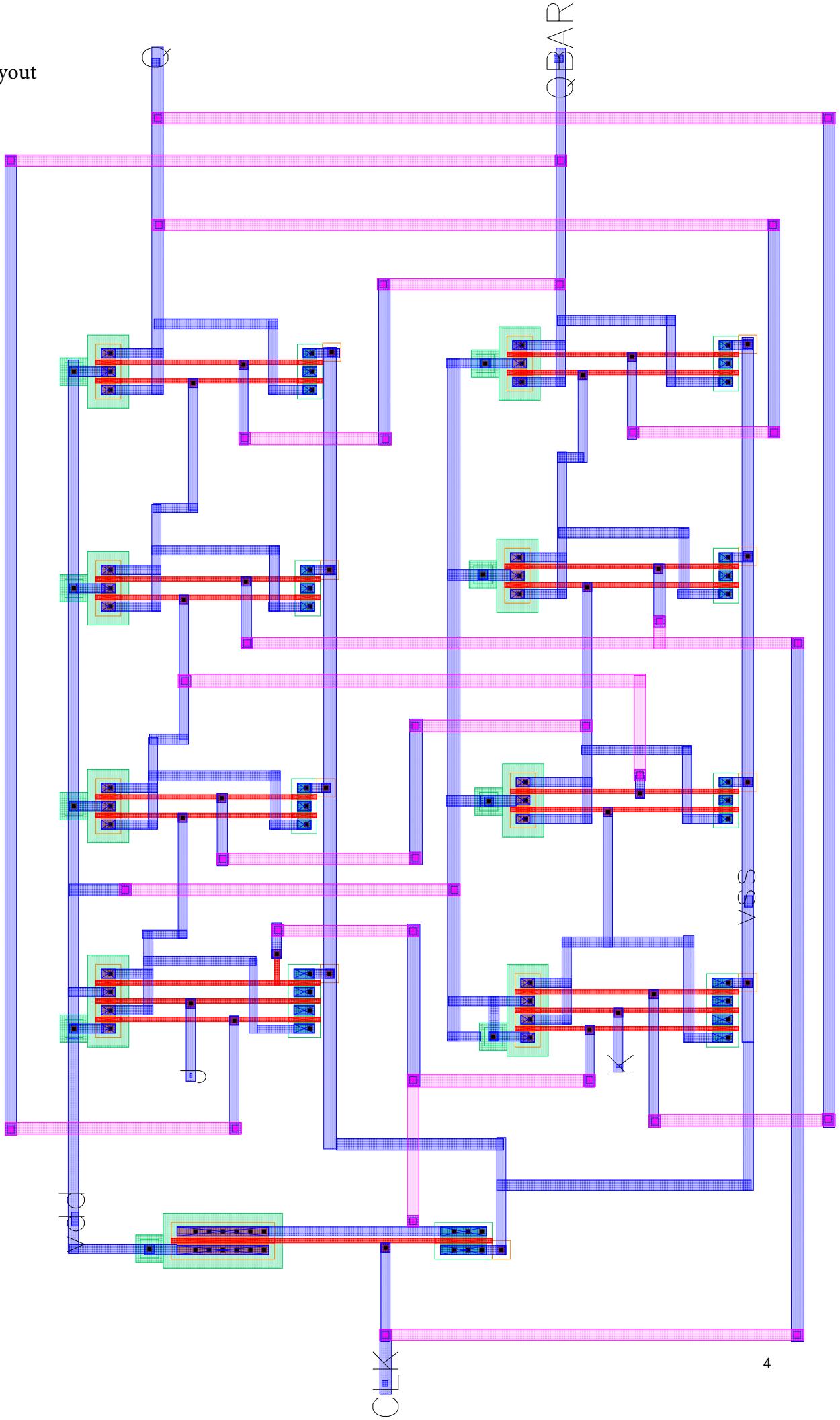


JK Flip Flop Testbench

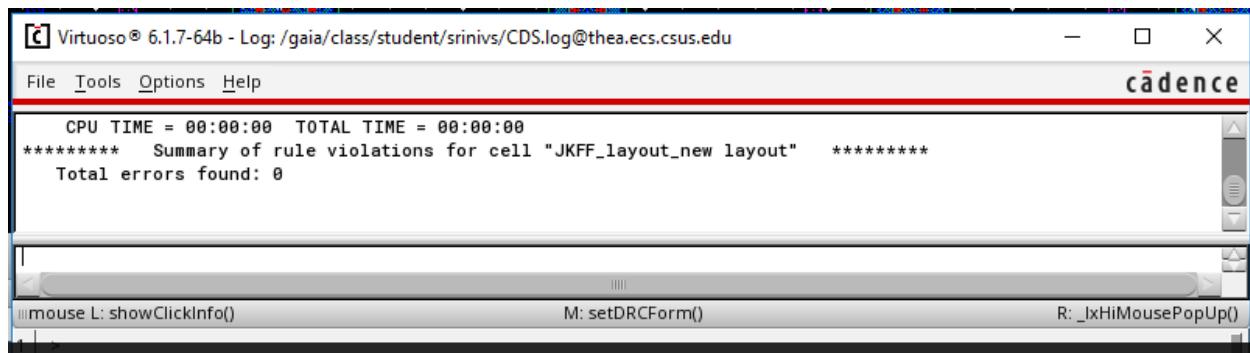


Transient Response**Wed Apr 17 14:31:35 2019**

JK Flip Flop Layout



JK Flip Flop DRC



JK Flip Flop LVS

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
```

Command line: /software/cadence/install/IC617/tools.lnx86/dfl/bin/64bit/LVS -dir
/gaia/class/student/srinivs/vlsi/Project1/LVS -l -s -t /gaia/class/student/srinivs/vlsi/Project1/LVS/layout
/gaia/class/student/srinivs/vlsi/Project1/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Net-list summary for /gaia/class/student/srinivs/vlsi/Project1/LVS/layout/netlist

count	
24	nets
7	terminals
19	pmos
19	nmos

Net-list summary for /gaia/class/student/srinivs/vlsi/Project1/LVS/schematic/netlist

count	
24	nets
7	terminals
19	pmos
19	nmos

Terminal correspondence points

N23	N13	CLK
N22	N2	J
N21	N1	K
N20	N7	Q

N18	N11	QBAR
N17	N9	vdd
N19	N4	vss

Devices in the netlist but not in the rules:

pmos nmox

The net-lists match.

layout schematic		
instances		
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	38	38
total	38	38

nets		
un-matched	0	0
merged	0	0
pruned	0	0
active	24	24
total	24	24

terminals		
un-matched	0	0
matched but different type	0	0

total 7 7

Probe files from /gaia/class/student/srinivs/vlsi/Project1/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/srinivs/vlsi/Project1/LVS/layout

devbad.out:

netbad.out:

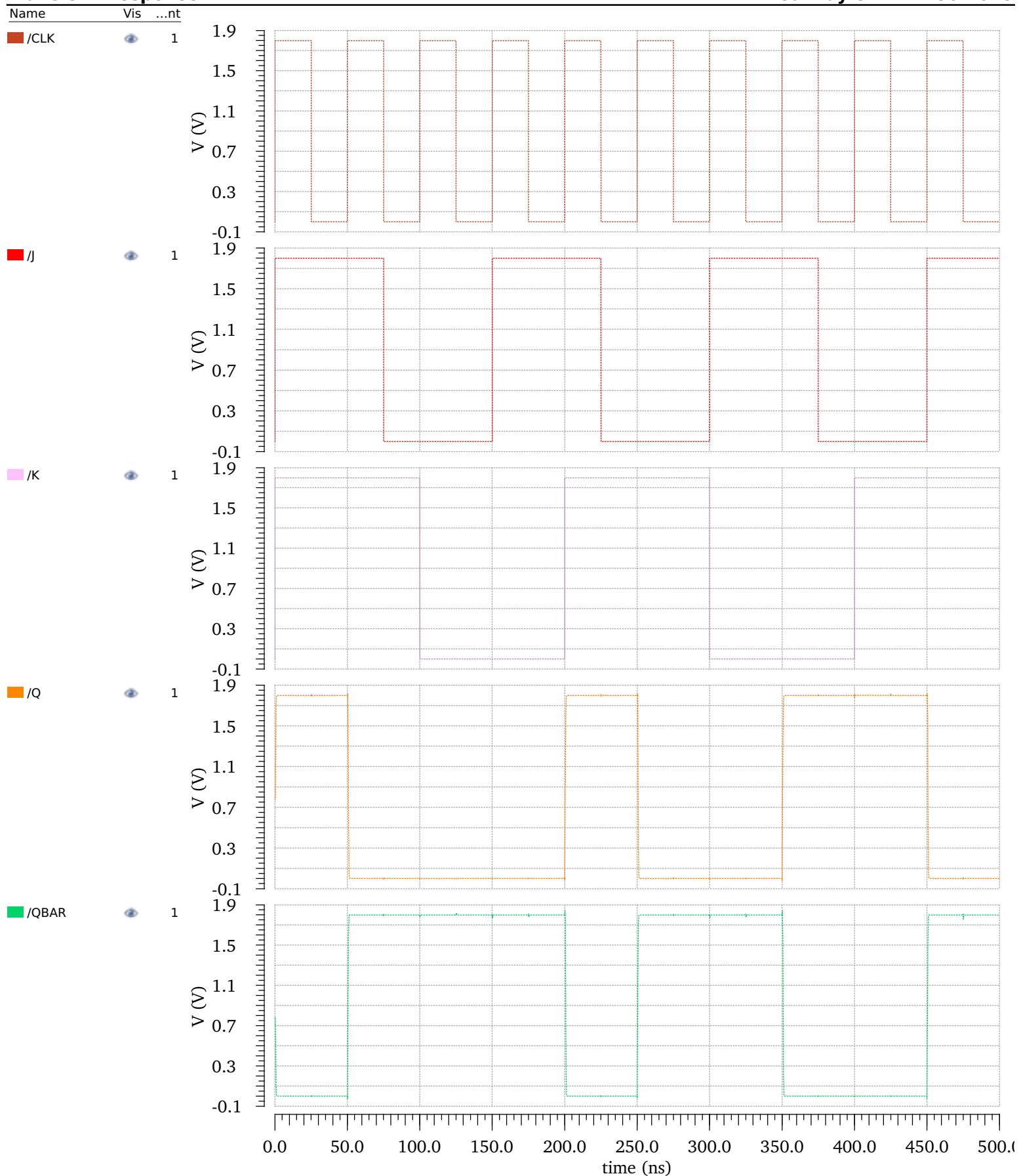
mergenet.out:

termbad.out:

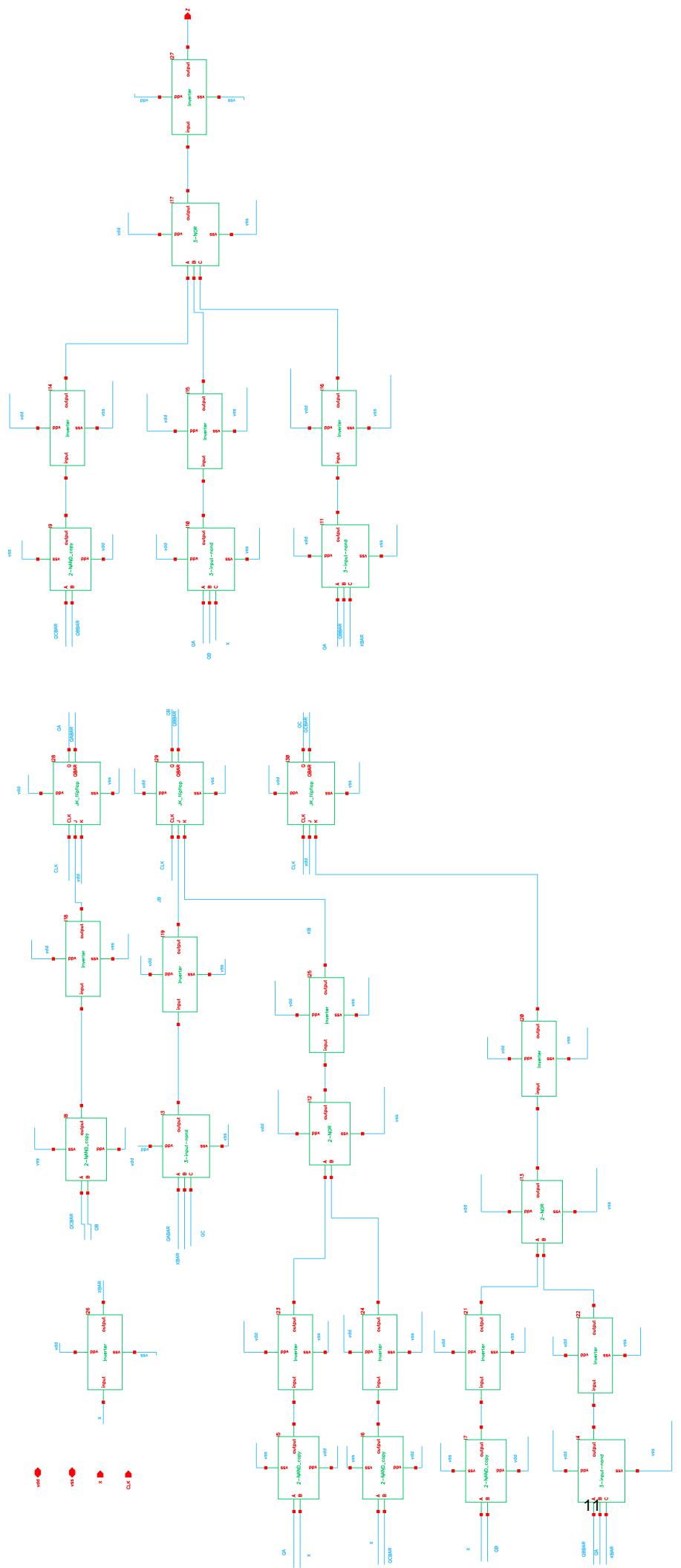
prunenet.out:

prunedev.out:

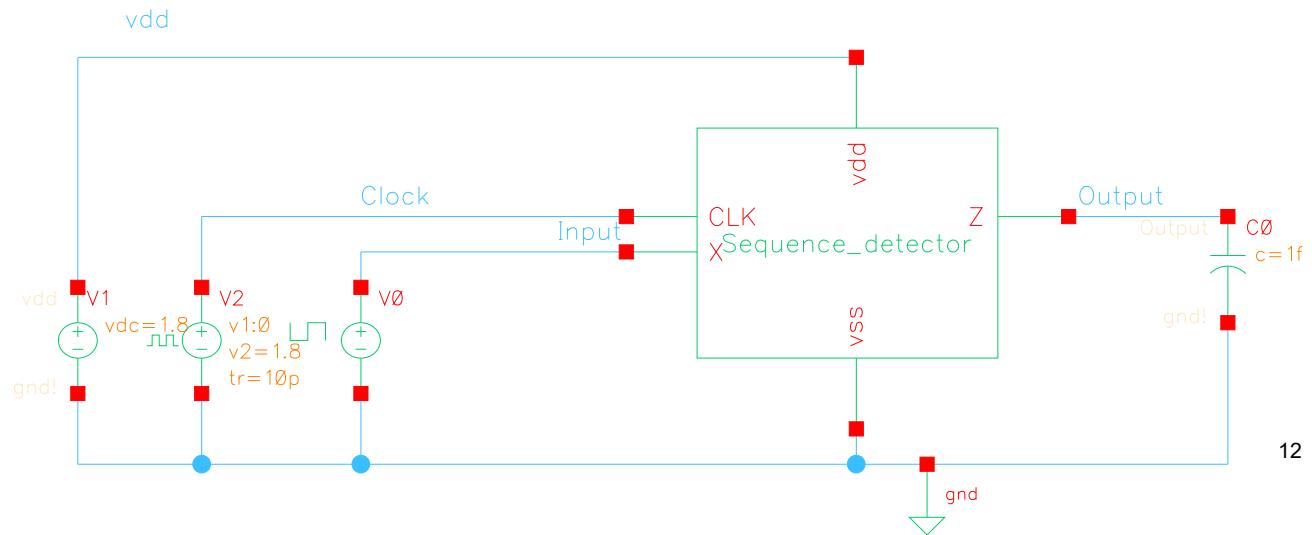
audit.out:

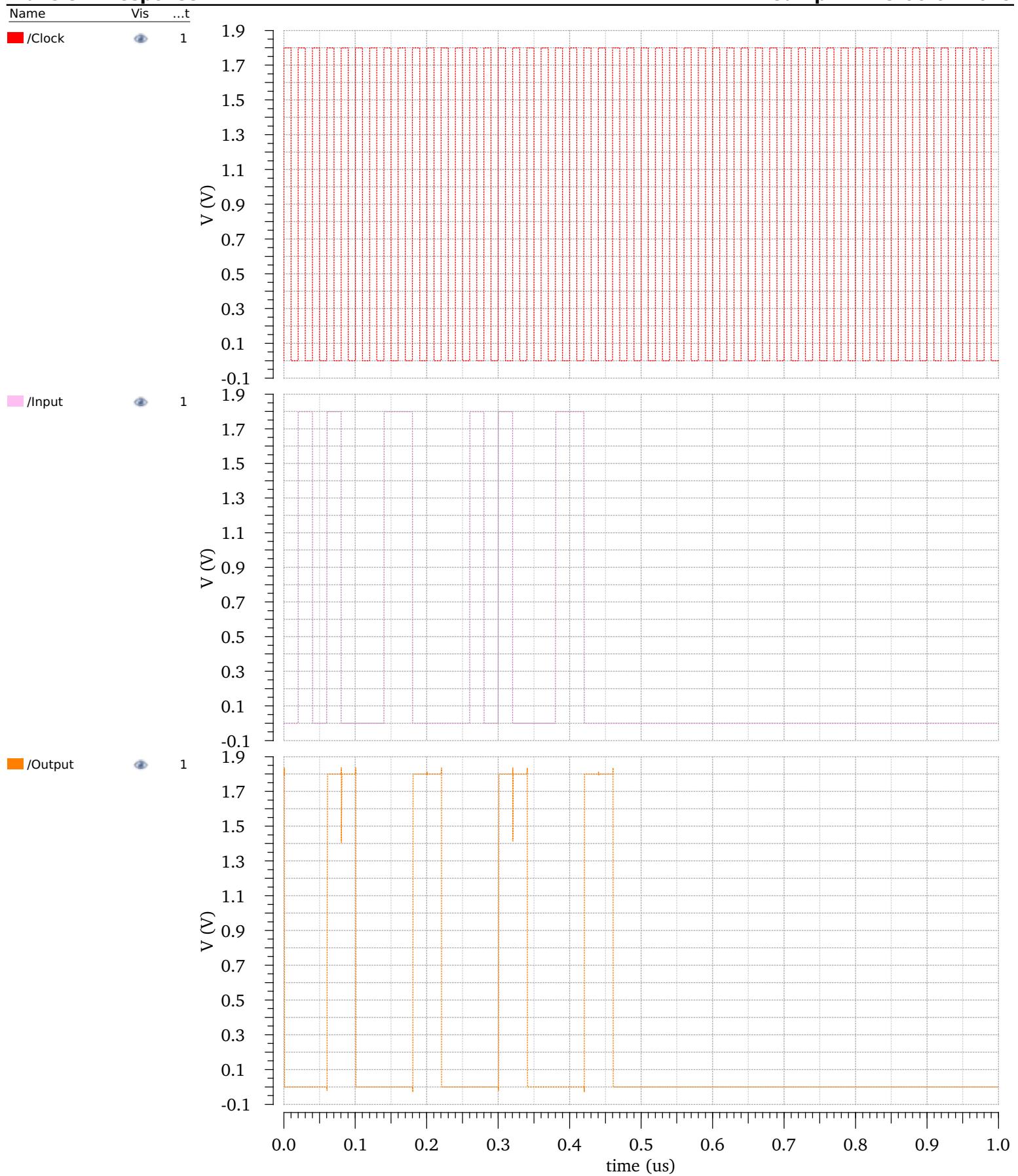
Transient Response**Wed May 8 22:12:50 2019**

Sequence Detector Schematic

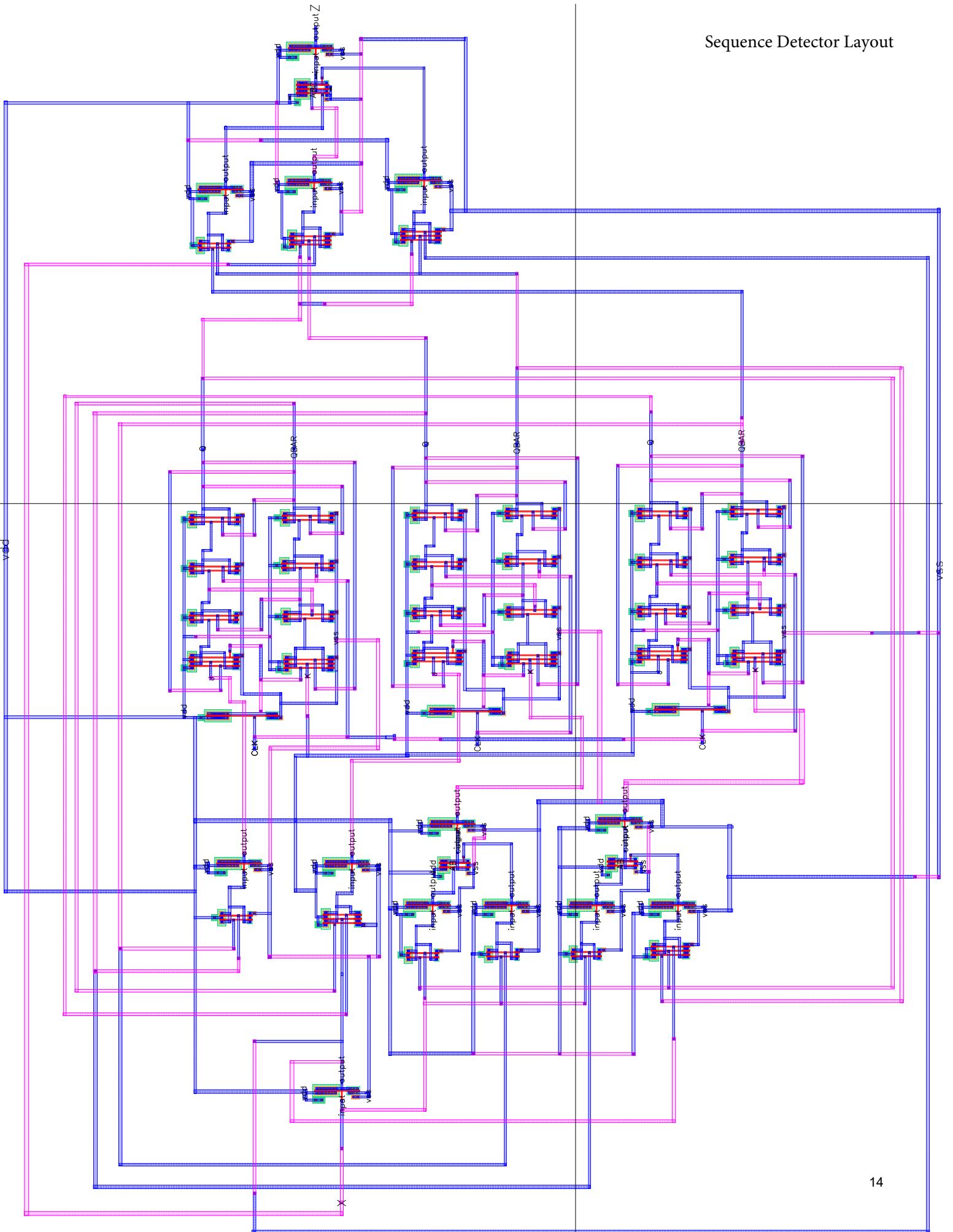


Sequence Detector Testbench

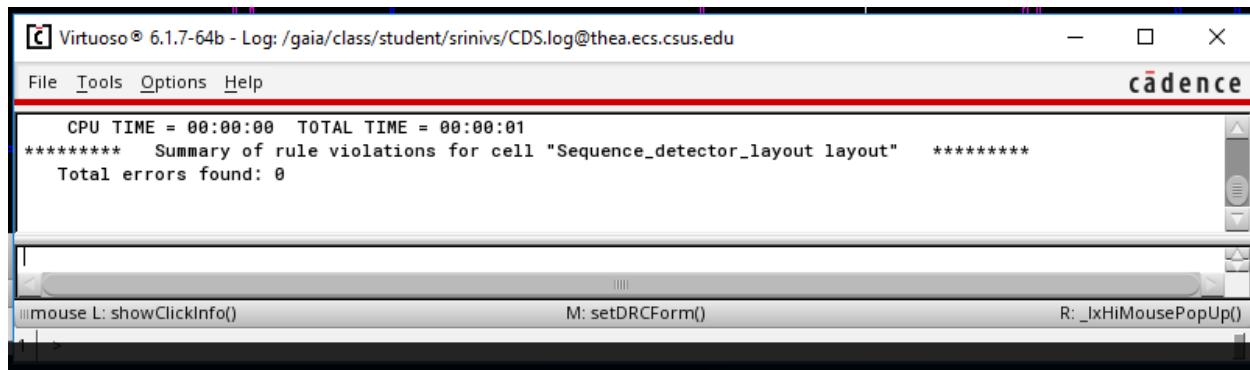


Transient Response**Wed Apr 17 15:06:01 2019**

Sequence Detector Layout



Sequence Detector DRC



Sequence Detector LVS

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
```

Command line: /software/cadence/install/IC617/tools.lnx86/dfl/bin/64bit/LVS -dir
/gaia/class/student/srinivs/vlsi/Project1/LVS -l -s -t /gaia/class/student/srinivs/vlsi/Project1/LVS/layout
/gaia/class/student/srinivs/vlsi/Project1/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Compiling Diva LVS rules...

Net-list summary for /gaia/class/student/srinivs/vlsi/Project1/LVS/layout/netlist

count	
103	nets
5	terminals
99	pmos
99	nmos

Net-list summary for /gaia/class/student/srinivs/vlsi/Project1/LVS/schematic/netlist

count	
103	nets
5	terminals
99	pmos
99	nmos

Terminal correspondence points

N102	N28	CLK
N100	N31	X
N99	N4	Z

N98 N33 vdd

N101 N3 vss

Devices in the rules but not in the netlist:

cap nfet pfet nmos4 pmos4

The net-lists match.

layout schematic

instances

un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	198	198
total	198	198

nets

un-matched	0	0
merged	0	0
pruned	0	0
active	103	103
total	103	103

terminals

un-matched	0	0
matched but		
different type	0	0
total	5	5

Probe files from /gaia/class/student/srinivs/vlsi/Project1/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/srinivs/vlsi/Project1/LVS/layout

devbad.out:

netbad.out:

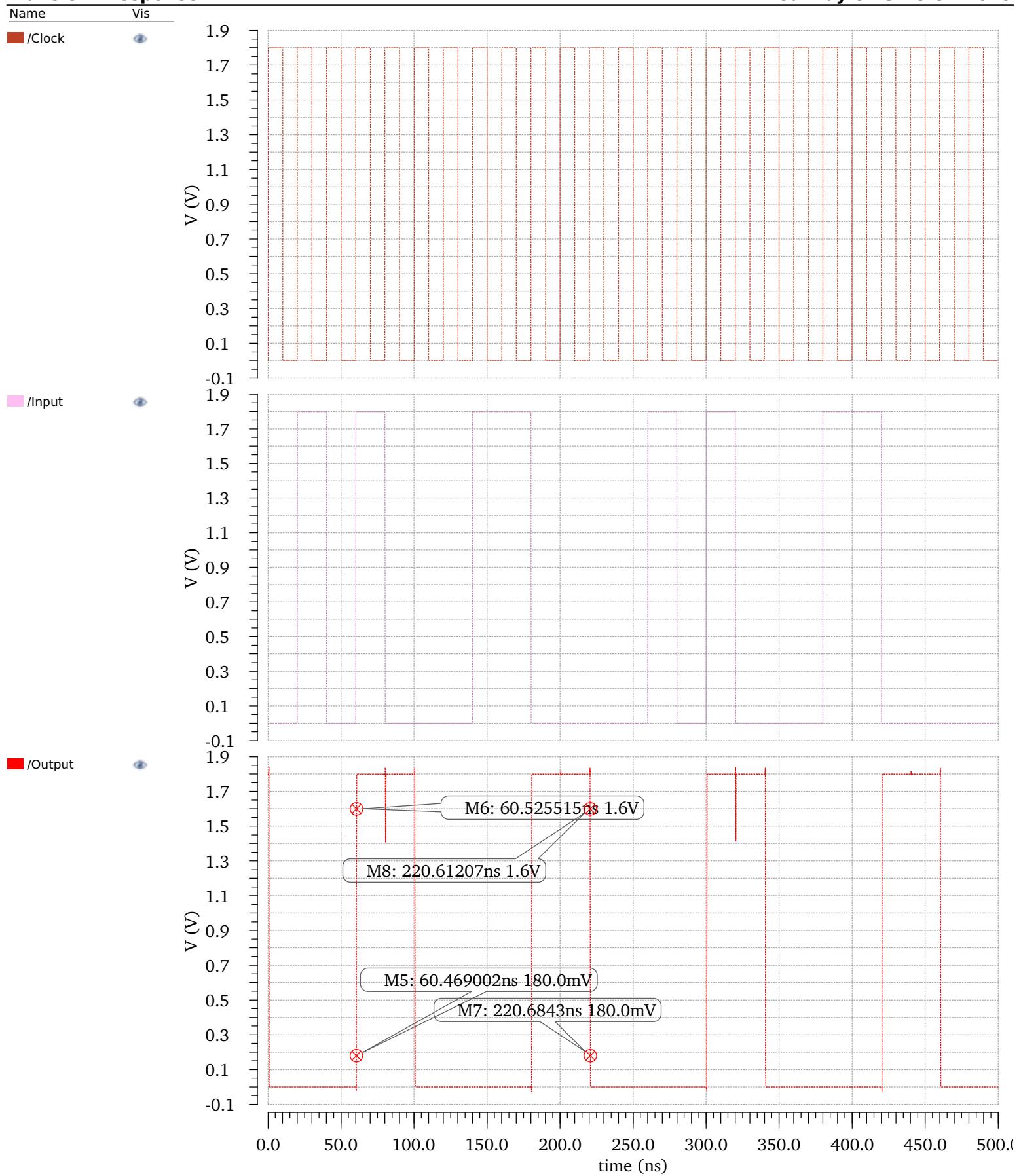
mergenet.out:

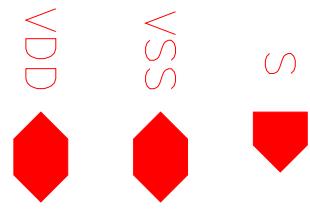
termbad.out:

prunenet.out:

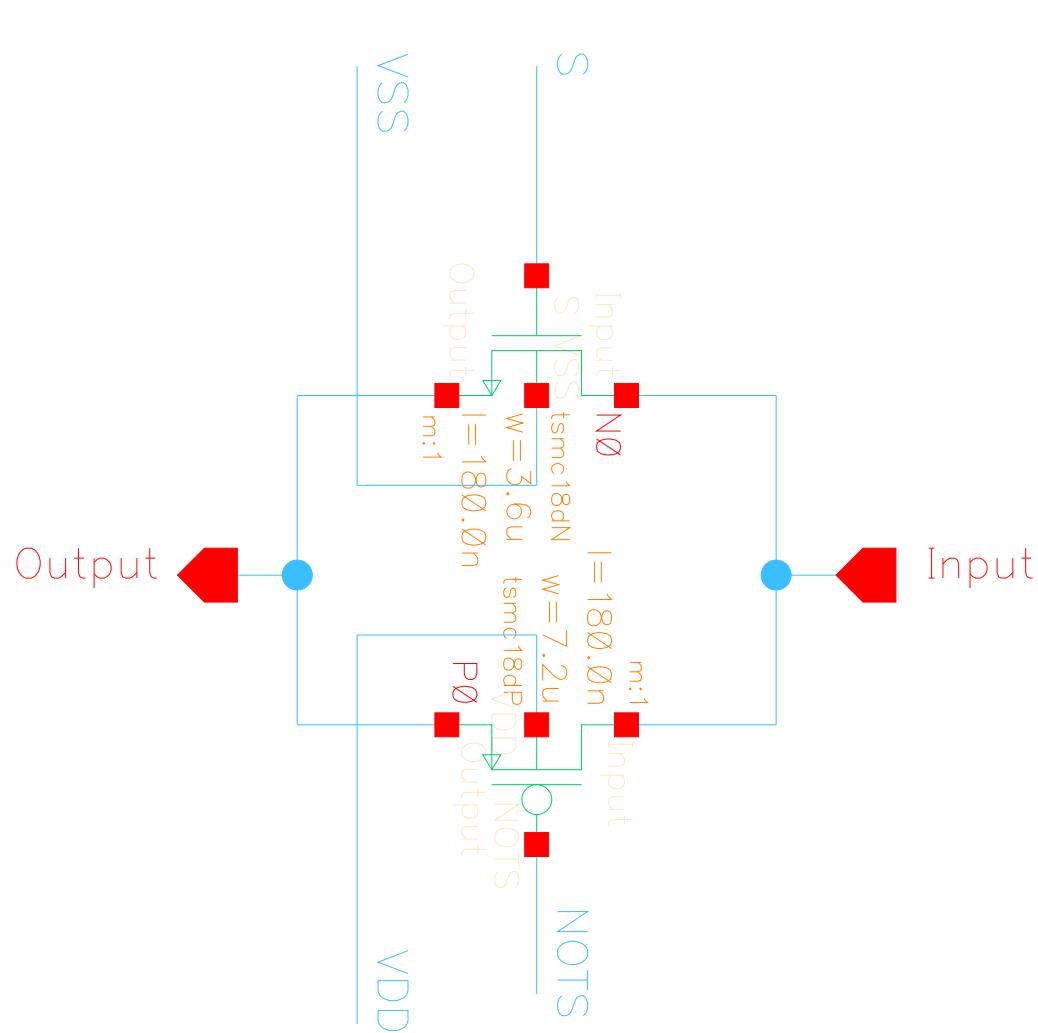
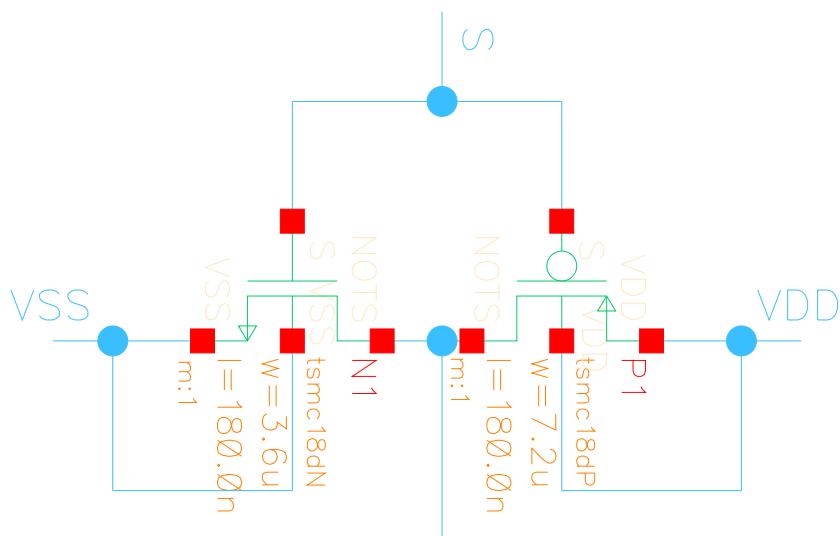
prunedev.out:

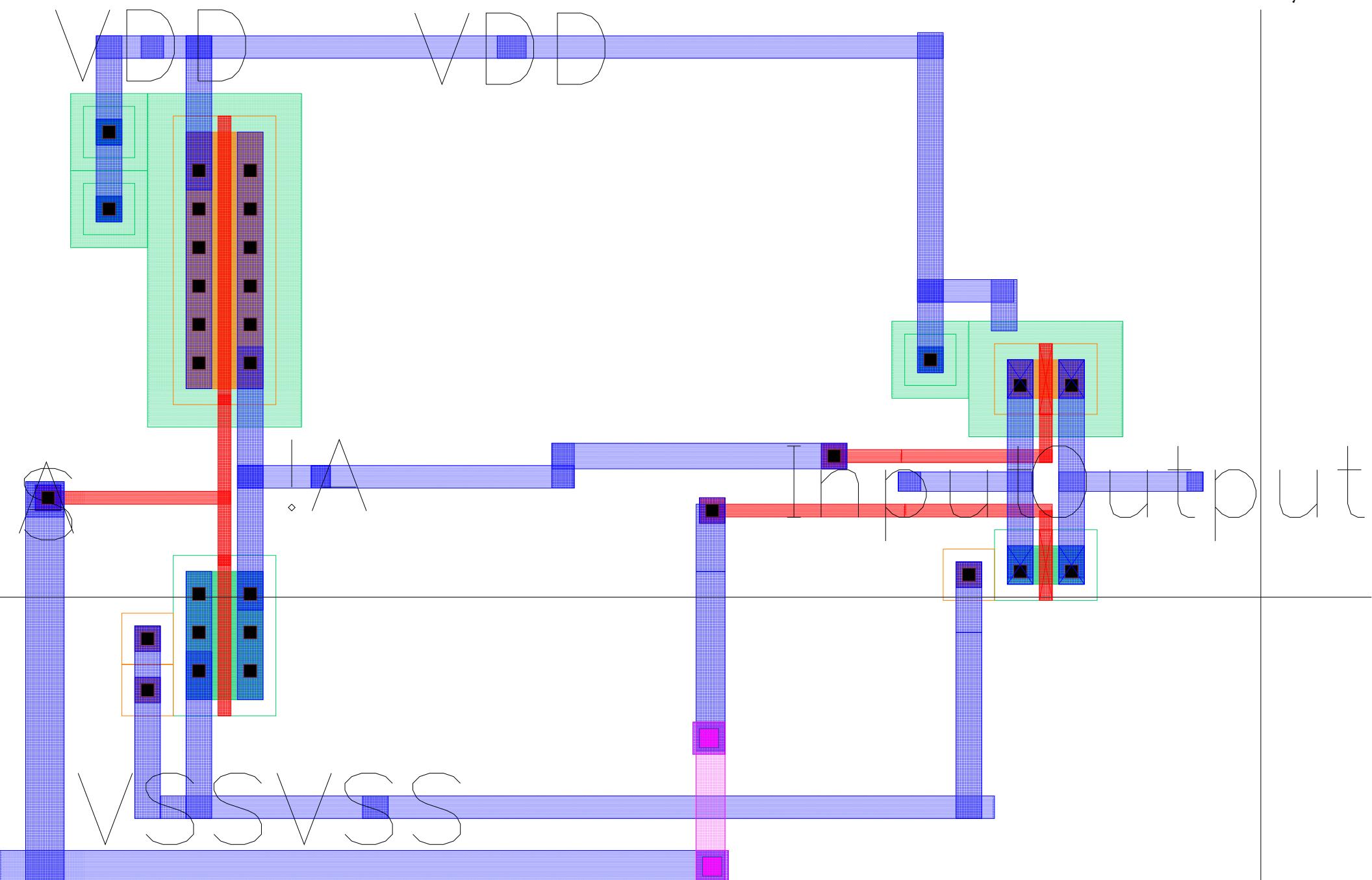
audit.out:

Transient Response**Wed May 8 13:25:37 2019**



Transmission Gate Schematic





File Tools Options Help

cadence

```
completed ....Wed May  8 12:21:00 2019
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
```

```
***** Summary of rule violations for cell "TXGATE_Layout layout" *****
Total errors found: 0
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
```

Command line:

```
/software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir  
/gaia/class/student/kachareo/EEE234/LVS -l -s -t  
/gaia/class/student/kachareo/EEE234/LVS/layout  
/gaia/class/student/kachareo/EEE234/LVS/schematic
```

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Net-list summary for
/gaia/class/student/kachareo/EEE234/LVS/layout/netlist

count	
6	nets
5	terminals
2	pmos
2	nmos

Net-list summary for
/gaia/class/student/kachareo/EEE234/LVS/schematic/netlist

count	
6	nets
5	terminals
2	pmos
2	nmos

Terminal correspondence points

N4	N5	Input
N2	N1	Output
N3	N4	S
N5	N2	VDD
N1	N3	VSS

Devices in the netlist but not in the rules:

pmos nmos

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	4	4
total	4	4

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	6	6

total	6	6
	terminals	
un-matched	0	0
matched but		
different type	0	0
total	5	5

Probe files from /gaia/class/student/kachareo/EEE234/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/kachareo/EEE234/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

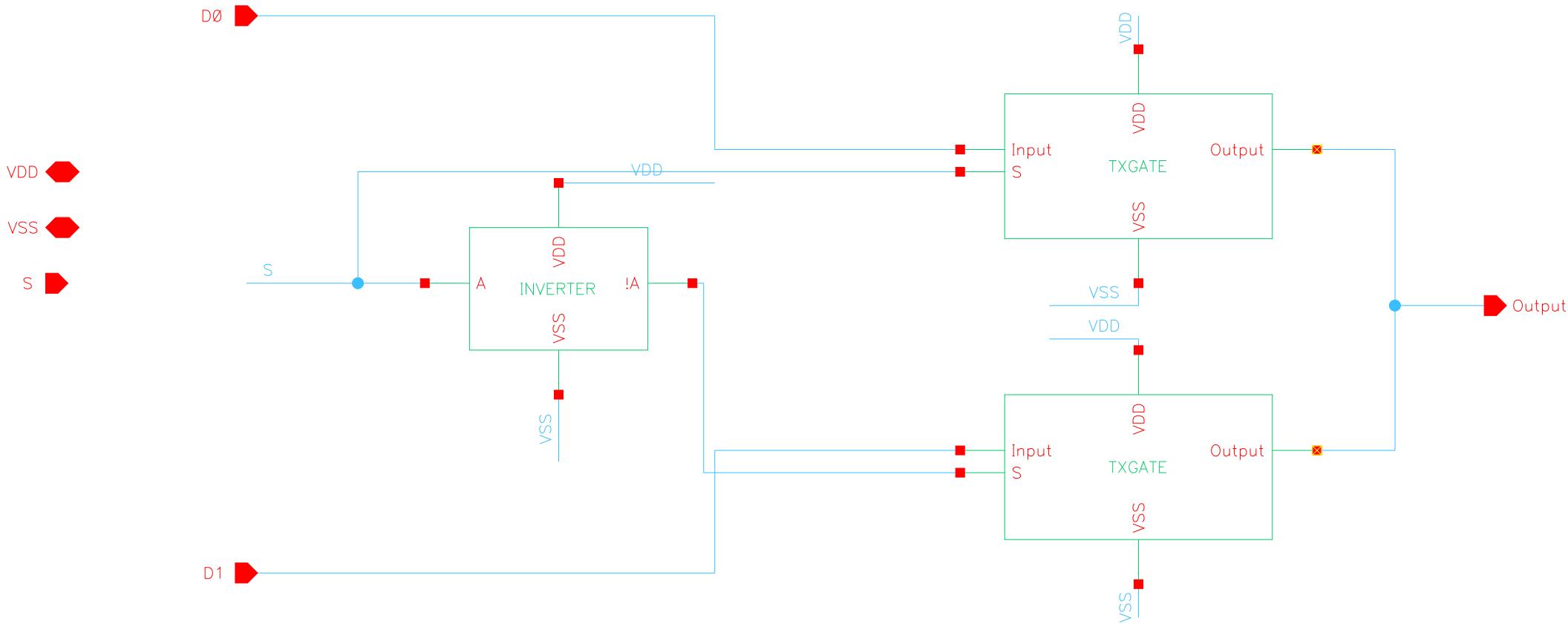
termbad.out:

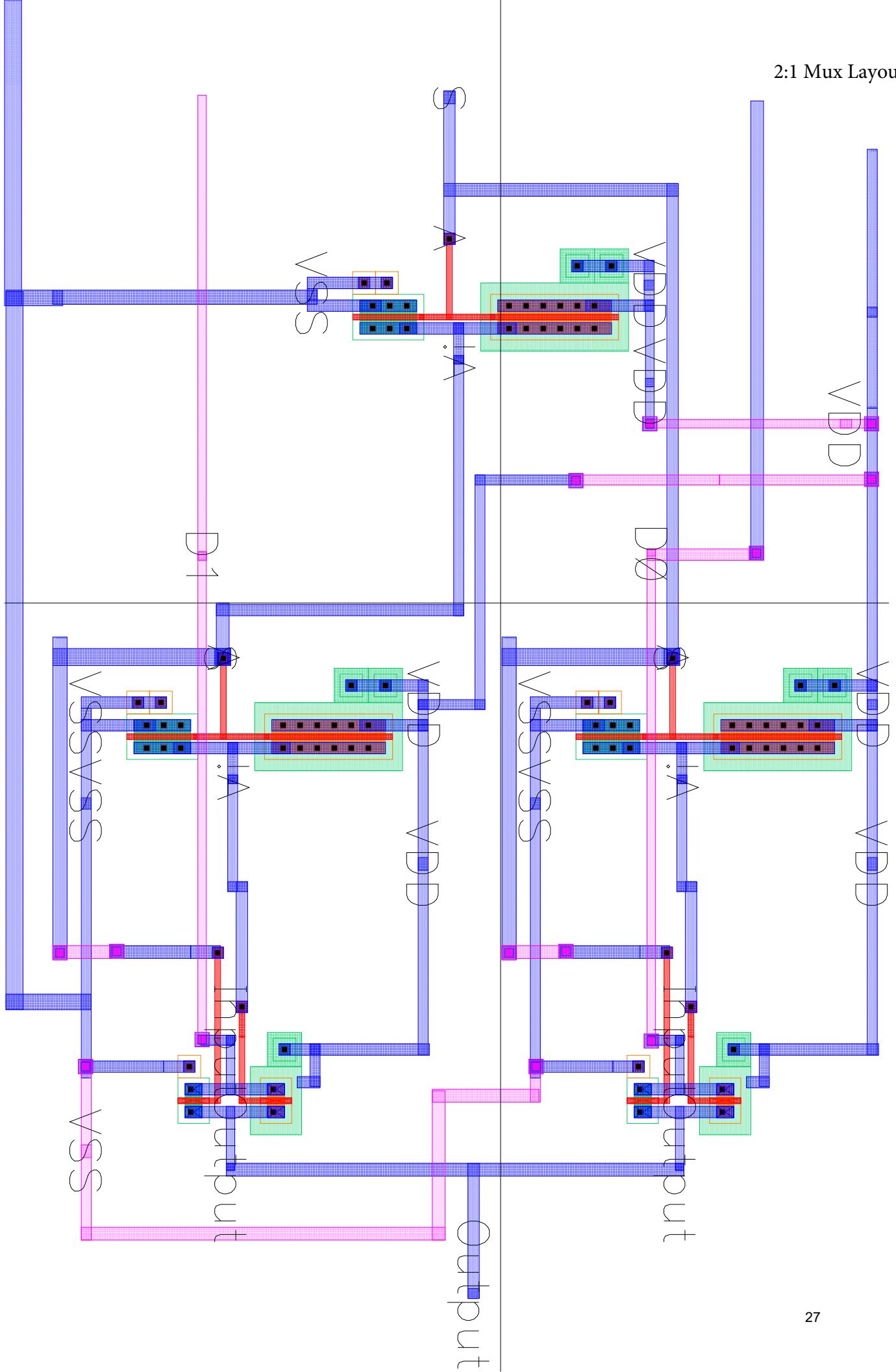
prunenet.out:

prunedev.out:

audit.out:

2:1 Mux Schematic





File Tools Options Help

cadence

```
completed ....Wed May  8 12:23:32 2019
```

```
CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
```

```
***** Summary of rule violations for cell "2_1MUX_layout layout" *****
```

```
Total errors found: 0
```

LVS FILE

```
@(#) $CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
```

Command line:

```
/software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir  
/gaia/class/student/kachareo/EEE234/LVS -l -s -t  
/gaia/class/student/kachareo/EEE234/LVS/layout  
/gaia/class/student/kachareo/EEE234/LVS/schematic  
Like matching is enabled.  
Net swapping is enabled.  
Using terminal names as correspondence points.
```

```
Net-list summary for  
/gaia/class/student/kachareo/EEE234/LVS/layout/netlist  
count  
9 nets  
6 terminals  
5 pmos  
5 nmos
```

```
Net-list summary for  
/gaia/class/student/kachareo/EEE234/LVS/schematic/netlist  
count  
9 nets  
6 terminals  
5 pmos  
5 nmos
```

```
Terminal correspondence points  
N7 N5 D0  
N6 N0 D1  
N4 N1 Output  
N5 N6 S  
N8 N2 VDD  
N3 N3 VSS
```

Devices in the netlist but not in the rules:

pmos nmos

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	10	10
total	10	10

	nets	
un-matched	0	0
merged	0	0
pruned	0	0

active	9	9
total	9	9
	terminals	
un-matched	0	0
matched but		
different type	0	0
total	6	6

Probe files from /gaia/class/student/kachareo/EEE234/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/kachareo/EEE234/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

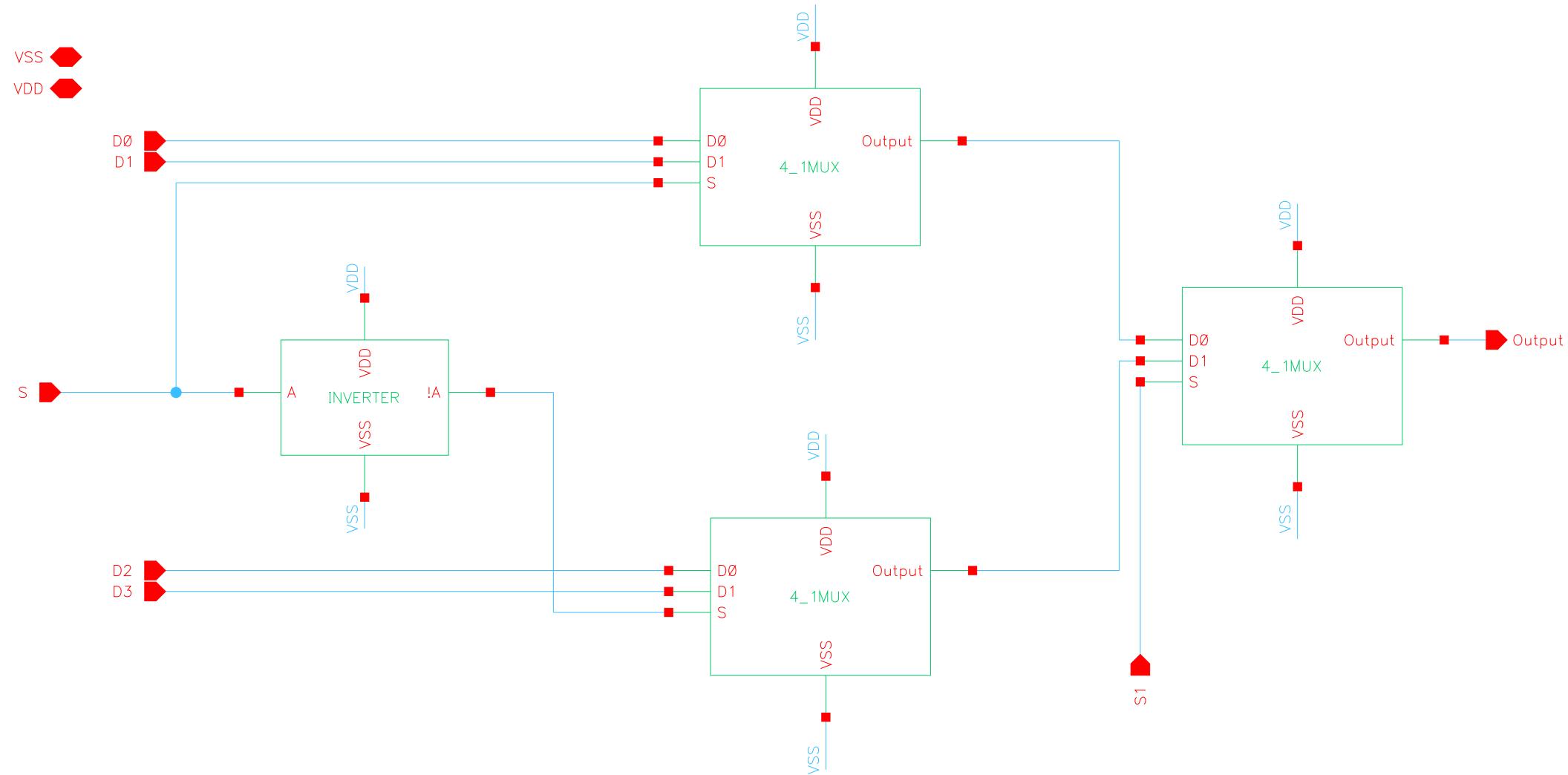
termbad.out:

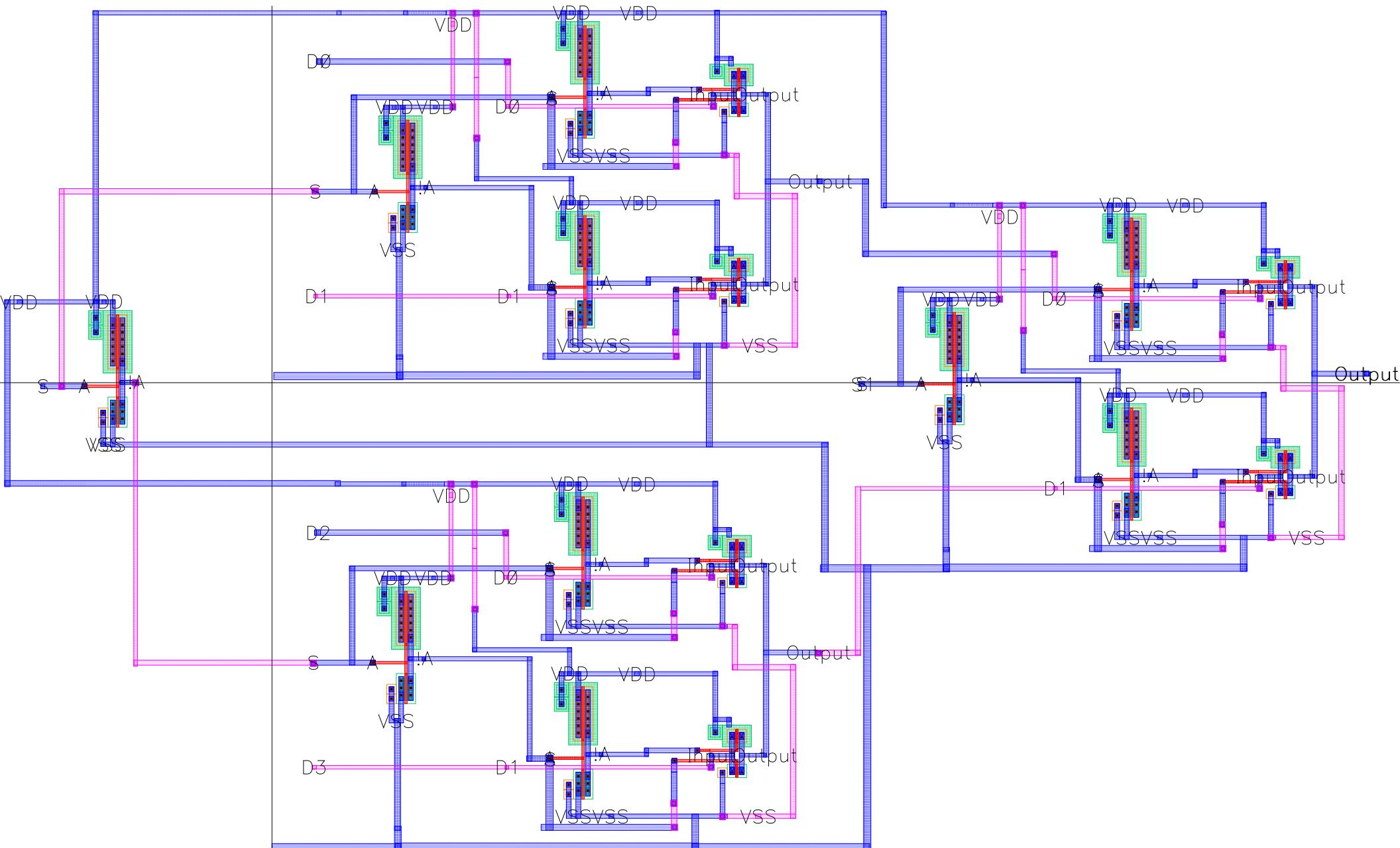
prunenet.out:

prunedev.out:

audit.out:

4:1 Mux Schematic





File Tools Options Help

cadence

completedWed May 8 12:25:26 2019

CPU TIME = 00:00:00 TOTAL TIME = 00:00:00

***** Summary of rule violations for cell "Real4_1_layout layout" *****

Total errors found: 0

mouse L:

M:

33

R:

LVS FILE

```
@(#) $CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
```

Command line:

```
/software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir  
/gaia/class/student/kachareo/EEE234/LVS -l -s -t  
/gaia/class/student/kachareo/EEE234/LVS/layout  
/gaia/class/student/kachareo/EEE234/LVS/schematic
```

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

```
Net-list summary for  
/gaia/class/student/kachareo/EEE234/LVS/layout/netlist  
count  
21 nets  
9 terminals  
16 pmos  
16 nmos
```

```
Net-list summary for  
/gaia/class/student/kachareo/EEE234/LVS/schematic/netlist  
count  
21 nets  
9 terminals  
16 pmos  
16 nmos
```

Terminal correspondence points		
N19	N9	D0
N18	N7	D1
N17	N1	D2
N16	N11	D3
N14	N8	Output
N15	N6	S
N12	N10	S1
N20	N4	VDD
N13	N5	VSS

Devices in the netlist but not in the rules:

```
pmos nmos
```

The net-lists match.

	layout	schematic
	instances	instances
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	32	32
total	32	32

nets

un-matched	0	0
merged	0	0
pruned	0	0
active	21	21
total	21	21

	terminals	
un-matched	0	0
matched but different type	0	0
total	9	9

Probe files from /gaia/class/student/kachareo/EEE234/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/kachareo/EEE234/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

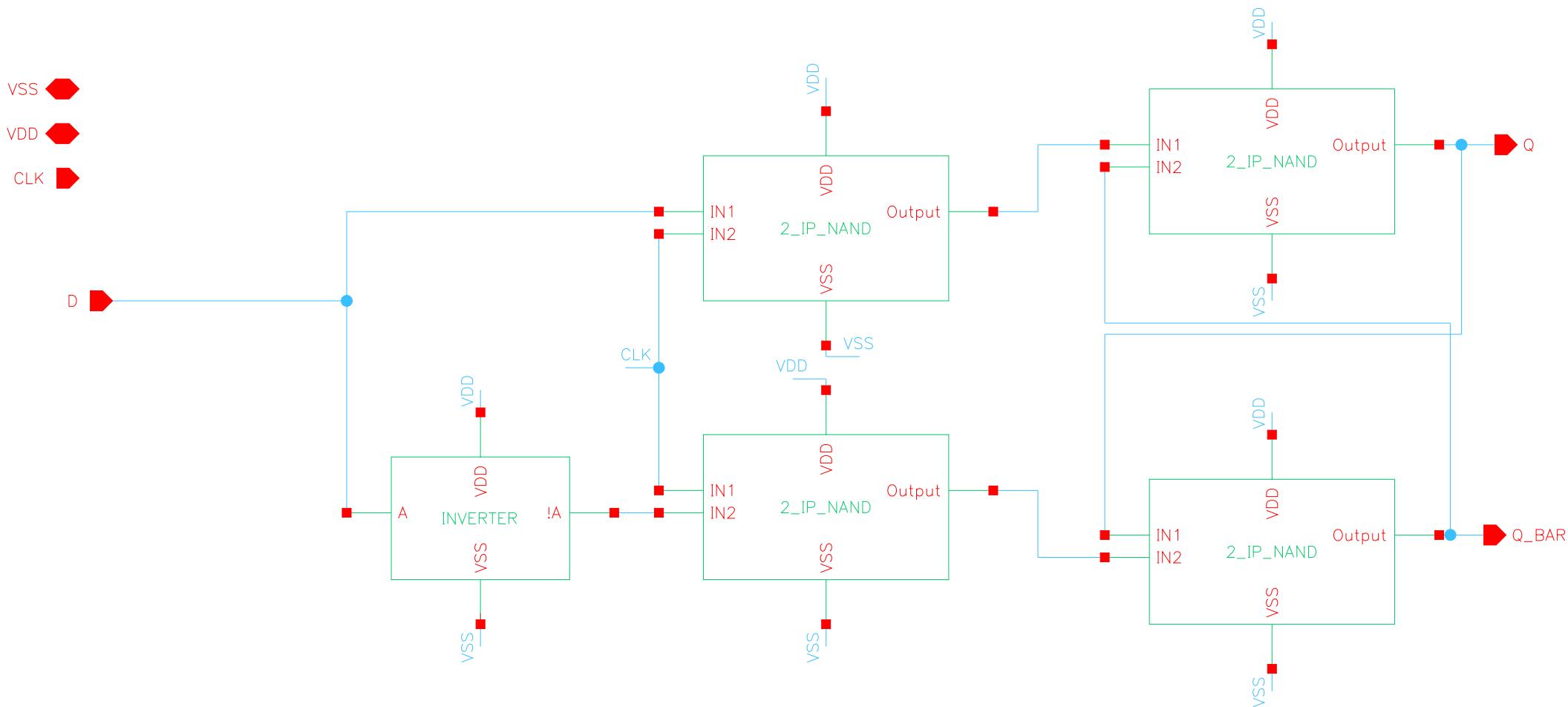
termbad.out:

prunenet.out:

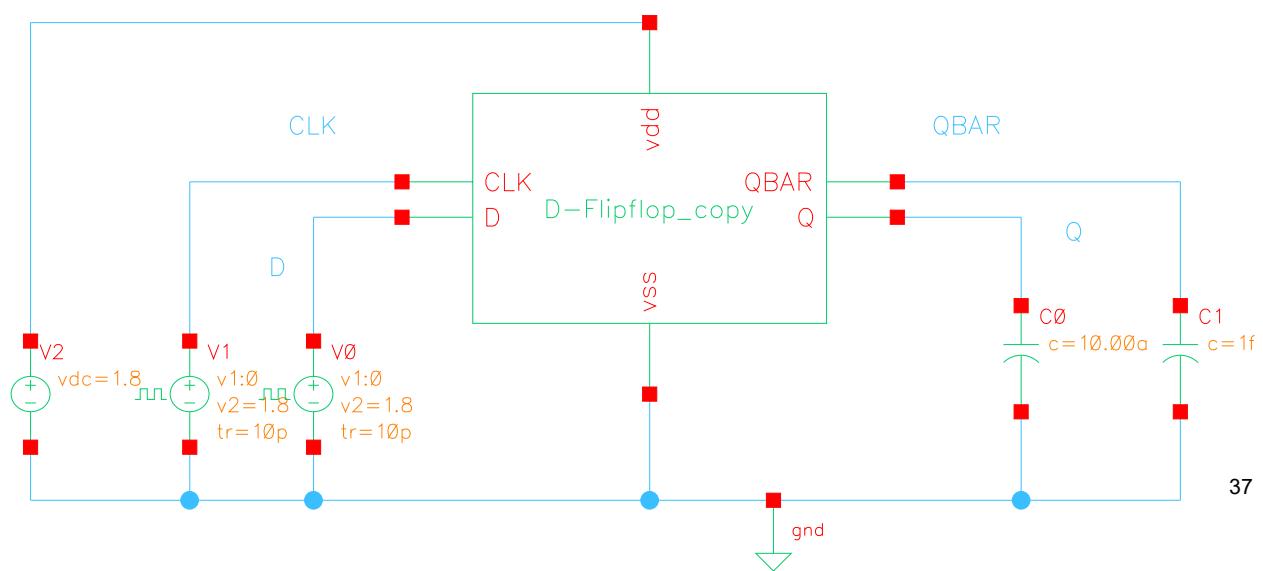
prunedev.out:

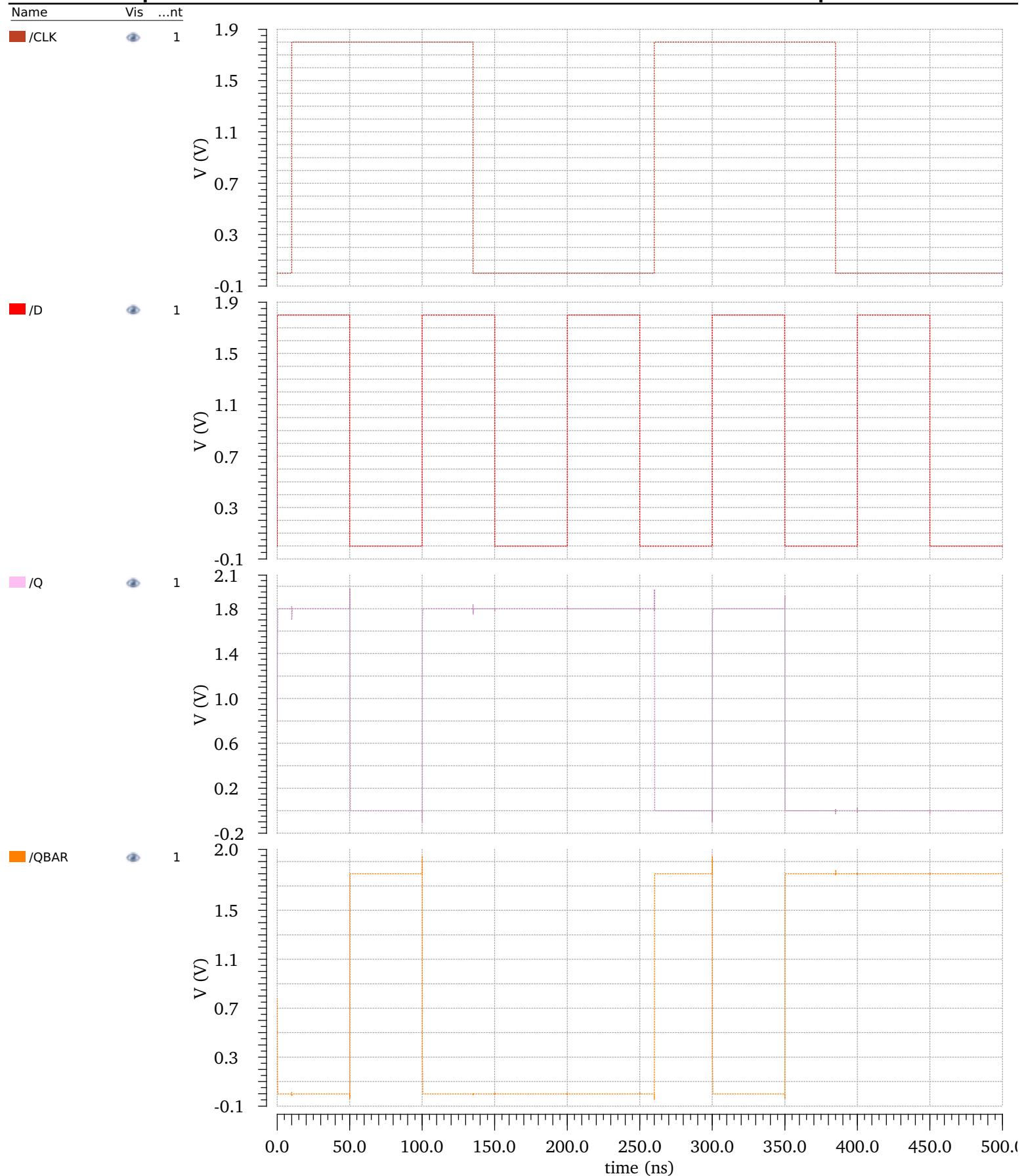
audit.out:

D Flip-Flop Schematic

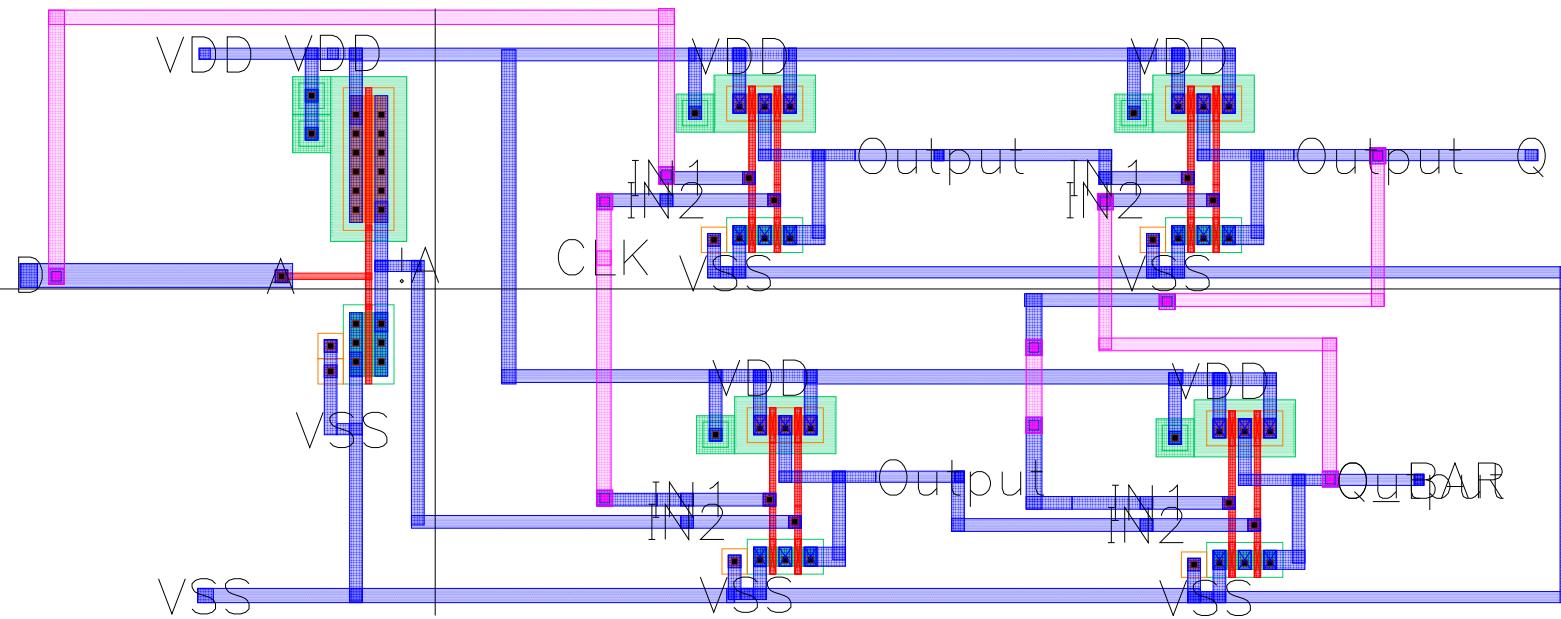


D Flip Flop Testbench



Transient Response**Fri Apr 19 18:44:29 2019**

D FFlip Flop Layout



File Tools Options Help

cadence

```
completed ....Wed May  8 12:28:41 2019
```

```
CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
```

```
***** Summary of rule violations for cell "D_FF_Layout layout" *****
```

```
Total errors found: 0
```

LVS File

```
@(#) $CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
```

Command line:

```
/software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir  
/gaia/class/student/kachareo/EEE234/LVS -l -s -t  
/gaia/class/student/kachareo/EEE234/LVS/layout  
/gaia/class/student/kachareo/EEE234/LVS/schematic
```

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

```
Net-list summary for  
/gaia/class/student/kachareo/EEE234/LVS/layout/netlist
```

count	
13	nets
6	terminals
9	pmos
9	nmos

```
Net-list summary for  
/gaia/class/student/kachareo/EEE234/LVS/schematic/netlist
```

count	
13	nets
6	terminals
9	pmos
9	nmos

Terminal correspondence points

N10	N7	CLK
N11	N6	D
N9	N5	Q
N8	N4	Q_BAR
N12	N1	VDD
N7	N0	VSS

Devices in the netlist but not in the rules:

pmos nmox

1 net-list ambiguity was resolved by random selection.

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	7	0
size errors	0	0
pruned	0	0
active	18	18
total	18	18

	nets	
un-matched	0	0

merged	0	0
pruned	0	0
active	13	13
total	13	13
		terminals
un-matched	0	0
matched but		
different type	0	0
total	6	6

Probe files from /gaia/class/student/kachareo/EEE234/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/kachareo/EEE234/LVS/layout

devbad.out:

netbad.out:

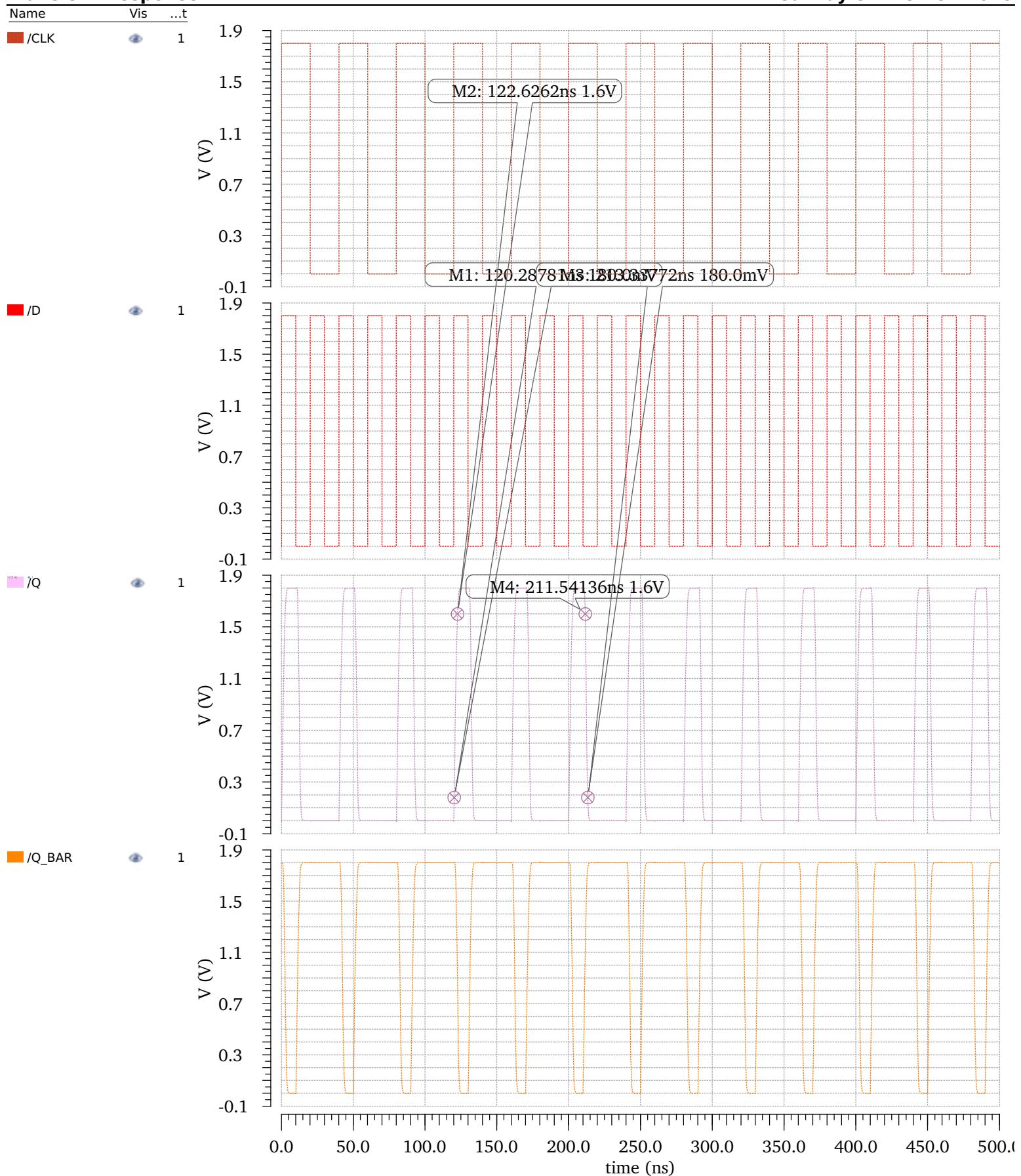
mergenet.out:

termbad.out:

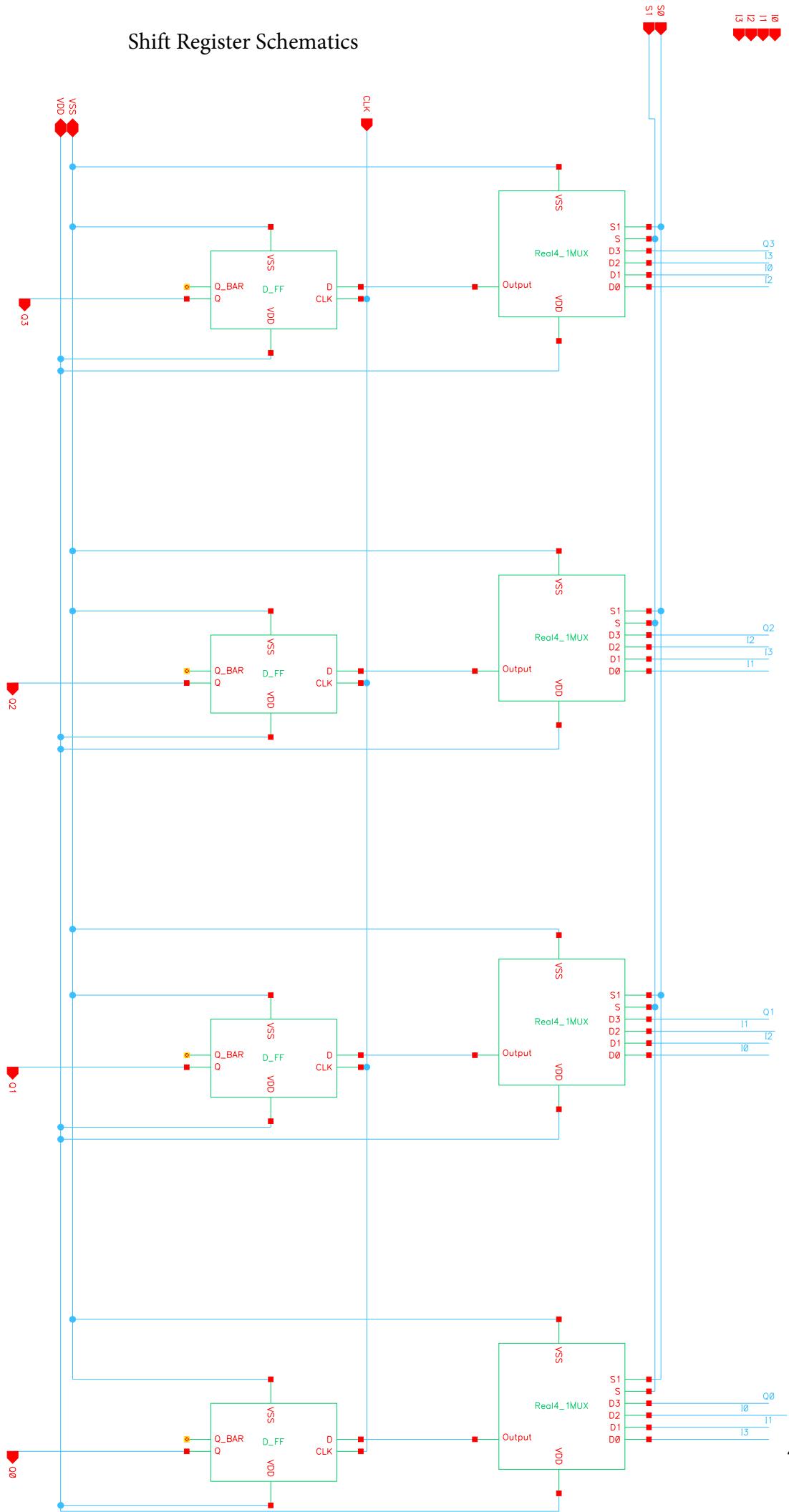
prunenet.out:

prunedev.out:

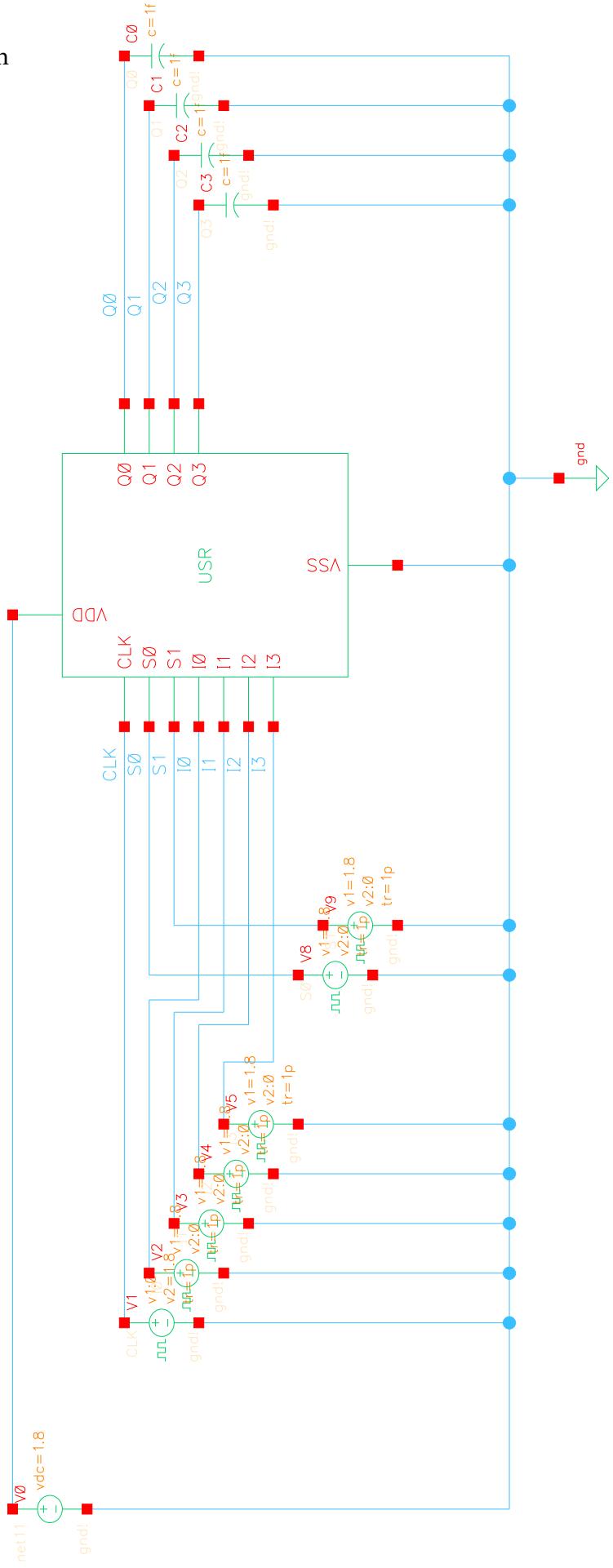
audit.out:

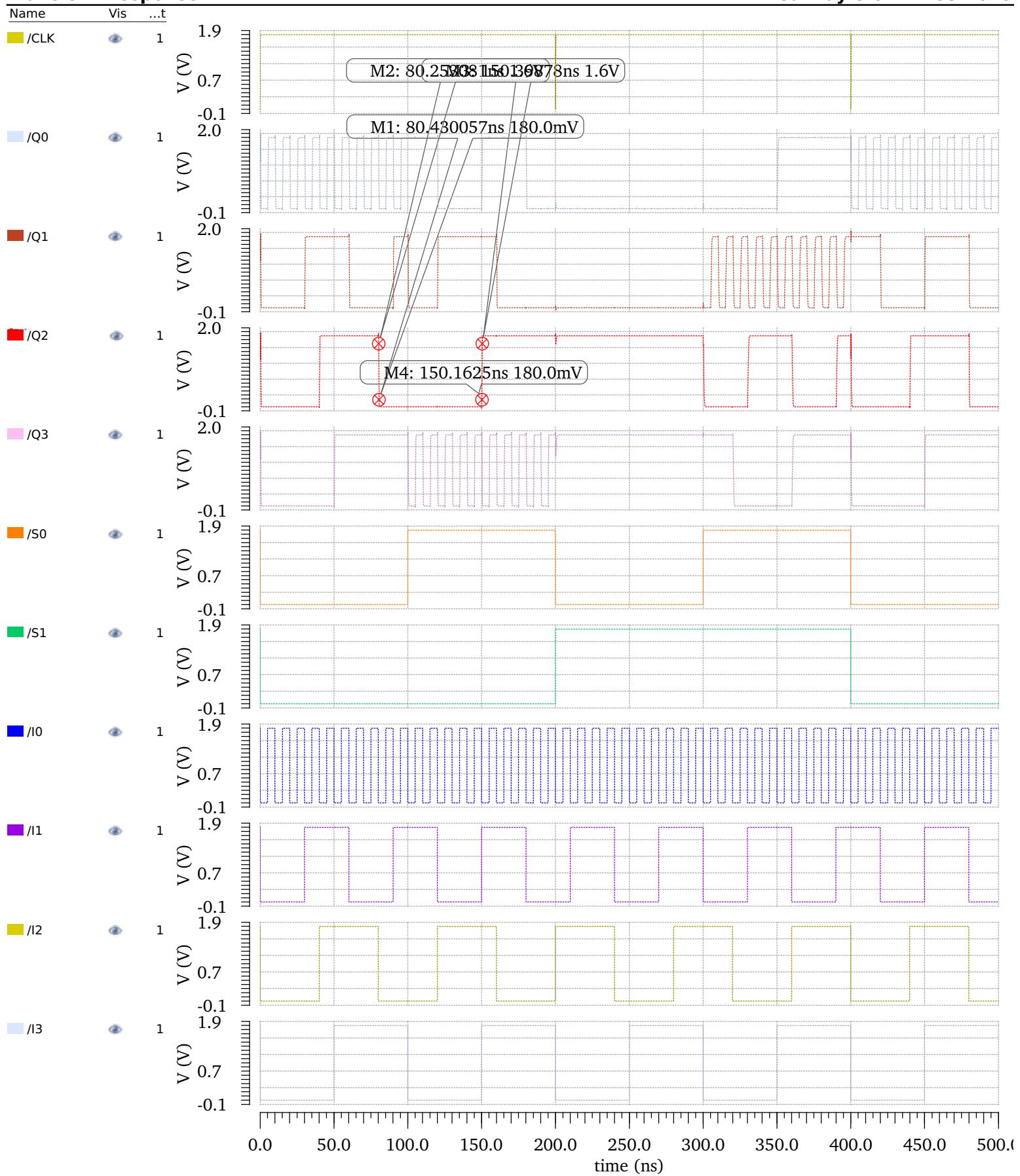
Transient Response**Wed May 8 21:52:57 2019**

Shift Register Schematics

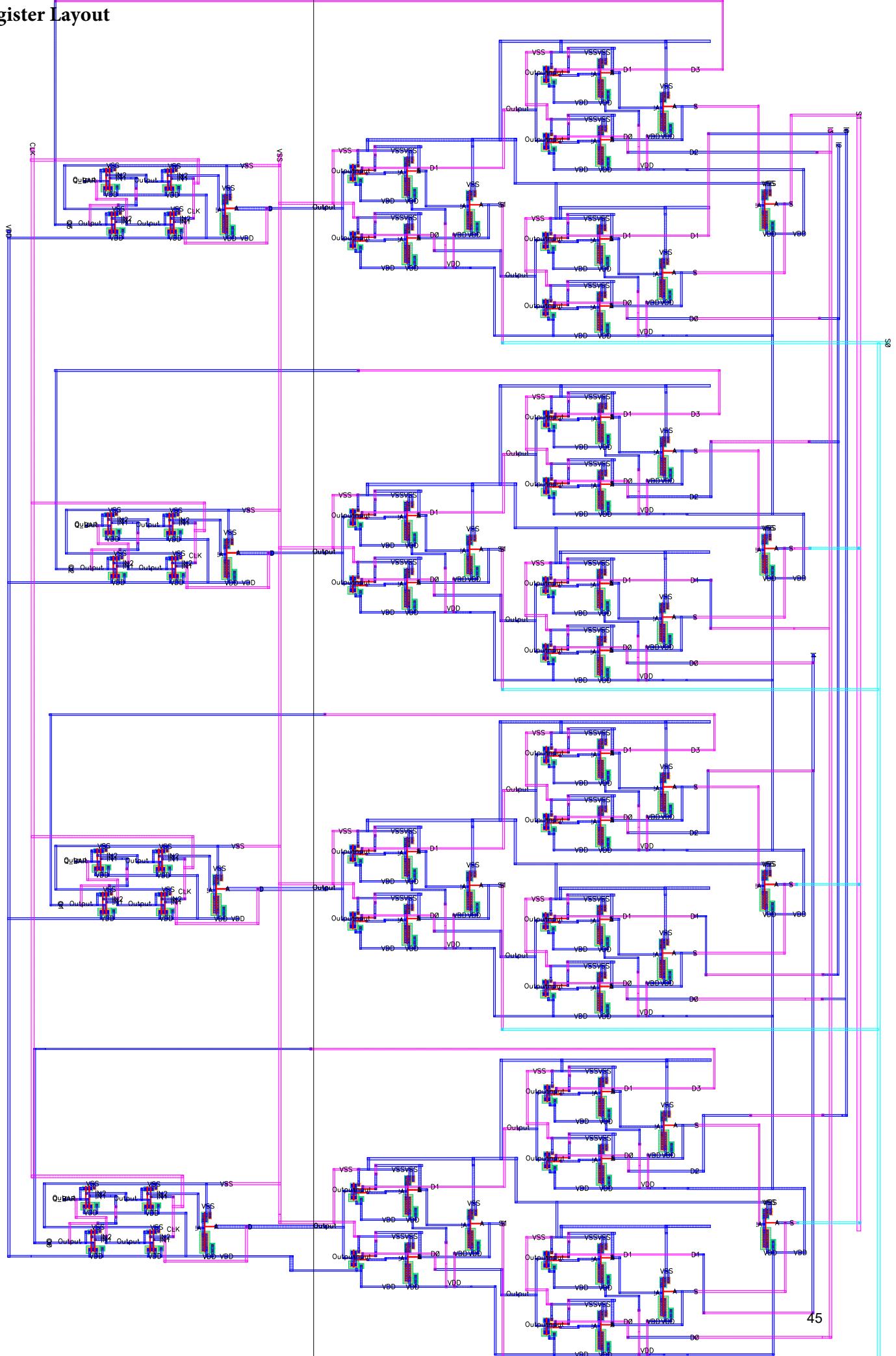


Shift Register Testbench



Transient Response**USR Simulation Waveforms****Wed May 8 02:21:53 2019**

Shift Register Layout



File Tools Options Help

Extraction started at Tue May 7 14:27:06 2019

Validating hierarchy instantiation for:

library: OK_project1

cell: USR_layout2

view: layout

Rules come from library NCSU_TechLib_tsmc02d.

Rules path is divaEXT.rul.

Inclusion limit is set to 1000.

Running layout Extraction analysis

flat mode

Full checking.

For layer nChannelTran :

100 shapes encountered.

100 nmos4 ivpcell NCSU_Analog_Parts devices well formed.

For layer pChannelTran :

100 shapes encountered.

100 pmos4 ivpcell NCSU_Analog_Parts devices well formed.

0 cap ivpcell NCSU_Analog_Parts parasitics created.

Extraction started.....Tue May 7 14:27:06 2019

completedTue May 7 14:27:06 2019

CPU TIME = 00:00:00 TOTAL TIME = 00:00:00

***** Summary of rule violations for cell "USR_layout2 layout" *****

Total errors found: 0

LVS File

```
@(#) $CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $
```

Command line:

```
/software/cadence/install/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir  
/gaia/class/student/kachareo/EEE234/LVS -l -s -t  
/gaia/class/student/kachareo/EEE234/LVS/layout  
/gaia/class/student/kachareo/EEE234/LVS/schematic
```

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Compiling Diva LVS rules...

```
Net-list summary for  
/gaia/class/student/kachareo/EEE234/LVS/layout/netlist  
count  
97 nets  
13 terminals  
100 pmos  
100 nmos
```

```
Net-list summary for  
/gaia/class/student/kachareo/EEE234/LVS/schematic/netlist  
count  
97 nets  
13 terminals  
100 pmos  
100 nmos
```

Terminal correspondence points

N95	N6	CLK
N90	N20	I0
N89	N13	I1
N88	N1	I2
N87	N14	I3
N94	N16	Q0
N93	N15	Q1
N92	N3	Q2
N91	N11	Q3
N85	N12	S0
N84	N5	S1
N96	N4	VDD
N86	N19	VSS

Devices in the rules but not in the netlist:

```
cap nfet pfet nmos4 pmos4
```

The net-lists match.

	layout	schematic
	instances	instances
un-matched	0	0
rewired	0	0
size errors	0	0

pruned	0	0
active	200	200
total	200	200
nets		
un-matched	0	0
merged	0	0
pruned	0	0
active	97	97
total	97	97
terminals		
un-matched	0	0
matched but different type	0	0
total	13	13

Probe files from /gaia/class/student/kachareo/EEE234/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/kachareo/EEE234/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

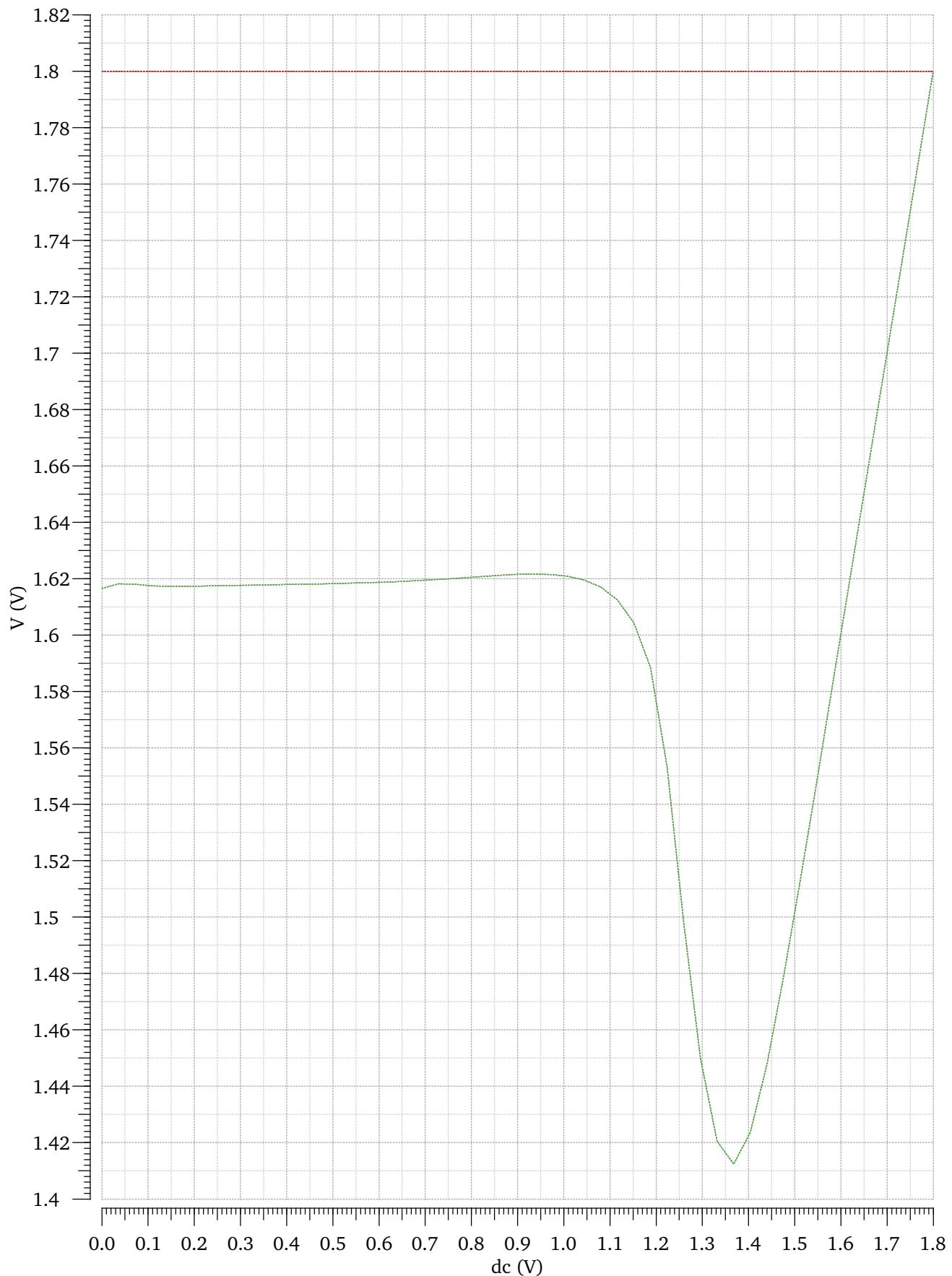
audit.out:

DC Response

Name	Vis
/CLK	●
/Q0	●
/Q1	●
/Q2	●
/Q3	●
/S0	●
/S1	●
/I0	●
/I1	●
/I2	●
/I3	●

DC Analysis

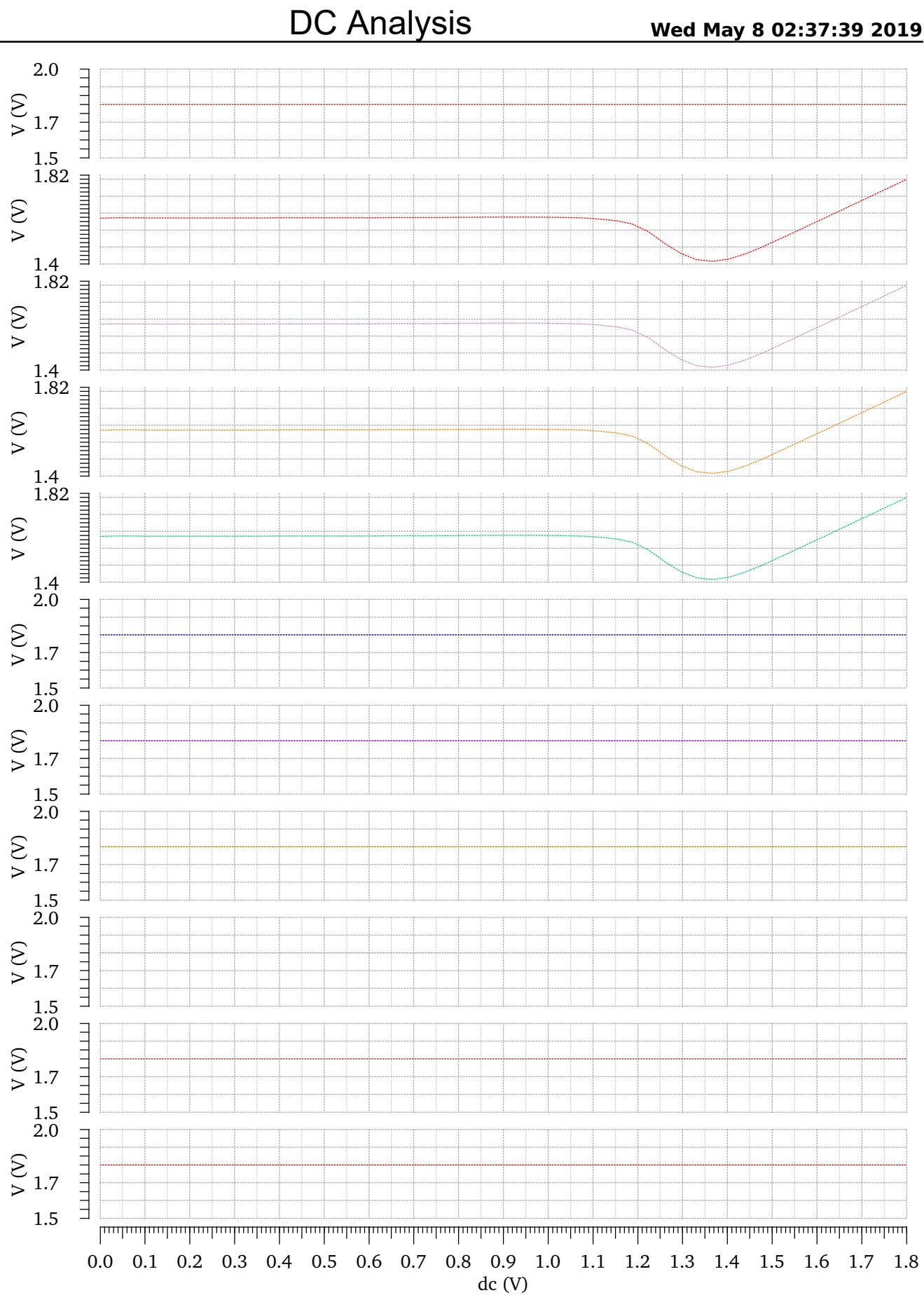
Wed May 8 02:37:39 2019

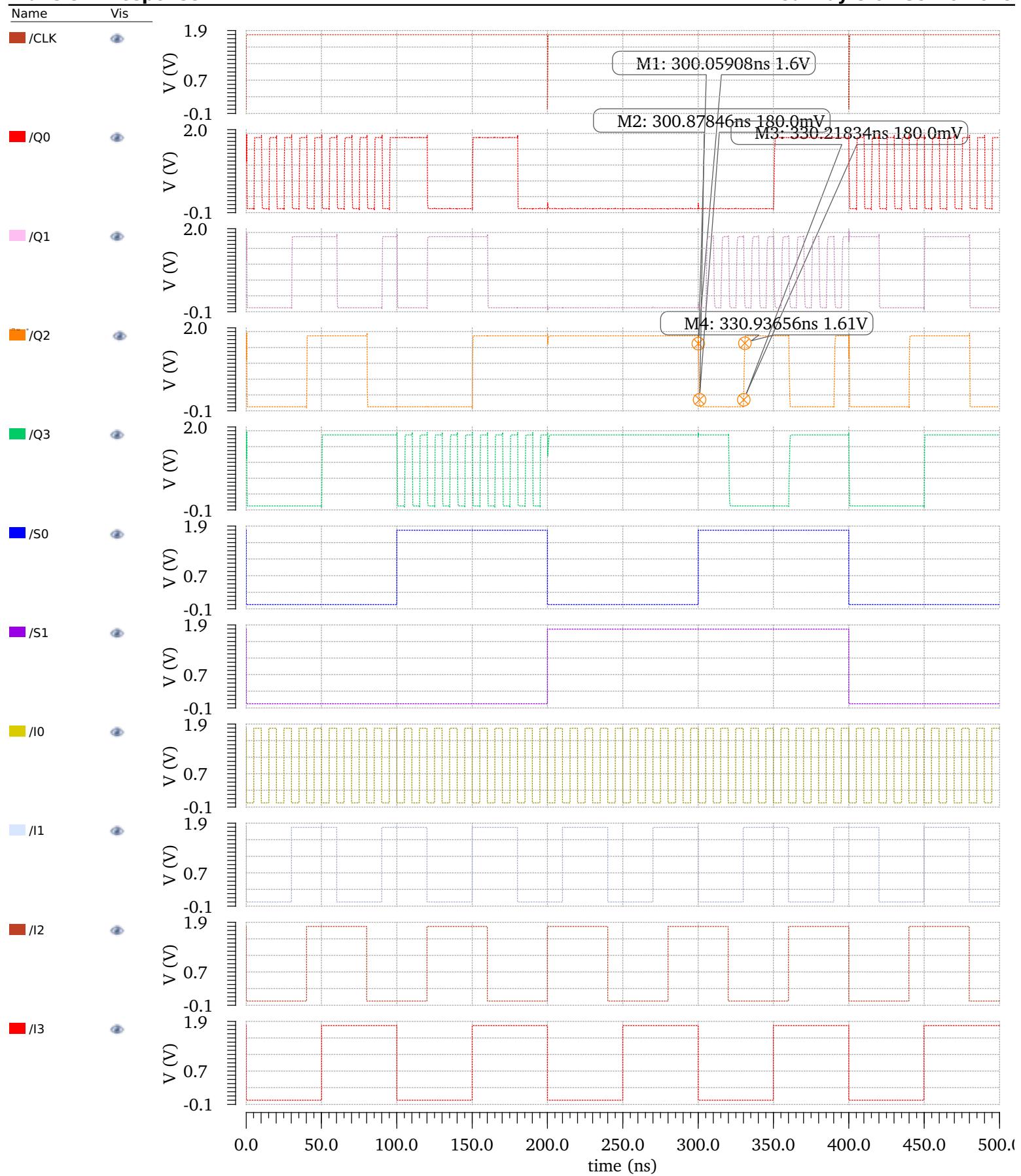


DC Response

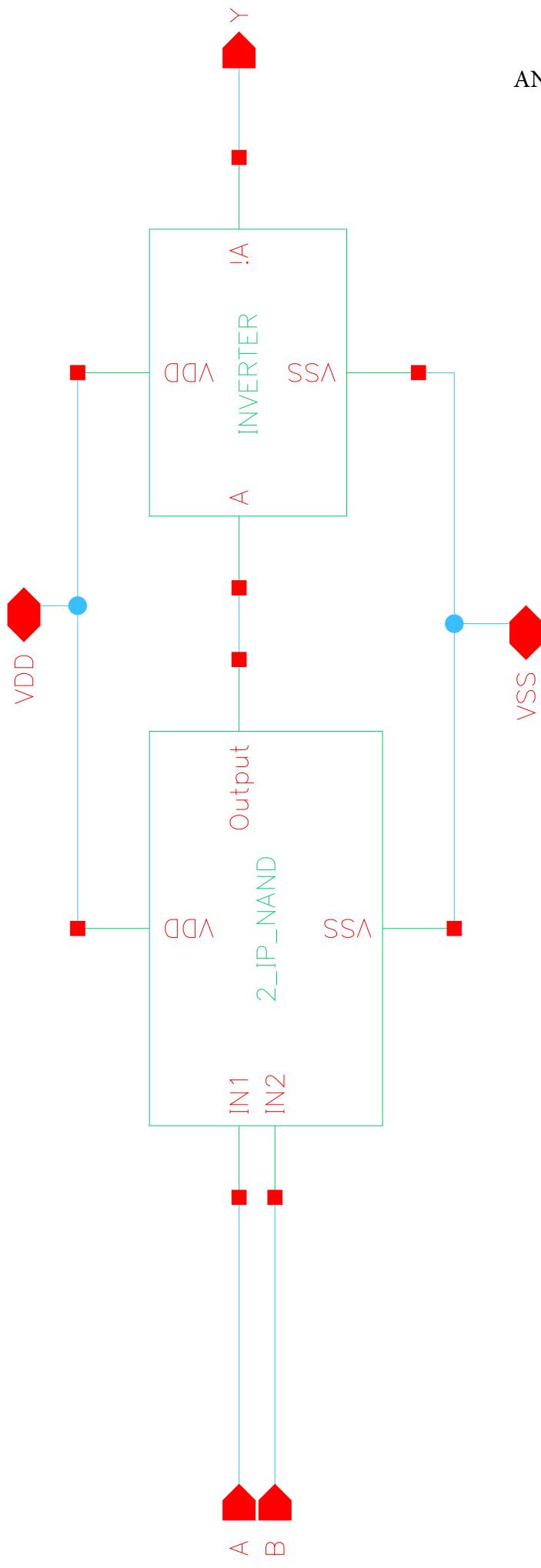
Name Vis

■ /CLK

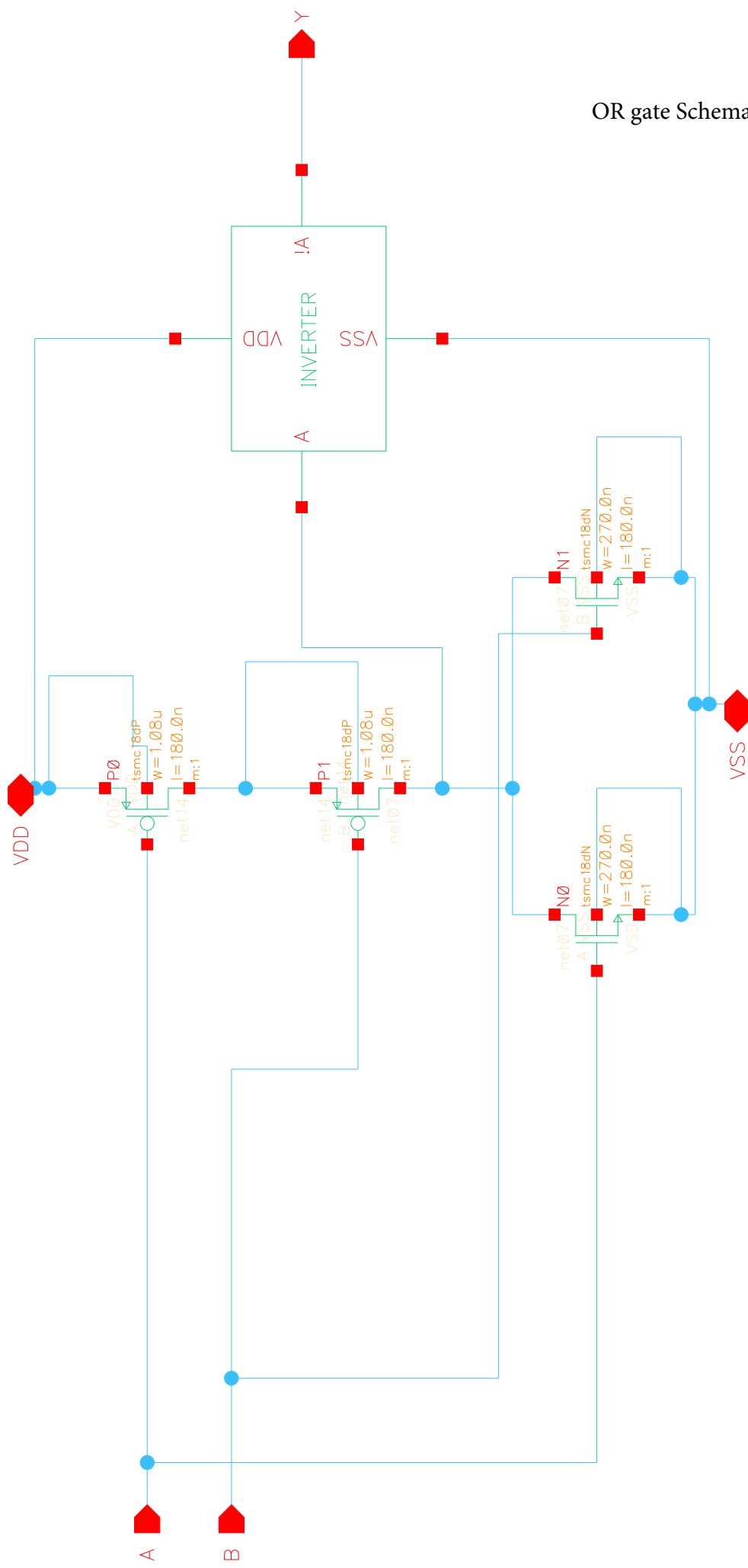


Transient Response**Post Sim Waveforms****Wed May 8 02:39:46 2019**

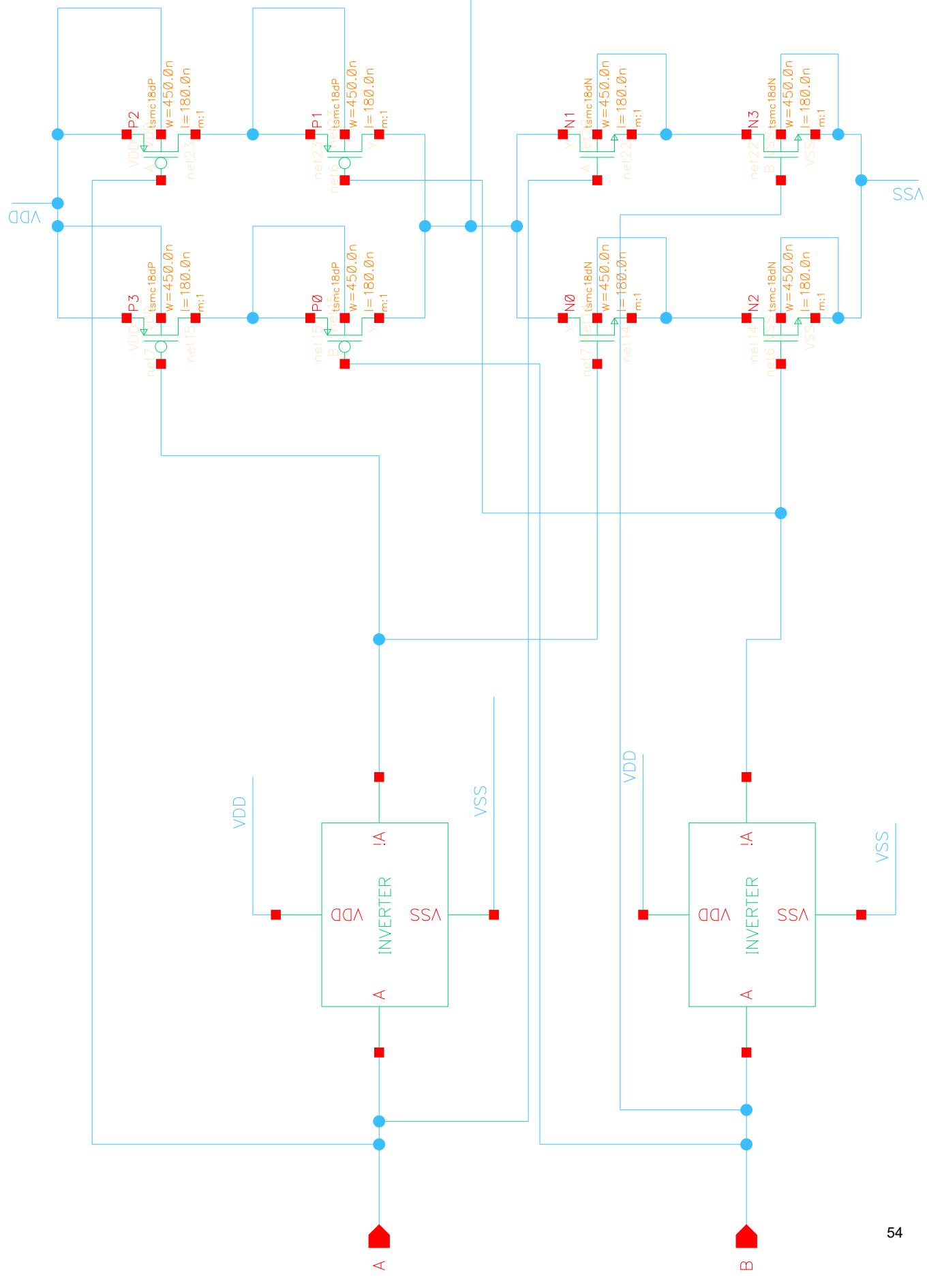
AND Gate Schematic



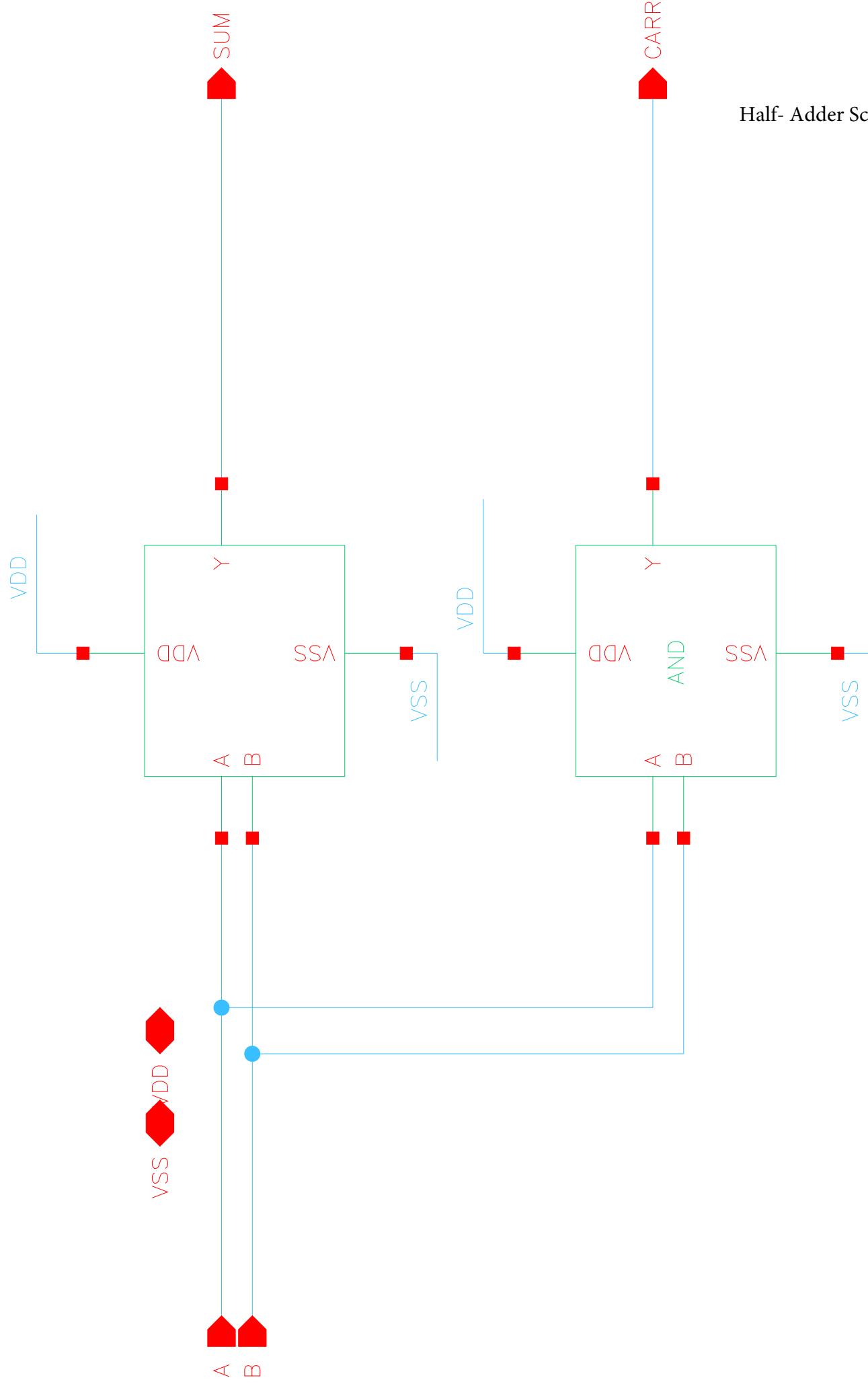
OR gate Schematic



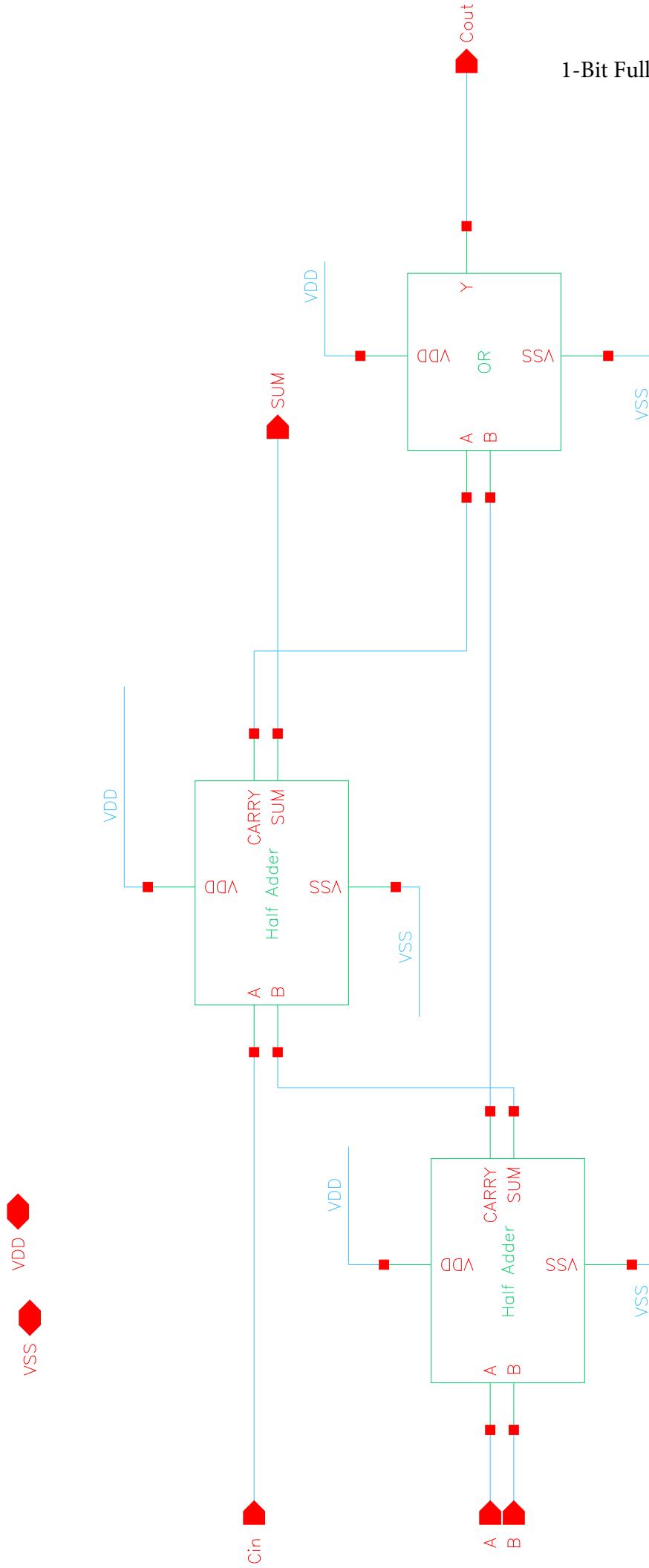
XOR gate Schematic



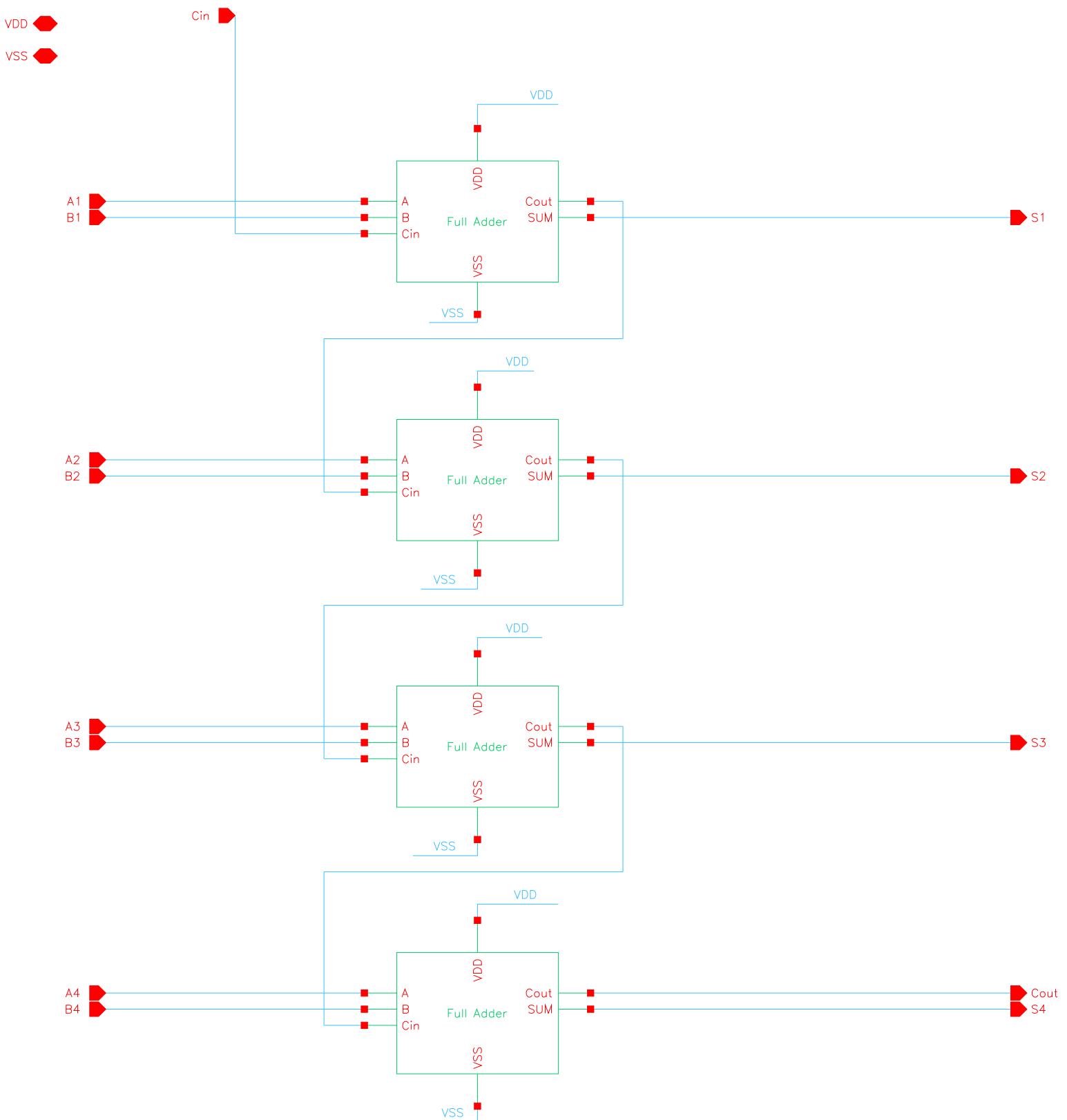
Half- Adder Schematic



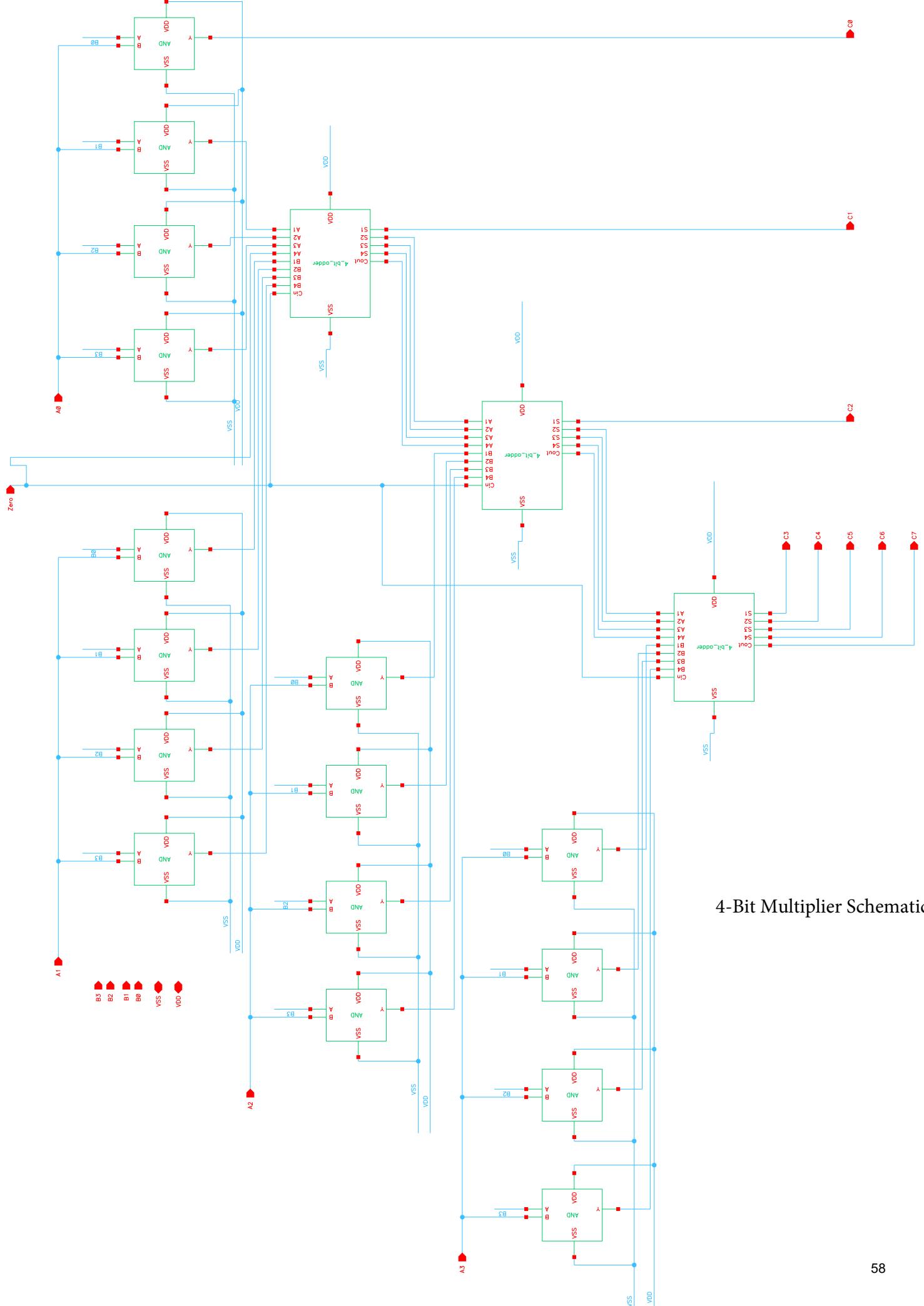
1-Bit Full Adder

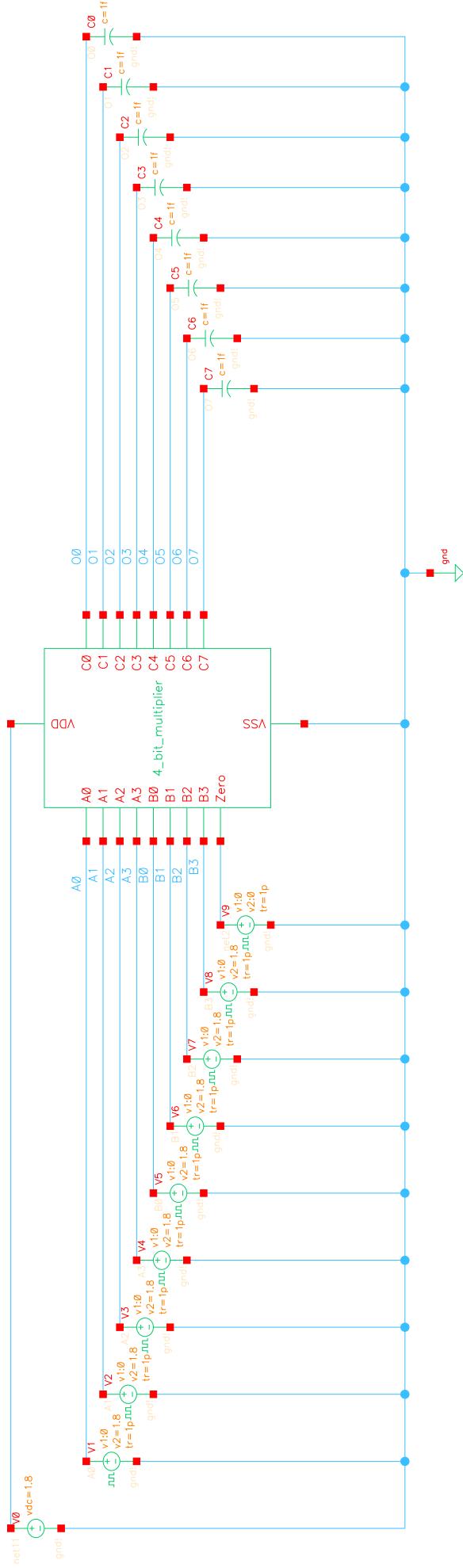


4-Bit Full Adder

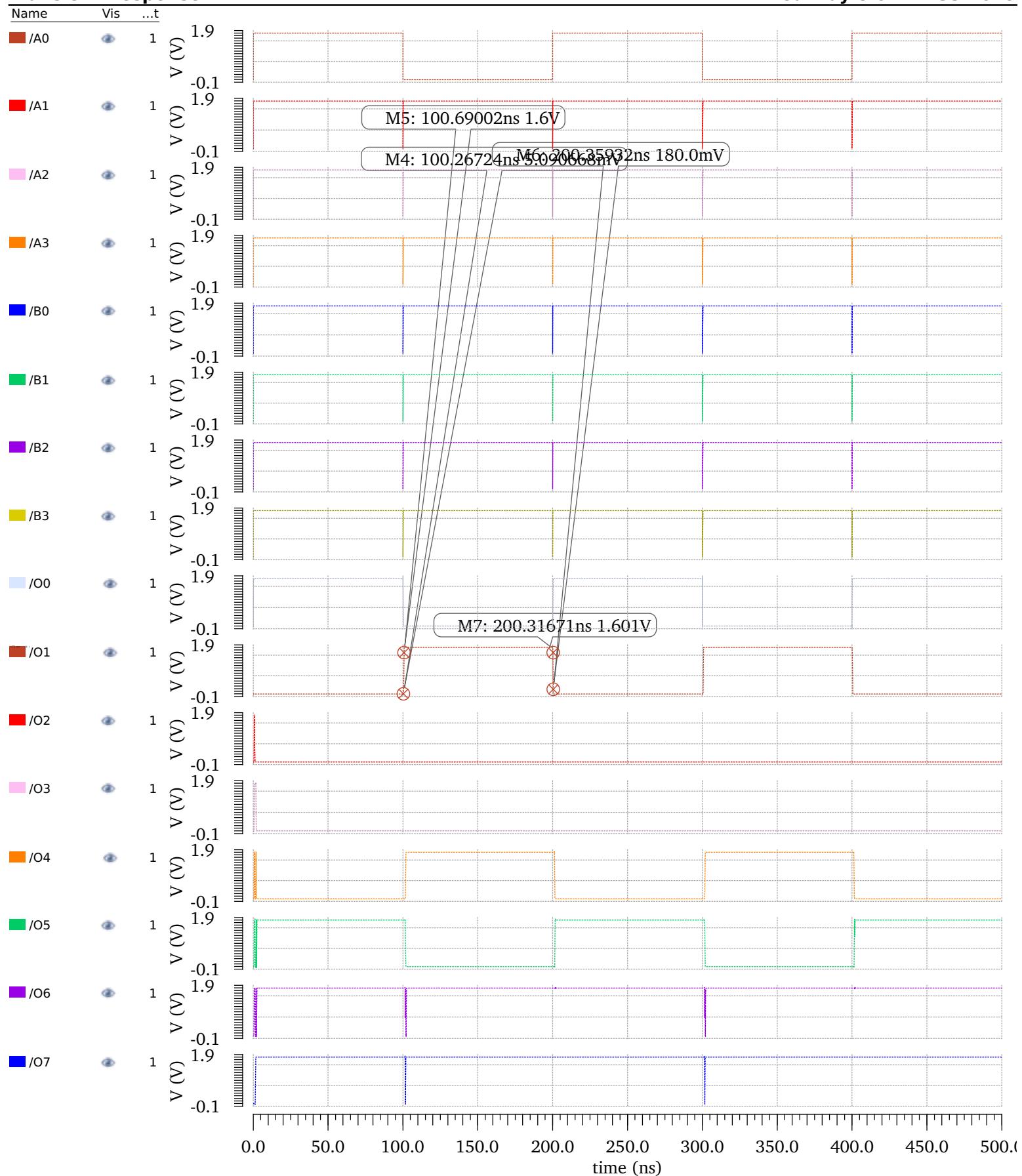


4-Bit Multiplier Schematic





4-Bit Multiplier Fixture

Transient Response**Sim waveforms****Wed May 8 02:11:33 2019**

4 Bit Multiplier Layout

