ELEC 4511/5511

Lab 9

Lab 9 Linear Regression Hardware-Software Co-design

In this lab, you will use Verilog to design an AXI-Stream wrapper for your vectorized gradient calculation module (lab8), and verify the new linear regression algorithm on the PYNQ board.

1. Experiment goal:

- Be further familiar with hardware-software co-design using Verilog and Xilinx Vivado IDE
- Understand the AXI-stream Protocol.
- Be further familiar with using linear regression algorithm.
- Understand the importance of timing.

2. Specific tasks:

1. Design an AXI-stream wrapper for your "gradient_calc" module. You can use the previous labs as reference.
2. Verify your design on the PYNQ board using the provided jupyter notebook file "**linear_regression_student**" and the csv file "**Advertising.csv**"

Please find the more detailed information in Lecture 25.

Canvas submission: Please submit your report in "**.pdf**" file format and compress your Verilog code into a "**.zip**" file.

What needs to be included in your report:

1. Copy the Verilog code of your AXI-stream wrapper in the report
2. Screenshot of the result shown in the jupyternote book
3. Please write a short analysis of each problem, mainly explaining how you think about the design of the function, what troubles you encountered during the design process, and how you finally solved them, etc.

What needs to be included in your "**.zip**" file:

Verilog code, jupternote book file.