ELEC 4511/5511

Lab 7

Customize a Sobel-X filter with AXI-Stream Interface

In this lab, you will design a "Sobel-X filter" accelerator with AXI-Stream interface using Verilog, and verify your design on the PYNQ board.

1. Experiment goal:

- Be further familiar with the process of using Vivado IDE to customize hardware IP with AXI-Stream interface.
- Master the method of using Verilog to process the two-dimensional image data stream.
- Understand how to use testbench to simulate image processing algorithms.
- Understand the method of handling two-dimensional array data on the PYNQ board system

2. Specific Steps:

1) Design a **Sobel-X** filter in **Verilog**. The Soble-X kernel is:

-1	0	1
-2	0	2
-1	0	1

Please use **Lecture 22** as reference. And you can find more detailed information in the **Video Lecture 22**. The testbench file is provided for you (**SobleX_tb.v**). The grayscale input image is named "**input.bmp**". The image size is **555x695** (image_width = **695**), which could be considered as the known information.

2) Add an AXI-stream wrapper onto your Sobel-X filter, and connect it with AXI_DMA. You can find more detailed information in the **Video Lecture 23**. Besides, for the steps of creating a ZYNQ system project, adding custom IP to the system, connecting your IP with the AXI_DMA module, exporting bitstream and block design files and other steps, please refer to **previous lectures and Lab 6**. Finally upload the bitstream and block design files to the PYNQ board and test your design.

The grayscale input image for this step is named "**1.tif**". The image size is still **555x695** (image_width = **695**), which could be considered as the known information. And the jupyter notebook file for testing your design is provided for you. (**SobelX.ipynb**)

Canvas submission: Please submit your report in ".**pdf**" file format and compress your Vivado project and your Jupyter notebook file into a "**.zip**" file.

What needs to be included in your report:

1. Copy your Verilog code of Sobel-X filter and AXI-stream wrapper (e.g. stream_v1_0.v) in the report
2. Screenshot of your Sobel-X filter simulation result
3. Screenshot of your verification result in Jupyter Notebook
4. Please write a short analysis of each problem, mainly explaining how you think about the design of the function, what troubles you encountered during the design process, and how you finally solved them, etc.

What needs to be included in your "**.zip**" file:

The folders of your vivado project and IP_repo.