# Bala Dhinesh Muthiah

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## Education

**Indian Institute of Technology Madras** — **Chennai, India**
*B.Tech in Electrical Engineering, Minor in Computing; CGPA 8.66/10* — Aug 19 - Present

## Achievements

- University Demo Best Demonstration, Honorable Mention, SIGDA Design Automation Conference 2021.
- $1500 stipend from Google for open-source contribution to FOSSi Foundation through Google Summer of Code, 2021.
- Semi-finalist, Terasic InnovateFPGA design contest 2021 sponsored by Intel.
- Ranked 2196 (among 170,000 applicants) in Joint Entrance Examination (JEE) Advanced Examination 2019.
- Ranked top 0.4% (among 1 million applicants) in Joint Entrance Examination (JEE) Mains Examination 2019.

## Publications

- **Bala Dhinesh**, Nan Wu, Hanran Wu, Yuan Xie and Cong "Callie" Hao, *"**When Approximate Computing Meets Graph Neural Networks**"*, Manuscript under review at Design Automation Conference (DAC) 2023.

## Research Projects

**Binary Neural Network (BNN) Inference on FPGA** — IIT Madras
*Bachelor's Thesis | Guide: Prof. Nitin Chandrachoodan | Collab with KLA Advanced Computing Labs* — Nov 2022 - Present
- Exploring various architectures and algorithms to alleviate the memory bottleneck problem for the UNet Segmentation model.

**Approximate Computing on Graph Neural Networks (GNNs)** — Remote
*Research Internship, Georgia Institute of Technology | Guide: Prof.Cong "Callie" Hao* — Feb 2022 - Present
- Replaced the traditional FP32 multipliers in the Graph Convolutional layers with various INT8, INT16 approximate multipliers.
- Reduced the power by **40%** and energy by **26%** in matrix multiplication | Performance closely similar to FP32 (**70x** gain).
- Employed **Degree Quant**, a Quantization Aware Training that selectively reduces the precision of multipliers of GNN nodes.
- Examined the effects of approximation component errors | Performed design exploration to determine the **Pareto curve** between power and GNN accuracy.

**Rapid Hardware Prototyping Framework for FPGAs** | Details — IIT Madras
*Research Project | Guide: Prof. Nitin Chandrachoodan* — Jan 2022 - July 2022
- Developed a framework that provides a **ready-to-use harness** for testing user designs on Xilinx ZYNQ FPGAs.
- Interfaced user designs with **AXI Lite and Stream protocols** | Dynamically determines the maximum operatable frequency.
- Exposed the PYNQ Jupyter Notebook server to the internet, allowing anyone to access the FPGA remotely.
- Employed Partial Reconfiguration, which considerably reduced area overhead and bitstream load time.
- This setup was used for assignments by more than 130 students enrolled in the Computer Organization (EE2003) course.

**Virtual FPGA Lab** | Details — Remote
*Student Developer, Google Summer of Code 2021 | Mentor: Mr.Steve Hoover* — May 2021 - Aug 2021
- Developed an online simulator to **visualize FPGA** and their peripheral outputs using the VIZ Visualization feature in the Makerchip platform, thereby mimicking the physical lab experience.
- Visualization is implemented in JavaScript | Supports both Transaction-Level Verilog (TL-Verilog) and SystemVerilog.
- Automated the entire **Xilinx Vivado flow** to run the design in an actual FPGA.

## Technical Professional Experience

**Qualcomm India Pvt. Ltd.** — Bengaluru, India
*Hardware Engineering Internship | Mentor: Mr. Sreekumar* — May 2022 - Aug 2022
- Automated the development of interrupt-related System Verilog modules for the latest processor.
- Eliminates manually writing of **more than 10K** lines of code | Script is robust and scalable to any microprocessor.
- Tested the automated Verilog modules after compilation and synthesis to check for functional correctness.

## Relevant Projects

**Custom Data Prefetcher Algorithm** | Details — IIT Madras
*Course Project | Computer Architecture | Guide: Prof. Madhu Mutyam* — Oct 2022 - Nov 2022
- Replaced Next-Line prefetcher in the IPCP prefetcher with Next or Previous Line prefetcher and simulated using **ChampSim**.
- Achieved **0.73%** improvement in **IPC**, up to **5%** decrease in **MPKC** and **60%** increase in favoring the **custom prefetcher class** over IPCP prefetcher on the SPEC benchmarks.

**RISC-V Bit Manipulation Extension Support** | Details — IIT Madras
*Course Project | CAD for VLSI | Guide: Prof. Kamakoti* — Nov 2022
- Implemented **RISC-V Bit Manipulation extension** for RV32 and RV64 in Bluespec SystemVerilog.
- Simulated the design using **Verilator** and **cocotb** is used for writing test benches and verification.

**Hardware efficient Bitonic Sorting in Verilog** | Details — Remote
*Personal Project* — Apr 2022
– Implemented a high-performance Bitonic Parallel sorting algorithm with a reconfigurable number of elements and bitwidth.

**Hardware Accelerator for Mandelbrot Fractal Generation** | Details — IIT Madras
*Course Project | Mapping DSP Algorithms to Architectures | Guide: Prof. Nitin Chandrachoodan* — Mar 2022 - Apr 2022
– Accelerated Mandelbrot Fractal Generation in FPGA by designing **AXI Stream IP design** in **Vitis HLS**.
– Utilized **Xilinx PYNQ framework** to interact between the PS and PL of the PYNQ-Z2 FPGA.

**Hardware Accelerator for Advanced Encryption Standard(AES) Algorithm** | Details — IIT Madras
*Course Project | Computer Organisation | Guide: Prof. Nitin Chandrachoodan* — Nov 2021 - Dec 2021
– Accelerated Standard and two security-enhanced modified 128bit AES encryption by designing custom **AXI-Lite IPs** in **Vivado**.
– Interfaced the design with **Microblaze** soft processor and achieved a **35x speedup** in Artix-7 FPGA board over 2.9GHz PC.
– Achieved **16%** gain in security performance (**Avalanche effect**) of the Modified AES versions over the Standard AES.

**8-bit signed Carry Save Multiplier(CSM) design** | Details — IIT Madras
*Course Project | Digital IC design | Guide: Prof. Janakiraman* — Oct 2021 - Nov 2021
– Designed the schematic and layout of **8bit signed CSM**, with and without pipelining using **Electric** software.
– Optimized performance by employing various configurations of vector merge, using various full adders (CSA, LCSM).
– Validated the **DRC & LVS checks**, performed **RC extraction** for the layout and simulated using LTSpice.

**RISC-V CPU core** | Details — Remote
*Personal Project* — June 2021
– Implemented a **5-stage pipelined** 32-bit RISC-V ISA processor design in Transaction-Level Verilog (**TL-Verilog**).
– Incorporated **Hazard-detection** and **Data forwarding** units | Tested in Makerchip platform.

**Circuit Solver Web Application** | Details — Remote
*Personal Project* — Aug 2020 - Sep 2020
– Developed a **circuit solver** in JavaScript that avoids manually solving complex circuits with controlled sources.
– Used Modified Nodal Analysis(**MNA**) algorithm. | Automatic node number generation | Implemented using draw2d.js.

## Relevant Coursework

- Computer Architecture *(Ongoing)*
- CAD for VLSI Systems *(Ongoing)*
- Digital System Testing and Testable Design
- Digital IC Design
- Microprocessor Theory+Lab
- Secure Processor Microarchitecture *(Ongoing)*
- Mapping Signal Processing Algorithms to DSP Architectures
- GPU Programming
- Computer Organization & Lab
- Digital Signal Processing

*G - Graduate Level Courses, level 5000 or higher

## Extra-Curricular Activities

**Core, Electronics Club, Center for Innovation (CFI)** — May 2021 - Apr 2022
– Spearheading a team of **50+** Electronics enthusiasts exploring diverse domains alongside managing the club activities.
– Organized a month-long session for **140+** participants, utilizing our **custom in-house MCU** and peripheral shields.

**Coordinator, Electronics Club, Center for Innovation (CFI)** — May 2020 - Apr 2021
– Handled all the club activities | Created and maintained the club website where we post interesting blogs.
– Conducted sessions on Machine Learning on Microcontrollers and MicroPython with our custom ESP32 to **100+** participants.

## Skills

**Programming Languages**: Python, C/C++, Assembly(ARM, RISC-V), Tcl, Bash, MATLAB, HTML, CSS, JavaScript.
**HDLs**: Verilog, TL-Verilog, SystemVerilog, Bluespec SystemVerilog.
**Tools and Softwares**: Xilinx Vivado, Vitis, PYNQ, ChampSim, Cachegrind, LT-Spice, Arduino, PyTorch, HLS4ML, cocotb.

## Teaching Experience

**Teaching Assistant for Prof. Nitin Chandrachoodan, Computer Organisation (EE2003) course** — Fall 2022
– Classroom responsibilities include weekly sessions for reviewing lecture material and assisting during lab sessions.
– Assignment responsibilities include creating test benches, grading assignments, and addressing students' concerns.

## Activities

– Talk on Rapid Hardware Prototyping Framework for FPGA - RISC-V MYTH Workshop 2022, VLSI System Design.
– Talk on Hardware efficient Bitonic Sorting Algorithm - Mini project seminar, IIT Madras.
– Instructor for the tutorial on Digital Design on FPGA using Makerchip - VSDOpen 2021 conference, VLSI System Design.
– Instructor for the workshop on **FPGA Programming - Building Whack-A-Mole game** - SHAASTRA 2021, IIT Madras.
– Selected among 100 students on a 14-day winter school on Computer Architecture conducted by the National Supercomputing Mission, India.