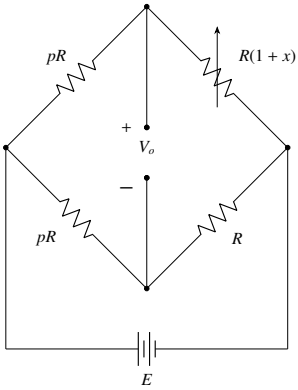
2015-EE-40-52

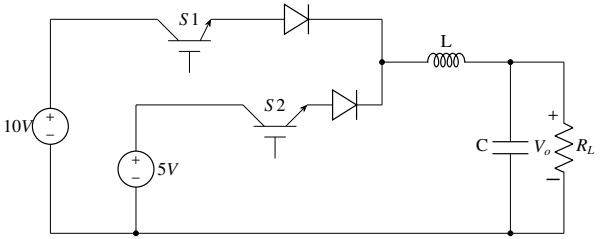
EE24BTECH11010 - BALAJI B

1) An unbalanced *DC* Wheatstone bridge is shown in the figure. At what value of p will the magnitude of V_0 be maximum? (2015-EE)

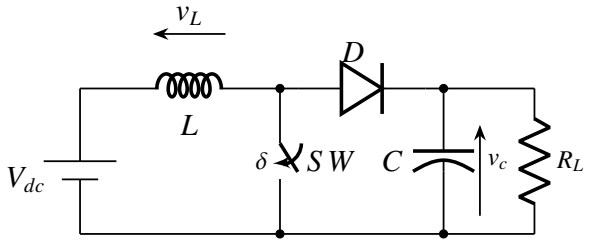


a) $\sqrt{(1+x)}$ b) $(1+x)$ c) $\frac{1}{\sqrt{(1+x)}}$ d) $\sqrt{(1-x)}$

2) The circuit shown is meant to supply a resistive load R_L from two separate *DC* voltage sources. The switches S_1 and S_2 are controlled so that only one of them is ON at any instant. S_1 is turned on for $0.2ms$ and S_2 is turned on for $0.3ms$ in a $0.5ms$ switching cycle time period. Assuming continuous conduction of the inductor current and negligible ripple on the capacitor voltage, the output voltage V_o (in Volt) across R_L is _____. (2015-EE)



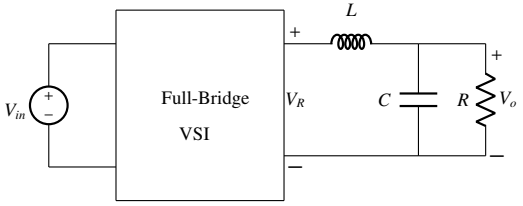
3) A self commutating switch SW operated at duty cycle δ is used to control the load voltage as shown in the figure



Under steady state operating conditions, the average voltage across the indicator and the capacitor respectively, are (2015-EE)

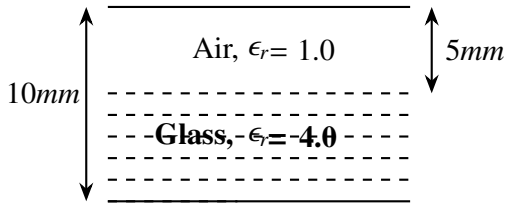
a) $V_L = 0$ and $V_C = \frac{1}{1-\delta}V_{dc}$
b) $V_L = \frac{\delta}{2}V_{dc}$ and $V_C = \frac{1}{1-\delta}V_{dc}$
c) $V_L = 0$ and $V_C = \frac{\delta}{1-\delta}V_{dc}$
d) $V_L = \frac{\delta}{2}V_{dc}$ and $V_C = \frac{\delta}{1-\delta}V_{dc}$

4) The single-phase full-bridge voltage source inverter (VSI) shown in figure, has an output frequency of $50Hz$. It uses unipolar pulse width modulation with switching frequency of $50kHz$ and modulation index of 0.7 For $V_{in} = 100V$, $L = 9.55mH$, $C = 63.66\mu F$ and $R = 5\Omega$ the amplitude of the fundamental component in the voltage V_o (in Volt) under steady-state is _____ (2015-EE)

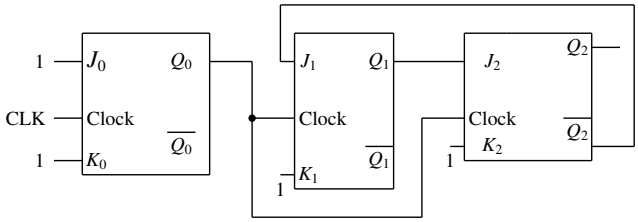


5) A 3-phase 50 Hz square wave (6-step) VSI feeds a 3-phase, 4 pole induction motor. The VSI line voltage has a dominant 5^{th} harmonic component. If the operating slip of the motor with respect to fundamental component voltage is 0.04, the slip of the motor with respect to 5^{th} harmonic component of voltage is _____ (2015-EE)

6) A parallel plate capacitor is partially filled with glass of dielectric constant 4.0 as shown below. The dielectric strengths of air and glass are $30kV/cm$ and $300kV/cm$, respectively. The maximum voltage (in kilovolts), which can be applied across the capacitor without any breakdown, is _____ (2015-EE)



7) The figure shows a digital circuit constructed using negative edge triggered $J-K$ flip flops. Assume a starting state of $Q_2Q_1Q_0 = 000$ This state $Q_2Q_1Q_0 = 000$ will repeat after _____ number of cycles of the clock CLK. (2015-EE)



8) $f(A,B,C,D) = \Pi M(0,1,3,4,5,7,9,11,12,13,14,15)$ is a maxterm representation of the Boolean function $f(A,B,C,D)$ where A is the MSB and D is the LSB. The equivalent minimized representation of this function is (2015-EE)

a) $\left(A+\bar{C}+D\right)\left(\bar{A}+B+D\right)$
b) $A\bar{C}D+\bar{A}+B+D$
c) $\bar{A}CD+A\bar{B}CD+A\bar{B}\bar{C}\bar{D}$
d) $\left(B+\bar{C}+D\right)\left(A+\bar{B}+\bar{C}+D\right)\left(\bar{A}+B+C+D\right)$

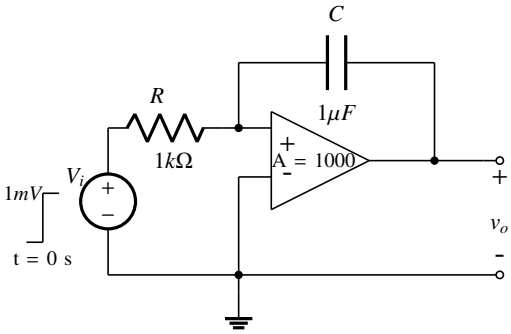
9) Consider a discrete time signal given by

$$x[n] = (-0.25)^n u[n] + (0.5)^n u[-n-1]$$

The region of convergence of its Z-transform would be (2015-EE)

a) the region inside the circle of radius 0.5 and centered at origin
b) the region outside the circle of radius 0.25 and centered at origin
c) the annular region between the two circles, both centered at origin and having radii 0.25 and 0.5
d) the entire Z plane

10) The op-amp shown in the figure has a finite gain $A = 1000$ and an infinite input resistance. A step voltage $V_i = 1mV$ is applied at the input at time $t = 0$ as shown. Assuming that the operational amplifier is not saturated, the time constant (in millisecond) of the output voltage V_o is (2015-EE)



11) An 8-bit, unipolar Successive Approximation Register type ADC is used to convert $3.5V$ to digital equivalent output. The reference voltage is $+5V$ The output of the ADC at the end of 3^{rd} clock pulse after the start of conversion, is (2015-EE)

a) 1010 0000
b) 1000 0000
c) 0000 0001
d) 0000 0011

12) Consider the economic dispatch problem for a power plant having two generating units. The fuel costs in Rs/MWh along with the generating limits for the two units are given below:

$$C_1(P_1) = 0.01P_1^2 + 30P_1 + 10 \; ; \; 100MW \leq P_1 \leq 150MW$$
$$C_2(P_2) = 0.05P_2^2 + 10P_2 + 10 \; ; \; 100MW \leq P_2 \leq 180MW$$

The incremental costs (in Rs/MWh) of the power plant when it supplies $200MW$ is (2015-EE)

13) Determine the correctness or otherwise of the following Assertion [a] and the Reason [r]

Assertion: Fast decoupled load flow method gives approximate load flow solution because it uses several assumptions.

Reason: Accuracy depends on the power mismatch vector tolerance. (2015-EE)

a) Both [a] and [r] are true and [r] is the correct reason for [a].
b) Both [a] and [r] are true but [r] is not correct reason for [a].
c) Both [a] and [r] are false
d) [a] is false and [r] is true