COEN 6501 – Project Description – Fall 2023

I. Project Description

The aim of this project is to design an Arithmetic Unit capable of calculating the following formula:

$$P = \frac{A * B}{4} + 1$$

The operands are two 8-bit unsigned inputs A and B. P is the 16-bit unsigned output. The two operands are latched into internal registers on the rising edge of the input clock when input load is set to 1 and the calculation starts thereafter. When completed, output status is set to 1 and result is available on output P. The design includes internal registers to store the operands and the result. Finally, the $\overline{reset}$ input (active low) will set all internal registers as well as the output to zero. Figure 1 illustrates the block diagram of the design.

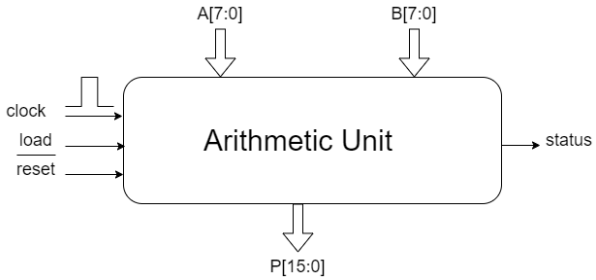

Figure 1: Arithmetic unit block diagram

Minimum design requirements are as follows:

1. Model your circuit using structural VHDL.
2. Chose the multiplier among existing solutions (e.g., Array Multiplier, Booth Multiplier, etc.) and justify your choice.
3. Provide a comprehensive testbench. Make sure to cover enough scenarios to validate the correctness of your design.

Additional requirements:

1. Provide a generic design allowing to simulate and synthesize the unit with any operand size chosen at design time.
2. Provide a generic VHDL model allowing to calculate the formula with C and D being user inputs (note: the size of C and D is defined at design time, but their value is specified by the user and can thus change):
$$P = \frac{A * B}{C^2} + D$$
3. Modify your design to enable the use of signed number for A and B.

4. To reduce the I/O count, use serial IOs for the inputs and the output. If necessary, add any control signal you find relevant.
5. Optimize the design in terms of speed and FPGA resource utilization.

II. Project Report and Source code

Use the Concordia Form and Style to prepare your report:

https://www.concordia.ca/content/dam/ginacody/docs/Form-Style.pdf

Submit your project report as a single .pdf file that include:

1. Confirmation of Originality Form (signed by all team members).
2. Cover page, abstract, introduction, dedicated sections for your design, conclusion (summary, possible improvements) and references.
3. A conceptual diagram for the design. Clearly label each block e.g., internal registers, flip-flops, logic gates) and provide a detailed description of the design. Justify your design choices.
4. Simulation results to validate the design functionality.
5. Based on the results, comment on the quality of the design in term of speed and resource utilization.
6. Do not include any VHDL code in your report.

Include all the source files, such as VHDL codes, test benches, simulation files, etc., in a single ZIP file along with the report. Ensure that the source code is organized as a ModelSim project and contains a README file that indicates the organization.

III. Report Submission Deadline

Project reports due date is December 11 at 23:59. A Moodle submission link will be available.

IV. Evaluation and grading criteria

The project will be evaluated based on:

- Delivery on time.
- High level description of the specification to be realized.
- Design methodology.
- Quality of the VHDL code.
- Simulation and synthesis results.
- Report, documentation, and presentation.

Grade Range	Criteria
90-100	Outstanding, **surpassed** requirements and perfectly organized report
85-89	Excellent, met **all** minimum and **all** additional requirements
80-84	Excellent, met **all** minimum and **most** additional requirements
70-79	Good quality, met **all** minimum and **some** additional requirements
60-69	Average quality, met **all** minimum requirements
0-59	Reserved for **poor results** or student that did not put in much effort