EXPERIMENT-7

Aim:

To make a half adder & full adder logic gate

Components Req:

And gate, XOR gate, Input, output, OR Gate.

Procedure:

i) Half adder:

$$S = \bar{X}X + X\bar{Y}$$

$$C = XY$$

S=Sum, C=Carry.

S can also be written as $S = X \oplus Y$

XOR Gate.

ii) Full adder:

$$S = \bar{X}\bar{Y}C_{in} + \bar{X}X'C_{in} + X\bar{Y}\bar{C}_{in} + XYC_{in}$$

$$S = C_{in}(\overline{\bar{X}Y + XY}) + \bar{C}_{in}(\bar{X}Y + X\bar{Y})$$

$$S = C_{in}(\overline{\bar{X}Y + X\bar{Y}}) + \bar{C}_{in}(\bar{X}Y + X\bar{Y})$$

$$S = C_{in} \oplus (X \oplus Y)$$

$$Cout = \bar{X}YC_{in} + X\bar{Y}C_{in} + XY\bar{C}_{in} + XYC_{in}$$

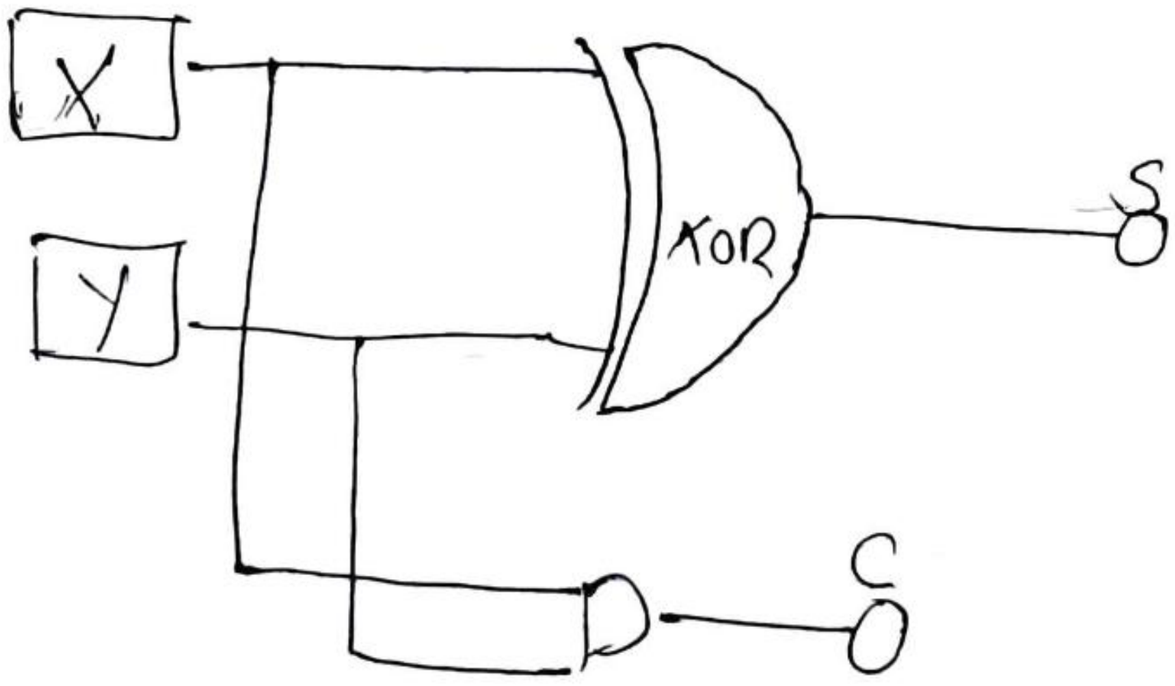
$$Cout = Cin(X \oplus Y) + XY$$

Result:

We have Sucessfully mode half full adder using logic gate simulation.

* Half adder:

X	Y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



* full adder:

X	Y	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0

1	0	1	0	1
1	1	0	0	1
1	1	1	1	1